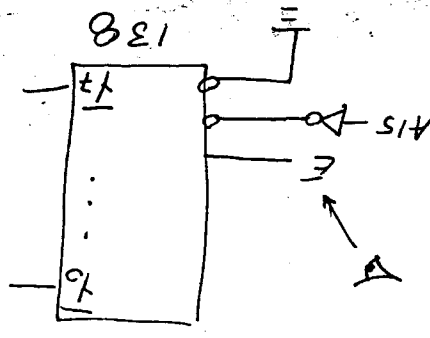


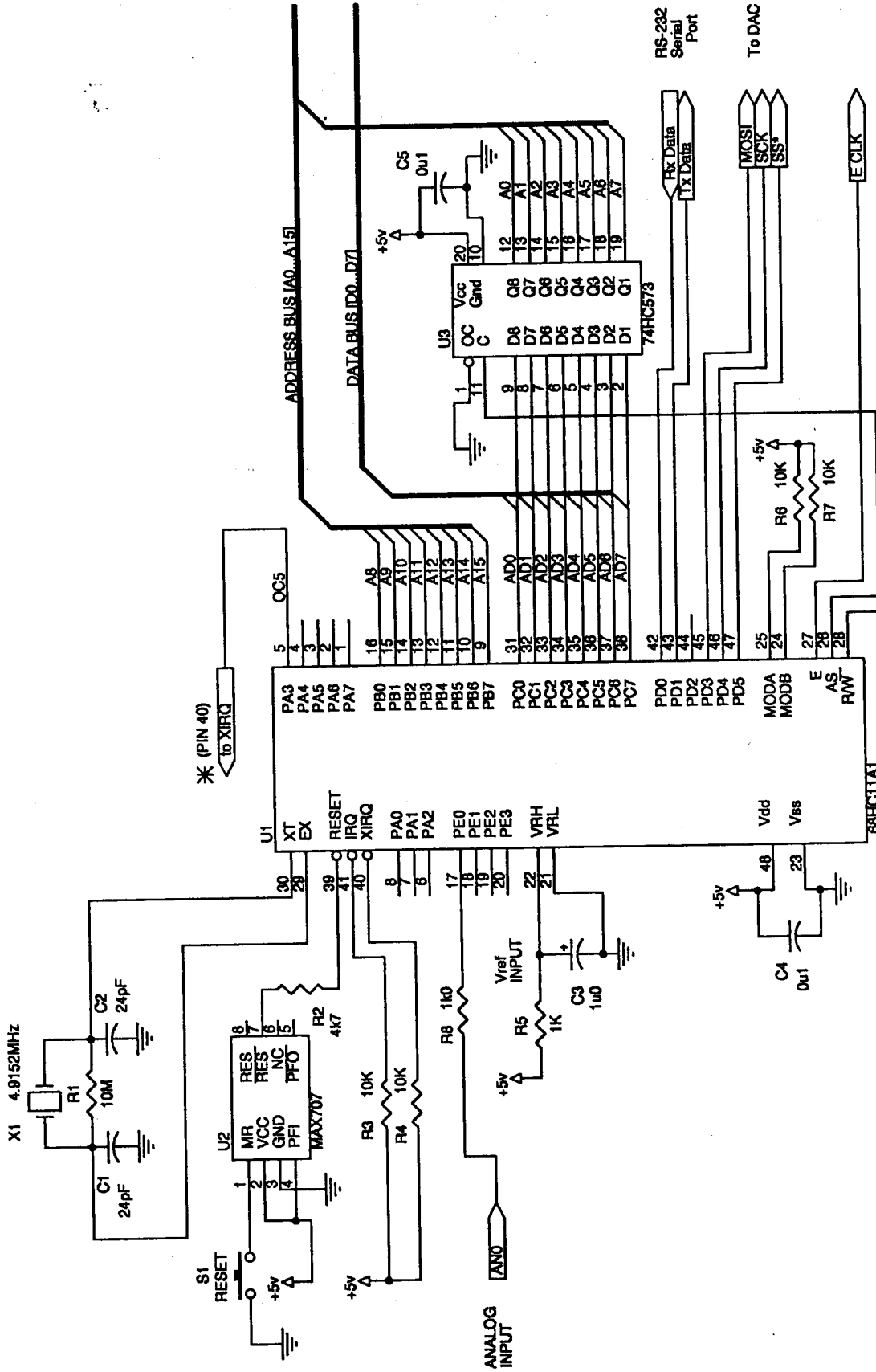
MUST NOT
 DELAY E
 w/ AGATE!



Note:

A/D, D/A and RS-232 interfaces are accessed via the internal registers (1000 - 103F).
 Cross-hatch indicates unused space.

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Title	68HC11 MEMORY MAP
Size	Document Number
A	MAP.11a
B	
REV	
B	
Date:	May 7, 1995
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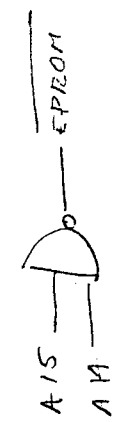
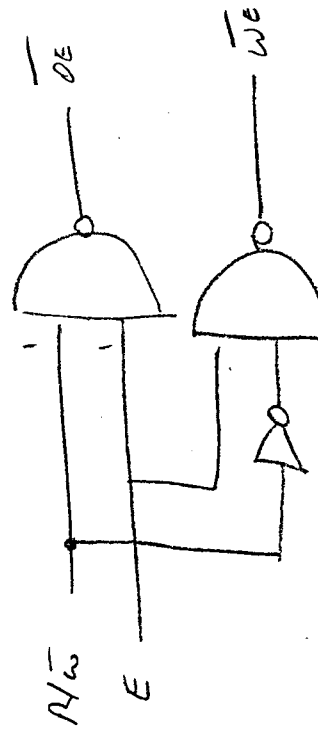
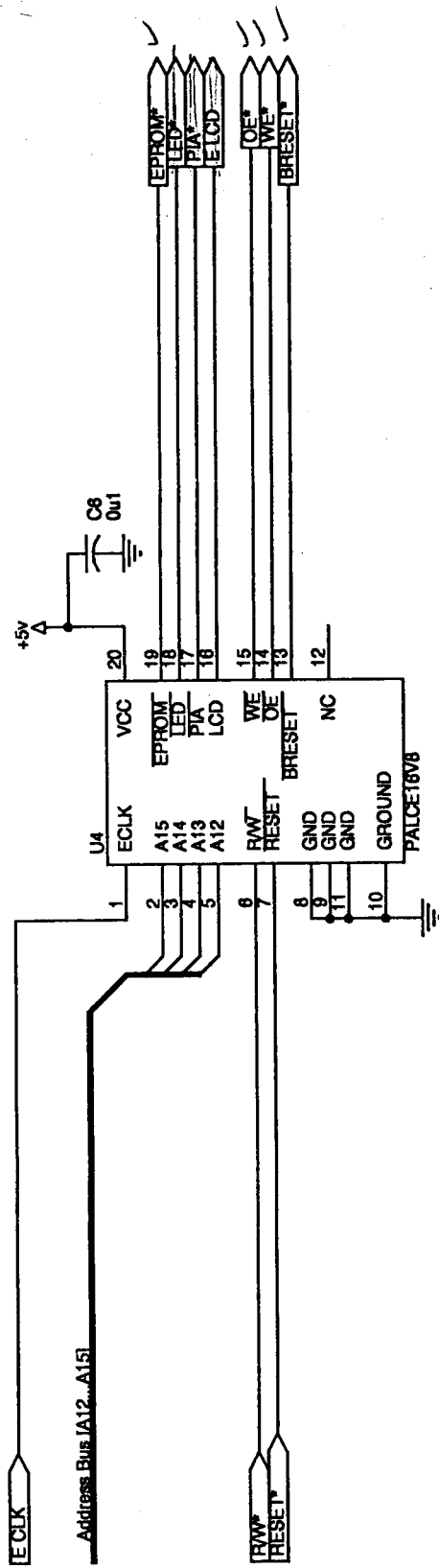
Notes:

1. For TRACE operation, OC5 must be tied to the XIRQ[®] input

Title	88HC11 CPU	
Size	Document Number	CPU.11a
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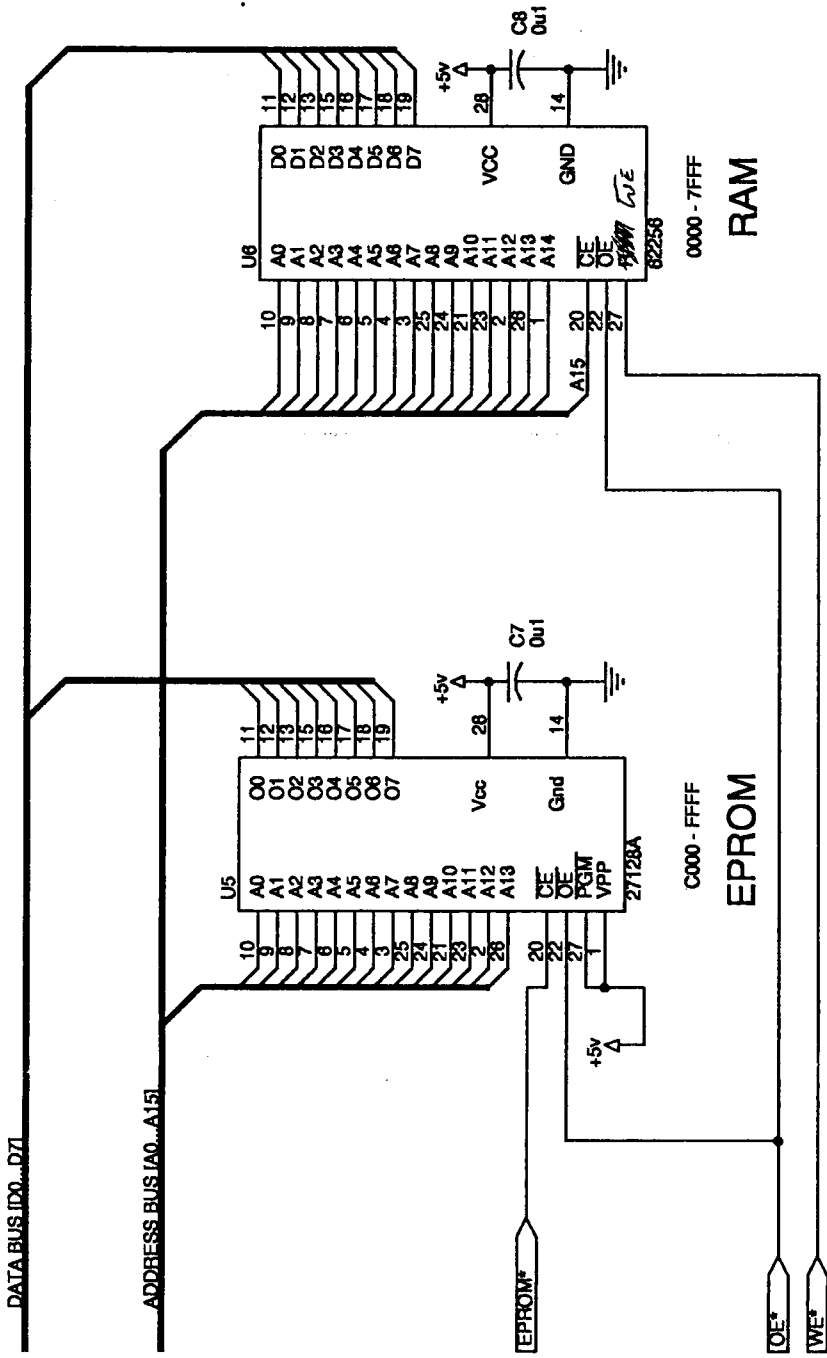
\overline{RES} — \overline{Do} — \overline{BRES}



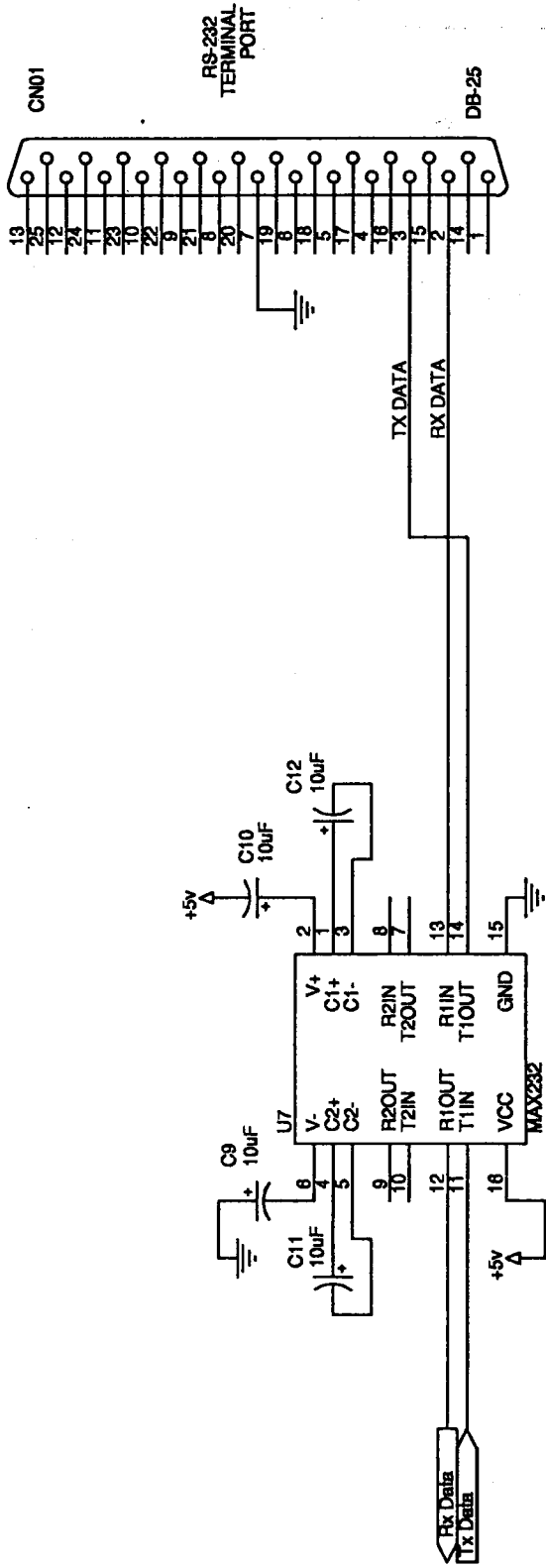
Note:

OE* and WE* are E qualified because RW* remains low throughout both cycles of a 16-bit write. Therefore, RW* must NOT be tied to any device requiring 16-bit writes (ie. RAM).

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Title 68HC11 ADDRESS DECODING	
Size A	Document Number ADDRESS.11a
Date: May 7, 1995	Sheet 3 of 6



DRAWN BY GRANT BEATTIE	
Title	68HC11 MEMORY
Size	Document Number
A	MEMORY.11a
Date:	May 7, 1995
Sheet	4 of 6
REV	B



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Title SCI RS-232 Serial Port			
Size A	Document Number SCI.11a	Sheet 5	of 6
Date: May 7, 1995	REV B		