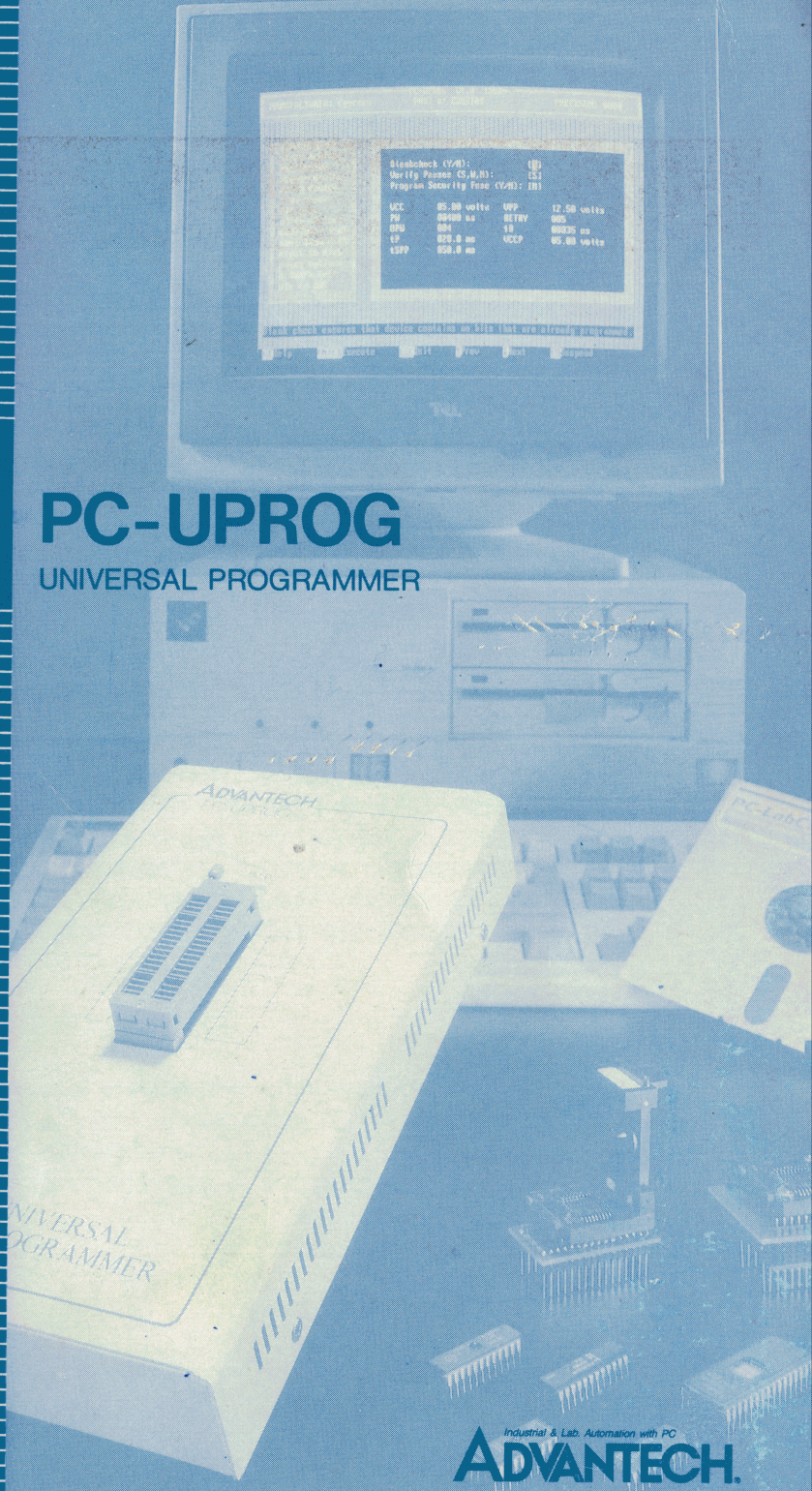
USERS' MANUAL

PC-UPROG

UNIVERSAL PROGRAMMER



Industrial & Lab. Automation with PC

ADVANTECH

PC-UPROG

UNIVERSAL PROGRAMMER

USER'S MANUAL

ACKNOWLEDGEMENTS

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CHAPTER 1. GENERAL INFORMATION

1.1. Introduction

Congratulations on purchasing the PC-UPROG programming tool. You will now experience the ease of use and flexibility that will make PC-UPROG the leading 'personal programmer' for professional users. With PC-UPROG, we have achieved professional quality combined with user upgradability at an affordable price. Our PC-UPROG system is designed with a 40-pin socket that supports most devices. PLCC, SO and LCC devices are also supported via industry standard adapters.

PC-UPROG is a convenient programming tool for all kinds of programmable devices, including PROMs and EPROMs (Erasable Programmable Read Only Memories), Flash EPROMs, EEPROMs (Electrically Erasable Programmable Read Only Memories), PALs (Programmable Array Logic), EPLDs (Erasable Programmable Logic Devices), FPLAs (Field Programmable Logic Arrays), Microcontrollers, and more. All popular technologies can be programmed, including bipolar, NMOS, CMOS, and more. PC-UPROG uses the popular IBM and IBM compatible desktop computers as its host system for data and algorithm storage, while actual programming is under control of the hardware pulse generators and D/A converters of the PC-UPROG system. PC-UPROG is very user-friendly, no special knowledge of programmable devices is required. All operations are menu driven and displayed in clear, easy to understand English text.

One key advantage of PC-UPROG is the ability to add new devices and features without modifying the hardware. Software updates are released on floppy disk.

We are responsive to your needs. Please write to us if you would like to have any devices added to the list of presently supported chips. We add devices as soon as they become available to us, with the priority set by feedback from our many customers.

Because the list of supported devices is growing rapidly, this manual contains no device list.

1.2. Specifications

1.2.1. Functions

Select Device
Select the device to be read or programmed from manufacturer and parts menus.

Read device
Read data from device in ZIF socket into RAM buffer.

Program device
Write to device in ZIF socket, from RAM buffer contents. (Perform optional blankcheck before programming or verify data after programming.)

Verify device
Compare the contents of a device in ZIF Socket with RAM buffer contents. Can select either standard or worst case VCC verify voltages.

Blank check
Check whether the device has not been programmed.

Edit data
Edit the contents of memory buffer using the following commands: goto, string search, fill, complement, copy, and calculate checksum.

Modify vector (logic devices only)
Editing or create functional test vectors, using test condition codes.

Functional test (logic devices only)
Execute the functional test using test vectors in RAM buffer.

Input from disk
Loads data, for programming, verify, or vector testing, from selected disk file into RAM buffer.

Output to disk
Saves the data from RAM buffer into disk file.

Device options
Allows programming parameters and device specs to be viewed or modified.

Hardware test
Performs diagnostic and calibration of hardware.

Quit to DOS
Exit the system to DOS and save current RAM buffer into temporary file.

1.2.2. Data Conversion Formats

Logic devices
JEDEC

Memory devices
Intel Hex, Motorola S, Tektronic Hex, HP64000ABS, and Binary.

1.2.3. Required PC Environment

Host computer	IBM PC/XT/AT or compatible
Memory	384K RAM or more.
Display	Hercules,CGA,VGA,EGA,MCGA or monochrome.
I/O ports	64 byte consecutive addresses; locations from 200 to 3C0 HEX.

1.2.4. Socket And Pin Drivers

Socket	40-pin ZIF socket, which accepts both 300mil and 600mil DIP devices.

VPP	Two separate programmable voltages from 5V - 25.5V, in 100mv steps, can be switched, under software control, with 350MA current limit, to any of 40 pins.
VCC	Programmable voltage source from 0V - 10V, in 50mv steps, under software control, to specific VCC pins.
Ground	3 relays, which are controlled by software, can select pin 20, pins 11 & 30, or pin 27 as ground.
Timer	On board real time clock that generates, CPU speed independent, programming pulses, in 200 ns steps.

1.2.5. General

PC adapter card
dimensions = 11.2cm x 10.6cm

Programmer Unit
dimensions = 25.4cm(L) x 14.9cm(W)

Total power consumption
+5V = 1A
+12V = 0.2A(Stand by), 1.0A(Active)
-12V = 0.1A (Max)

Connector: 37 pin D-type

1.2.6. Ordering Information

PC-UPROG	PC-based universal programmer, including universal programmer unit, PC adapter card (PCL-560A), system interface cable (PCX-79502-0.75)

Accessories furnished: System disk
Operations manual

PLCC-2020-01	20-pin PLCC to 20-pin DIP adapter
PLCC-2824-04	28-pin PLCC to 24 pin DIP adapter no connection pin on (5,8,11,19)
PLCC-2824-05	28-pin PLCC to 24 pin DIP adapter no connection pin on (1,8,15,22)
PLCC-3228-01	32-pin PLCC to 28 pin DIP adapter no connection pin on (1,12,17,26)
PLCC-3232-01	32-pin PLCC to 32-pin DIP adapter

CHAPTER 2. INSTALLATION

2.1. Initial Inspection

The PC-UPROG package consists of three basic functional units:

1. An IBM Compatible Plug-in Board
   The PC-UPROG plug-in board contains all the hardware logic that is required to interface between the IBM compatible PC/XT/AT computer and the programmer unit. The PC-UPROG plug-in board should be left permanently installed in the user's IBM compatible PC/XT/AT computer, it does not interfere with normal operation.

2. Floppy Disk Based Software
   The standard PC-UPROG package contains 1 floppy disk which contains all the programs and utilities that you need to use PC-UPROG. The programs on the floppy disk directly control the hardware logic of the programmer unit.

3. One 75cm long 37-pin D-TYPE connector cable.

4. Programmer unit
   The PC-UPROG programmer unit contains all the hardware needed to program a device.

2.2. Changing hardware I/O Ports

The PC-UPROG PC adapter card contains a DIP switch (SW1) which may be reconfigured to change the I/O port base address that the hardware recognizes. The following is a table of possible I/O port base address settings and their corresponding DIP configurations.

I/O Address (Hex)	Switch Position 1 A8	2 A7	3 A6	4 A5
200 hex	ON	ON	ON	ON
240	ON	ON	OFF	ON
280	ON	OFF	ON	ON
2C0	ON	OFF	OFF	ON
300 *	OFF	ON	ON	ON
340	OFF	ON	OFF	ON
380	OFF	OFF	ON	ON
3C0	OFF	OFF	OFF	ON

* : Factory Setting

2.3. Hardware Installation

```
************************ WARNING ****************************
* TURN OFF your PC power supply whenever installing or     *
* removing PC-UPROG, or connecting or disconnecting cables.*
*************************************************************
```

PC-UPROG can be installed in any 8 or 16 bit slot of the IBM PC/XT/AT or compatible computer. PC-UPROG operation is completely independent of CPU clock speed. Systems from 4.77 MHz to over 25 MHz have been successfully used with PC-UPROG. Simply open the computer, and plug the card into a spare slot. PC-UPROG uses port address 300-32F hex. If you are aware of another card in your system with the same I/O port address, you should change the address of the PC-UPROG (or other card) now.

Installing the card in your computer:

1. Turn off your computer and all peripheral devices (such as printers and monitors).

2. Disconnect the power cord and any other cables from the back of the computer. Turn the system unit so the back of the unit faces you.

3. Remove the system unit cover (see your computer user's guide if necessary).

4. Locate the expansion slots at the rear of the unit and chose any unused slot.

5. Remove the screw that secures the expansion slot cover to the system unit (save the screw to secure interface card retaining bracket).

6. Carefully grasp the upper edge of the PCL-560 card. Align the hole in the retaining bracket with the hole on top of the expansion slot, and align the gold striped edge connector with the expansion slot socket. Press the board firmly into the socket.

7. Replace the screw in the expansion slot retaining bracket.

8. Connect the 37-pin D-TYPE connector cable between the PCL-560 adapter card and external programmer unit.

2.4. I/O Port Address Conflicts

We have chosen the address 300 hex for factory setting because very few other products have used this address for I/O cards. If you have problems during the software installation, (usually PC-UPROG will display an error message, during installation), please first temporarily remove other add-on cards from your system; if the problem goes away, that means there is an I/O port address conflict. Either PC-UPROG, or other board using address 300-33F hex, needs to be changed.

2.5. Changing your CONFIG.SYS file

Since PC-UPROG opens up to 10 file during operation, the system will return an error if the FILES parameter of CONFIG.SYS file is less than 15 (DOS already using 5 files).

The CONFIG.SYS file may be edited with any ASCII text editor.

2.6. Software Installation

The PC-UPROG software is distributed on one 360K diskette. The diskette initially contains only two files.

INSTALL.EXE	9K bytes
INSTALL.DAT	100K

First you should make a backup copy of the diskette (the PC-UPROG software is not copy protected). Keep the master diskette in a safe place (there is a nominal fee for replacement of lost disks).

After plugging in the board, boot your system with your standard DOS boot diskette or hard disk. If your system has a hard disk, insert PC-UPROG diskette into your floppy drive and type INSTALL C: The install utility will create the directory '\PC-UPROG' on your hard disk, and install the following files.

pc-uprog.dev
pc-uprog.dmp
pc-uprog.pin
pc-uprog.fam
pc-uprog.wav
pc-uprog.exe

The install utility will then test the hardware to verify that programmer unit and PC adapter card are installed correctly. If any error occurs, repeat the hardware installation process and try again.

For floppy disk installation, insert PC-UPROG diskette into drive A: and the destination diskette into drive B: Then type INSTALL B:

After you have finished installation, go to directory '\PC-UPROG' and type 'PC-UPROG'. The system will now display the main menu and you may now refer to 'OPERATION' section of this manual for details on specific programming procedures, etc.

After exiting PC-UPROG software, PC-UPROG will have created two files.

pc-uprog.opt
pc-uprog.$$$

'pc-uprog.opt' contains the software I/O port base address and last device selected. 'pc-uprog.$$$' is the device data edit buffer.

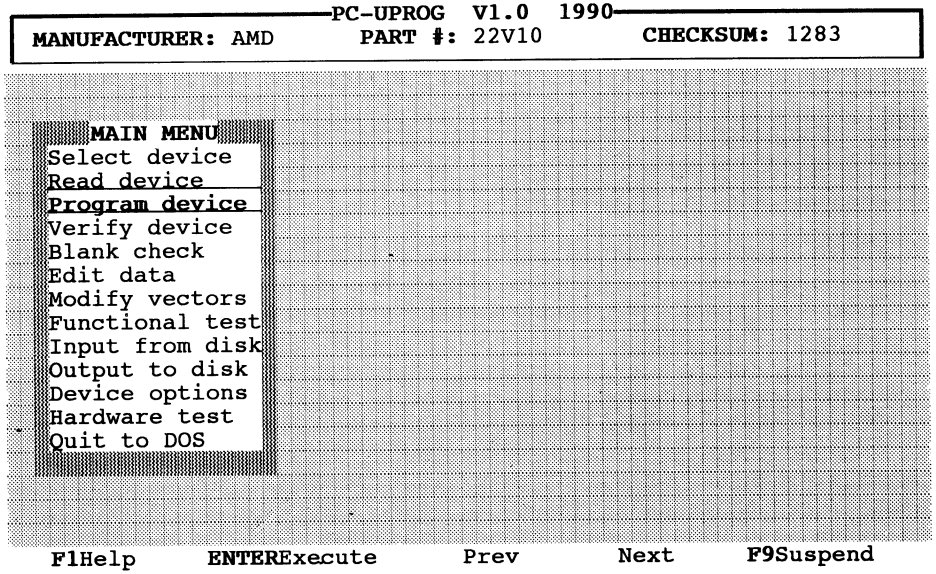
2.7. Starting PC-UPROG

The user should follow the instructions detailed in the Installation Section of this Manual in order to ensure correct installation (and eventual calibration) of the PC-UPROG programmer unit.

With the PC-UPROG board installed according to the installation instructions, power-on your computer. If using a hard disk, select the "\PC-UPROG" directory. If using a floppy based system, insert your copy of the PC-UPROG software into the floppy disk drive. Then enter the command:

C>PC-UPROG<cr>

The PC-UPROG main menu as shown below will be displayed.



2.8. Changing PC-UPROG's Software I/O Port

PC-UPROG I/O port base address defaults at 300 hex. However by executing the 'Set I/O port' command of the 'Hardware test' menu, we may change the I/O port base that the software uses to control the programmer unit. To change the I/O port base, perform the following sequence:

1. From 'Main menu' type 'H' to enter 'Hardware test' menu.
2. Type 'F' to select 'Set I/O port' command.
3. PC-UPROG will now display a list of possible I/O port base address settings.
4. Use the cursor keys to select the setting you desire.
5. PC-UPROG will now perform an I/O check to determine if there are any conflicts. If there are, PC-UPROG will display an error message and then allow you to select a new I/O port base address, otherwise it will return you to 'Hardware test' menu.

CHAPTER 3. OPERATION

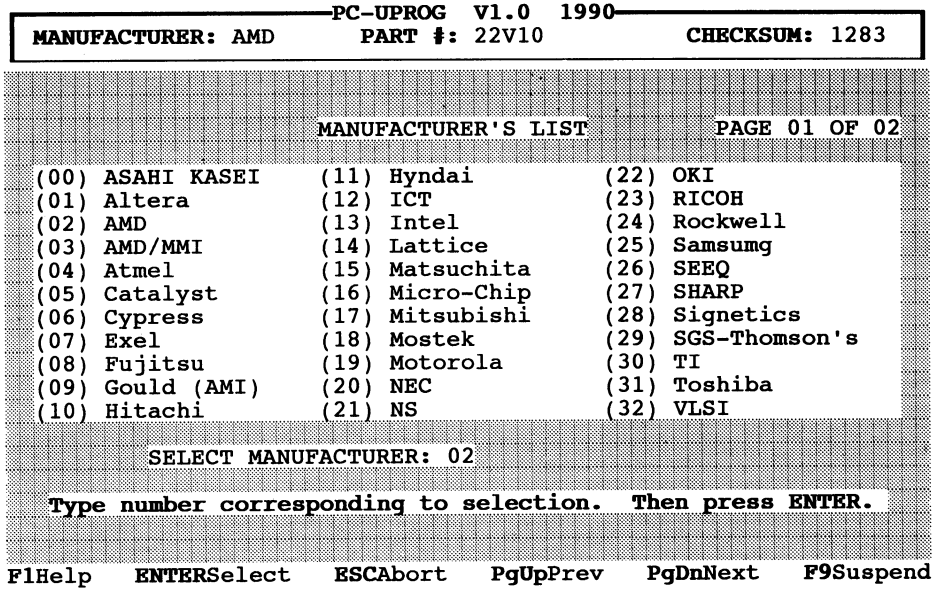
3.1. Cursor Control & Function Key Summary

The following control key may be accessed anywhere in the application.

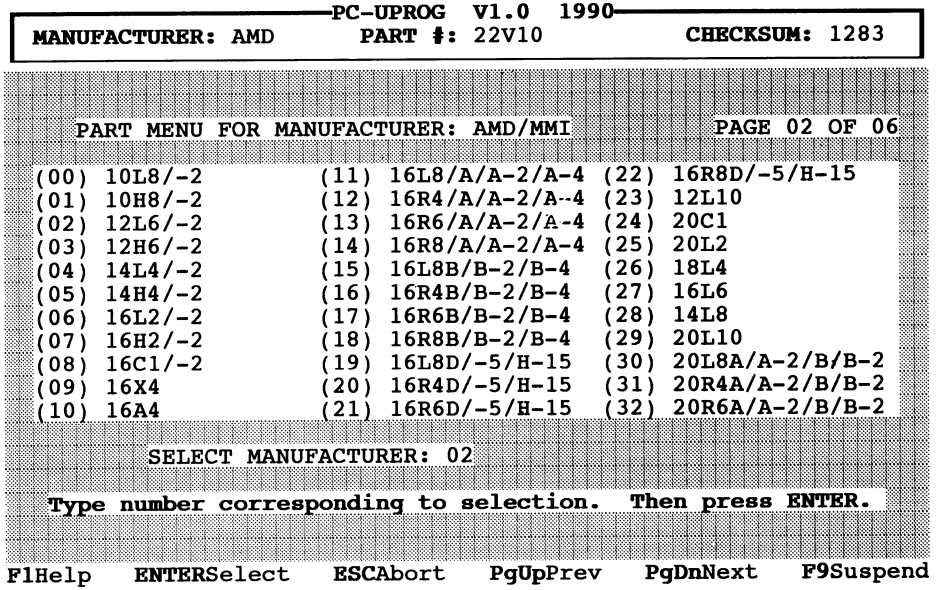
F1	Help.
F9	Suspends to DOS.
ESC	Goes to previous menu or aborts operation.
UpArrow	Moves menu selection bar to previous selection.
DownArrow	Moves menu selection bar to next selection.
ENTER	Executes the command or makes selection.

3.2. Select Device

This command may be used to change the active device type. When this command is selected the user is prompted with a menu of all the manufacturers currently supported by PC-UPROG.



The user may select the manufacturer by entering the number corresponding to that manufacturer and pressing ENTER. The user will then be prompted with a menu of all the devices currently supported for that manufacturer.



Select the device by entering the number corresponding to that device and pressing ENTER. The device menu may occupy more than one page. In this case, use the PgUp, PgDn, End, and Home keys to navigate through the menu.

When the device type is changed, the active memory buffer area is automatically changed to accommodate larger or smaller devices as necessary; however, data previously stored in the memory buffer remains unchanged until either a device is read, or data is read from the disk.

Pressing the Escape key 'ESC', at any time during the select device phase will return the user to the previous menu without affecting the currently selected device.

3.3. Read Device

This command reads the contents of the socketed device into the memory buffer. Note that after data has been read into memory, the same size or smaller device type may be selected without altering any data stored.

Pressing ENTER, at 'Read device' selection, or 'R' will begin the read operation. If the operation is successful, the "DEVICE READ OK" message will be displayed, otherwise the appropriate error message will be displayed.

WARNING: **Do not remove device until operation is complete, for it may damage device.**

After executing the initial read cycle, PC-UPROG may perform an additional verify, depending on 'Verify passes' option.

NOTE: See 'Device options' command for setting programming options.

3.4. Program Device

This command programs the socketed device with the contents of memory buffer.

Pressing ENTER, at 'Program device' selection, or 'P' will begin the program operation. If the operation is successful, the "DEVICE PROGRAMMED OK" message will be displayed, otherwise the appropriate error message will be displayed.

WARNING: **Do not remove device until operation is complete, for it may damage device.**

The device will first be checked for erasure (Blank check). If the device is EEPROM based, then an erase cycle will be automatically executed. If the device is not erased, and does not have an EEPROM cell, PC-UPROG will prompt "Device is not blank, continue programming (Y/N): [N]". Entering 'Y' will over-program the device.

The device will be programmed using the algorithm defined by the manufacturer. Intelligent, Flashrite, Rapid, Quickpulse, Quickpro, Page Mode and all other fast programming methods are used to keep the programming time to a minimum. The programming algorithm used is automatically determined by the manufacturer/device chosen. Most devices will be verified after programming each byte, however, PC-UPROG will perform an additional verify to confirm proper programming. If any errors are detected, they will be reported and the process will be aborted. If the chip vendor specifies it and the 'Verify passes' option equals (W)orstcase, verify will be done at the VCC high and low levels according to the data sheet. After verification, if the 'Program security fuse' option equals (Y)es, the security fuse of the device will be set (the 'Program security fuse' option is only available for devices with a security fuse).

NOTE: See 'Device options' command for setting programming options.

3.5. Verify Device

This command verifies that the contents of the socketed device is the same as contents of memory buffer.

Pressing ENTER, at 'Verify device' selection, or 'V' will begin the verify operation. If the operation is successful, the "DEVICE VERIFIED OK" message will be displayed, otherwise the appropriate error message will be displayed.

WARNING: **Do not remove device until operation is complete, for it may damage device.**

3.6. Blankcheck device

This command verifies that the socketed device is has not been programmed.

Pressing ENTER, at 'Blankcheck' selection, or 'B' will begin the blankcheck operation. If the operation is successful, the "DEVICE BLANKCHECKED OK" message will be displayed, otherwise the ap-

propriate error message will be displayed.

NOTE: Some devices have no defined unprogrammed state (unprogrammed fuses are floating), in which case, the blank check will always fail.

WARNING: Do not remove device until operation is complete, for it may damage device.

3.7. Edit data

This command allows the user to examine and/or modify the contents of the memory buffer.

Pressing ENTER, at 'Edit data' selection, or 'E' will bring you to one of two editors, depending on the device selected (memory or logic). One of the following two screens will then be displayed.

```
                    PC-UPROG  V1.0  1990
MANUFACTURER: AMD       PART #: 27C64

      00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D       ASCII
0000  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
0010  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
0020  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
0030  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
0040  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
0050  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
0060  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
0070  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
0080  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
0090  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00A0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00B0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00C0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00D0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00E0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF
          Cursor at address: 00034
F3Goto  F4Search  F5Fill  F6Complement  F7Copy  F8Checksum
```

or


```
                    PC-UPROG  V1.0  1990
MANUFACTURER: AMD       PART #: 22V10

      0000000000111111111122222222223333333333444444444455555555
      0123456789012345678901234567890123456789012345678901234567
0000  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
002C  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
0058  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
0084  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
00B0  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
00DC  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
0108  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
0134  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
0160  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
018C  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
01B8  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
01E4  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
0210  XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
          Jedec fuse #: 00B7
F1Help  F3Goto  F5Fill  ^EndDevice end  ^HomeDevice begin
```

By using the cursor keys any fuse or memory cell can be pointed to and changed if desired.

3.7.1. Cursor control (both editors)

LeftArrow	moves cursor left one column.
RightArrow	moves cursor right one column.
UpArrow	moves cursor up one row.
DownArrow	moves cursor down one row.
PgUp	moves cursor up one page.
PgDn	moves cursor down one page.
Home	moves cursor to the beginning of page.

End	moves cursor to end of page.
CtrlHome	moves cursor to beginning of buffer.
CtrlEnd	moves cursor to end of buffer.

3.7.2. Memory Editor commands

TAB	toggles between ASCII and HEX edit modes.
F3:Goto	goes to any address in the memory buffer.
F4:Search	this is an ASCII string search and may be used to find any ASCII string in the memory buffer.
F5:Fill	fills a range of the memory buffer with an ASCII character or HEX digit.
F6:Complement	performs one's complement on a range of the memory buffer.
F7:Copy	copies a block of the memory buffer to a new address.
F8:Checksum	calculates the checksum of a block of the memory buffer.

3.7.3. Logic Editor commands

F3:Goto	goes to any JEDEC address in the fusemap buffer.
F5:Fill	fills a range of the fusemap buffer with the fuse blown character (-) or fuse not blown character (X).

Some devices have fuse arrays greater than 80 character and therefore can not be displayed on one screen. The following commands only

apply to these devices.

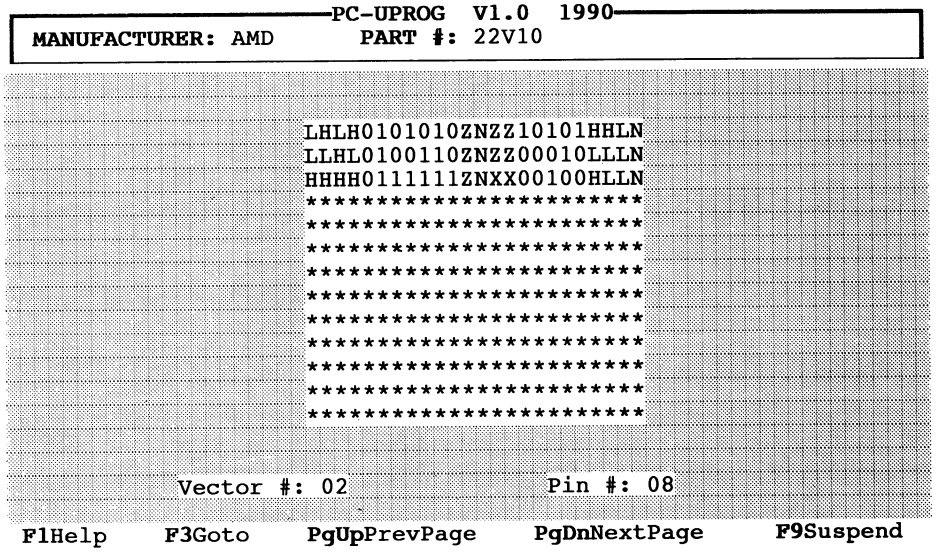
CtrlLeft	Shifts the fusemap buffer screen left one column.
CtrlRight	Shifts the fusemap buffer screen right one column.

3.8. Modify Vectors (Logic devices only)

Allows the user to edit or create functional test vectors, which will be used by 'Functional test' command to verify that device operates as designed. If test vectors are defined in JEDEC file, they will be automatically loaded when the fusemap is loaded. The test vectors can be created by ABEL, PALASM, CUPL or other PLD development system.

NOTE: Up to 1000 test vectors may be loaded or created.

Pressing ENTER, at 'Modify vector' selection, or 'M' will bring you to the vector editor and the following screen will be displayed.



The vector buffer is arranged in rows (corresponding to vector number) and columns (corresponding to pin number). Each vector consists of the test condition codes for each pin of the device. The valid test condition codes are:

0	Drive input low.
1	Drive input high.
B	Buried register preload.
C	Drive input low, high, low.
F	Float input or output.
H	Test output high.
K	Drive input high, low, high.
L	Test output low.
N	Power pins and outputs not tested.
P	Preload registers.
X	Output not tested, input default level.
Z	Test input or output for high impedance.

3.8.1. Vector Editor Commands & Cursor Control Keys

F3:Goto	goes to any vector in vector buffer.
LeftArrow	next pin.
RightArrow	previous pin.
DownArrow	next vector.
UpArrow	previous vector.
PgUp	moves cursor up one page.
PgDn	moves cursor down one page.
Home	moves cursor to beginning of page.
End	moves cursor to end of page.

CtrlHome	moves cursor to the beginning of buffer.
CtrlEnd	moves cursor to the end of buffer.

3.9. Functional Test (Logic devices only)

This command is used to execute the functional test vectors to determine if the device will operate according to the design.

Pressing ENTER, at 'Functional test' selection, or 'F' will begin the functional test operation. If the device passes the functional test, the "OPERATION PASSED." message will appear. Otherwise, an error message will be displayed indicating the vector number and pin number where the error occurred.

The functional test operation has 3 passes for each vector. Pass 1 sets up all input pins. Any 0, 1, or X levels are presented to the device. All device outputs are set to read mode. PC-UPROG has a special method for handling the 'X' (don't care) level, which is incompletely defined in the JEDEC specification and often is a cause of vector test failures in other systems.

Pass 1 also executes the preload function if a P or B vector is found. A P or B in pin 1 of the vector indicates preload. Note that entering and leaving preload mode can generate transient logic levels that can have other effects in a PAL design.

Pass 2 applies any clocks to the device. The vector is scanned from lowest pin to highest pin, and the clocks are output in that order. If a multiple clock device requires a controlled sequence of clocks, then there should be a separate vector for each clock. It is impossible for a universal programmer like PC-UPROG to generate simultaneous clocks on 2 pins. There will always be a time spacing between multiple clocks in a test vector. Note that the 'C' clock is normally low, and the 'K' clock is normally high.

Pass 3 verifies the outputs of the device against the test vector. If there are no errors, the next vector is processed.

Pins defined as 'X' in the vectors are set as inputs to '0' unless the

pin is determined to be an unused output, in which case it is floated. High impedance outputs are tested for incorrect '0' conditions, but not for low impedance '1' conditions. Test simulation also can be used to verify a device after the fuse has been programmed, (note that AMD PALCE family devices disable preload when security is set).

3.10. Sources Of Test Vector Errors

3.10.1. Preload

Preload is silicon device dependant. The same device type from different vendors use different preload sequences. Some of these sequences can interfere with normal device operation.

For example, if a Cypress 22V10 application uses pin 8 as an asynchronous reset input, then each time preload is done, the registers will be reset and the preload will fail. Other similar conditions exist with almost all devices. Use of the PC-UPROG vector editor will allow these problems to be quickly identified.

If preload of the output registers is attempted in a device that does not support preload, no high voltages will be applied, and an error message will be reported.

NOTE: As preload involves voltages above 5V, the device type selected must match the device in the socket. If an incorrect device is inserted in the socket, damage to that device may occur.

3.10.2. Power-on Reset

If the first line of a sequence of test vectors fails, check that the power-on condition is defined in the equations. It may be required to add an initialization test vector, to reset/preset the device registers, as the first vector.

3.10.3. Synchronous Clocks

With PC-UPROG, under certain conditions, it is possible that a device could double clock. Double clocking means that a counter or state machine advances 2 steps instead of one step. This can occur if the device is extremely fast. PC-UPROG can handle devices as fast as 15 ns without double clocking, some faster parts may double clock if all the outputs switch at the same time.

This problem exists in ALL universal programmers.

3.10.4. Asynchronous or Multiple clocks

Clocking devices with internal asynchronous clocks enabled (EP600, ATV750, 20RA10, etc.) may result in double clocking. This is application dependant, and exists only in extreme cases. The easiest solution is to disable the outputs before clocking the device.

If a device has multiple clocks, it is not possible to drive them at the same time, there will always be some hundreds of nanoseconds of delay between clocks. Use 2 vectors for multiple clock devices.

3.10.5. Signal Sequence

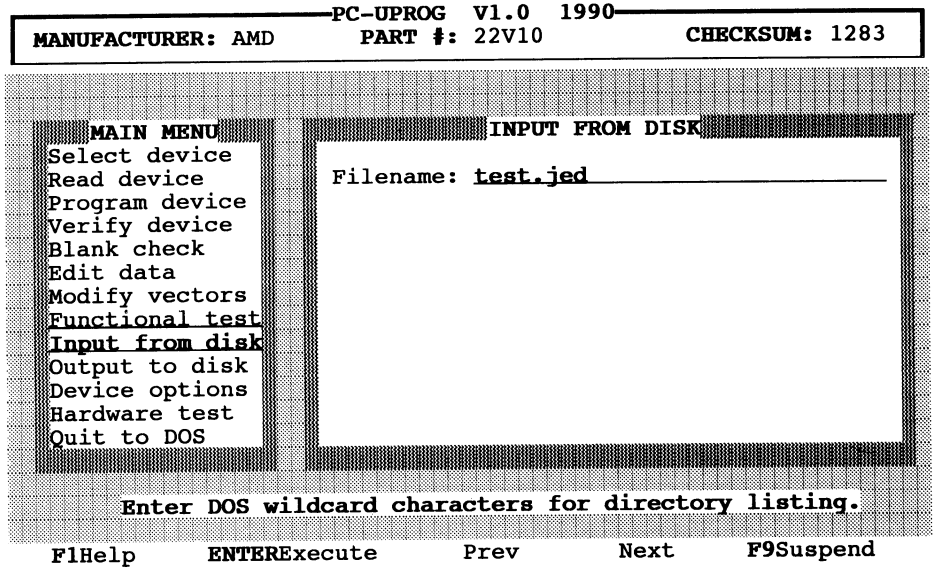
Pass 1 applies levels from pin 1 to the last pin of the device. Pass 2 applies clocks from pin 1 to the last pin of the device. Various equations are possible that may be affected by this sequence, for example a cross-coupled SET/RESET flip flop is possible in a 16L8 device, this could mis-function under certain vector sequences.

3.11. Input From Disk (Logic devices)

This command loads the data from the selected file into the fusemap buffer. The file to be loaded must be in the standard JEDEC format. The JEDEC file is generated by any PLD development system, for example PALASM, ABEL, CUPL, AMAZE, etc. The file contains all the data necessary to program the device for the desired function. If the data file contains test vectors, then these will be stored in a

separate buffer for use by the 'Modify vectors' and 'Functional test' commands. Up to 1000 vectors may be loaded.

When this command is selected, the user will be prompted with the following screen:



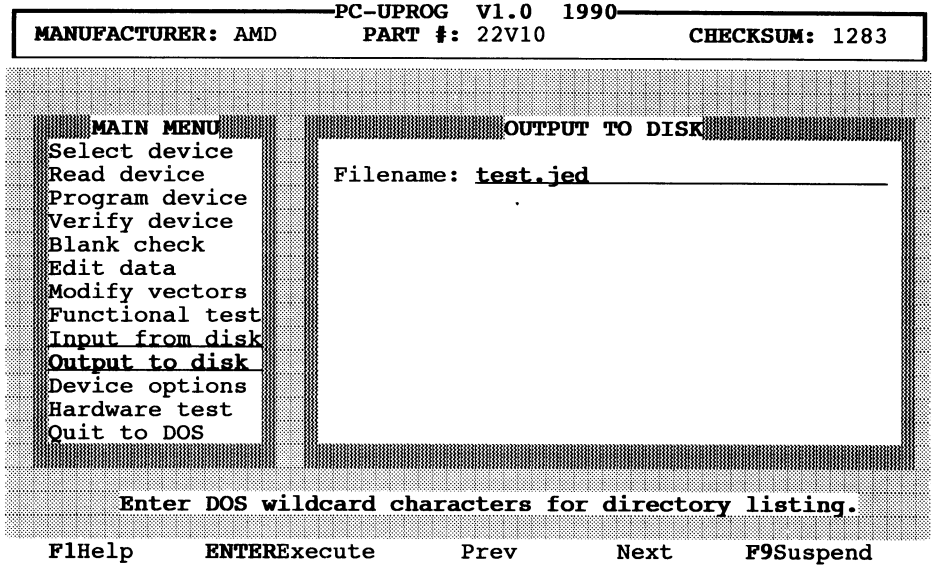
Filename - this is the drive/path/filename of the file to be loaded. Entering DOS wildcard characters will cause a directory listing to be displayed allowing the user to select the file to be loaded. For example, entering *.JED will cause all files with the extension .JED to be displayed.

After the filename is entered, the ENTER key may be pressed to begin the read operation. If the operation is successful, the "OPERATION COMPLETE." message will be displayed.

3.12. Output To Disk (Logic devices)

This command writes the fuse pattern and test vectors to disk, using standard JEDEC format.

When this command is selected, the user will be prompted with the following screen:



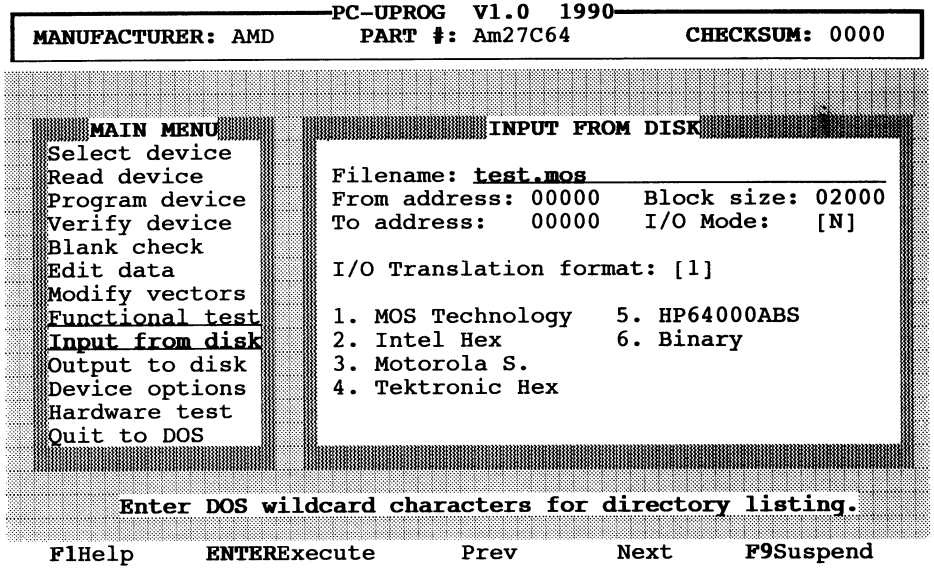
Filename - this is the drive/path/filename of the file to write data to. Entering DOS wildcard characters will cause a directory listing to be displayed allowing the user to select the file to write to. For example, entering *.JED will cause all files with the extension .JED to be displayed.

After the filename is entered, the ENTER key may be pressed to begin the write operation. If the operation is successful, the "OPERATION COMPLETE." message will be displayed.

3.13. Input From Disk (Logic devices)

This command loads the data from the selected file into the memory buffer. The file to be loaded must conform to one of the file formats supported by PC-UPROG.

When this command is selected, the user will be prompted with the following screen:



Filename -
this is the drive/path/filename of the file to be loaded. Entering DOS wildcard characters will cause a directory listing to be displayed allowing the user to select the file to be loaded. For example, entering *.MOS will cause all files with the extension .MOS to be displayed.

From address -
this specifies the starting address of the disk file to load edit buffer from.

To address -
this specifies the starting address of edit buffer load disk file to.

Block size -
size number of byte to load into edit buffer.

I/O translation format -
specifies the format of the file to be loaded. The currently supported file formats are: Intel Hex, Motorola S, Tektronic Hex, HP64000ABS, MOS Technology and Binary.

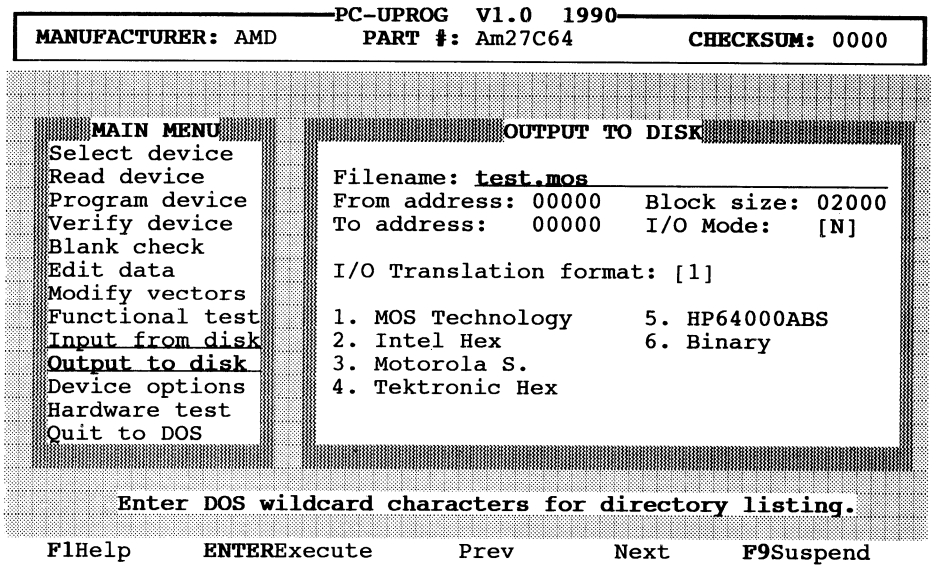
I/O mode -
specifies how the data is to be loaded into memory. Entering E (Even) specifies to load the data into even bytes only. O (Odd) specifies to load into odd bytes only. N (Normal) specifies to load into both odd and even bytes.

After the parameters are entered, the ENTER key may be pressed to begin the read operation. If the operation is successful, the "OPERATION COMPLETE." message will be displayed.

3.14. Output To Disk (Logic devices)

This command writes data from memory to disk using one of the currently supported file formats.

When this command is selected, the user will be prompted with the following screen:



Filename -

this is the drive/path/filename of the file to write data to. Entering DOS wildcard characters will cause a directory listing to be displayed allowing the user to select the file to write to. For example, entering *.MOS will cause all files with the extension .MOS to be displayed.

From address -

this specifies the starting address of edit buffer to begin writing to disk file from.

To address -

this specifies the starting address of disk file to write to.

Block size -

number of bytes to write to disk file.

I/O translation format -

specifies the format of the file to be loaded. The currently supported file formats are: Intel Hex, Motorola S, Tektronic Hex, HP64000ABS and Binary.

I/O mode -

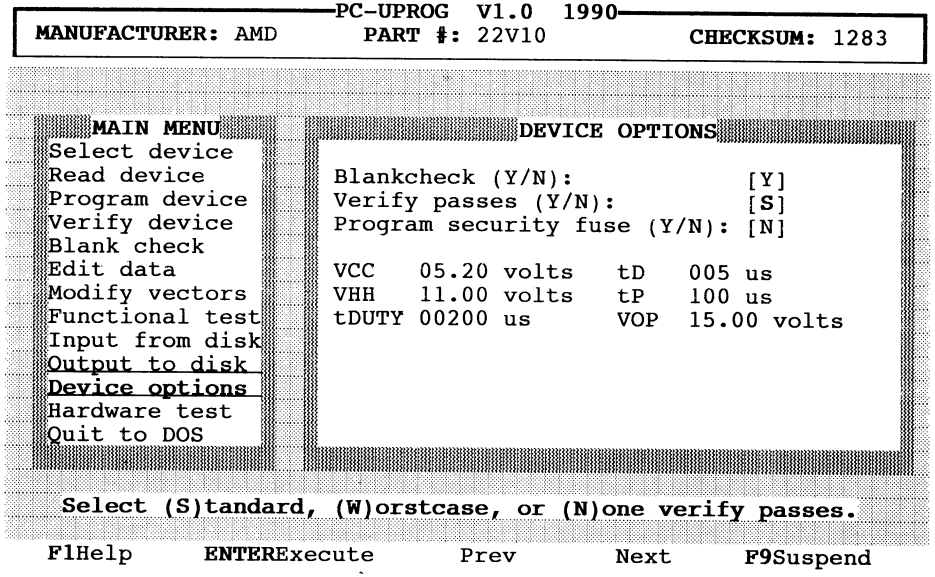
specifies how the data is to be written to the disk. Entering E (Even) specifies to write the even bytes only. O (Odd) specifies to write the odd bytes only. N (Normal) specifies to write both odd and even bytes.

After the parameters are entered, the ENTER key may be pressed to begin the read operation. If the operation is successful, the "OPERATION COMPLETE." message will be displayed.

3.15. Device Options & Parameter

This command is used to modified programming options and/or device specific parameters.

When this command is selected, the user will be prompt with the following screen:



Blank check -
verifies that the device is blank, before programming. Some devices automatically erase, before programming, in which case, this parameter would not apply.

Verify Passes -
this is the number and type of verification to be performed after programming or reading the device. [S]tandard performs verification at normal VCC operating voltage, [W]orstcase verifies at worstcase operating voltages, and [N]one does not perform any additional device verification. Note that most devices will still perform program verification after each word is programmed.

From address (memory devices only) -
this specifies the devices starting address to begin loading, programming, or verifying socketed device.

To address (memory devices only) -
this specifies the device's ending address to stop loading, programming, or verifying the socketed device.

Erase All -
erases the device before programming. Not all devices have this feature, in which case, this parameter would not be displayed.

Program Security Fuse -
programs the device's security fuse after programming.

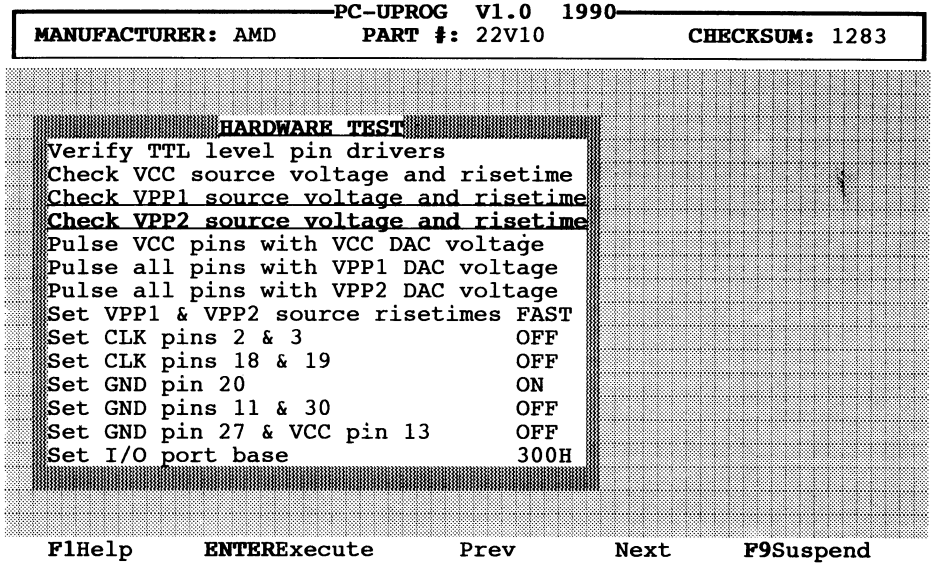
CAUTION: **after the security fuse is programmed, the device may not be read or verified. Not all devices have this feature, in which case, this parameter would not be displayed.**

The user will also be prompted with a number of device specific programming parameters, such as VCC, VPP, tD, PW, OPW, RETRY, etc. The type and number of these parameters will vary according to the device selected. Under normal conditions, these parameters should not be modified. If you want to modify any of these parameters please refer to manufacturer's programming specifications.

CHAPTER 4. HARDWARETEST & CALIBRATION

4.1. Hardware test

This command may be used periodically to verify that the unit is operating correctly and to calibrate the output voltages, or to change the I/O port base address. When this command is selected, the following menu will be displayed.



4.2. Verify TTL level pin drivers

Used to verify that TTL level read and write functions are operating correctly. When this command is selected, PC-UPROG will start testing every pin of the 40-pin DIP. It will continue testing until any key is pressed. The number of verify passes and pin# being tested will be continuously displayed.

4.3. Check VCC source voltage and risetime

Use this command to calibrate the VCC source voltage and verify that risetime is correct. To calibrate VCC source voltage, perform the following steps:

1. Use 'Set GND pin 20 ON/OFF' command to select pin 20 as ground pin.
2. Connect 500ohm resister between GND pin 20 and pin 40.
3. Connect digital multimeter probe between GND pin 20 and pin 40.
4. When this command is selected, the user will be prompt to enter voltage level between 5 and 10 volts.
5. After entering the voltage level and then pressing enter, the entered voltage level should be verified on multimeter. If there are any deviations, the VCC DAC adjustment screw (VR1) should be adjusted accordingly. Please remove the cover of PC-UPROG programmer unit and turn VR1 clockwise to increase DAC's voltage or counter-clockwise to decrease. Please refer to Fig. 1. The VR1, VR2, VR3 position.

To verify VCC source risetime is correct, perform the following:

1. Use 'Set GND pin 20 ON/OFF' command to select pin 20 as ground pin.
2. When this command is selected, the user will be prompt to enter voltage level between 0 and 10 volts and pin No. to be tested.
3. Connect 500ohm resister between GND pin 20 and selected pin.
4. Connect digital oscilloscope probe to GND pin 20 and selected pin.
5. Set the trigger level of oscilloscope to 3 volts.
6. Set time base of oscilloscope to 100us/div.

7. Set voltage/div of oscilloscope to 5V/div.
8. Upon pressing "enter" the Scope should be trigger and the time from 0 volts to 10 volts should be verified at about 300us +/- 50us.

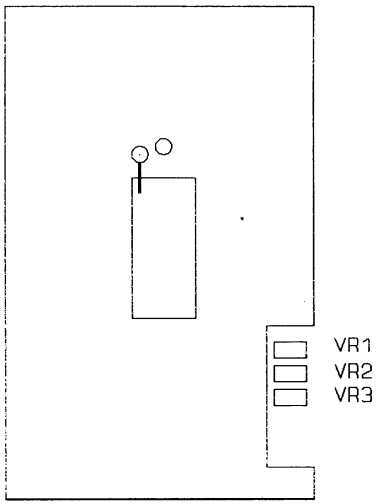


Fig.1 Position of VR1, VR2, VR3. CW for increase, CCW for decrease-

4.4. Check VPP1 source voltage and risetime

Use this command to calibrate the VPP1 source voltage and verify that risetime is correct. To calibrate VPP1 source voltage, perform the following steps:

1. Use 'Set GND pin 20 ON/OFF' command to select pin 20 as

ground pin.

2. When this command is selected, the user will be prompt to enter voltage level between 5 and 25 volts and pin No. to be tested.

3. Connect 1.1Kohm (1/2W) resistor between GND pin 20 and the selected pin.

4. Connect digital multimeter probe between GND pin 20 and the selected pin.

5. After entering the voltage level 25Volts and then pressing enter, the entered voltage level should be verified on multimeter. If there are any deviations, the VPP1 DAC adjustment screw (VR2) should be adjusted accordingly. Please remove the cover of PC-UPROG programmer unit and turn VR2 clockwise to increase DAC's voltage or counter-clockwise to decrease. Please refer to Fig. 1. The VR1, VR2, VR3 position.

To verify VPP1 source risetime is correct, perform the following:

1. Use 'Set GND pin 20 ON/OFF' command to select pin 20 as ground pin.

2. When this command is selected, the user will be prompt to enter voltage level between 5 and 25 volts and select pin number to be tested. Enter the maximum VPP2 source voltage which is 25 volts and pin No. to be tested.

3. Connect digital oscilloscope probe to GND pin 20 and selected pin.

4. Set the trigger level of oscilloscope to 3 volts.

5. Set time base of oscilloscope to 10us/div.

6. Set voltage/div of oscilloscope to 5V/div.

7. Upon pressing Enter the oscilloscope should have been trigger, and you can read the risetime of VPP2 source DAC. The time from 0 volt to 25 volts should be verified at 30us +/- 10us

4.5. Check VPP2 source voltage and risetime

Use this command to calibrate the VPP2 source voltage and verify that risetime is correct. To calibrate VPP2 source voltage, perform the following steps:

1. Use 'Set GND pin 20 ON/OFF command to select pin 20 as ground pin.

2. When this command is selected, the user will be prompt to enter voltage level between 5 and 25 volts and pin No. to be tested.

3. Connect 1.1Kohm (1/2W) resistor between GND pin 20 and the selected pin.

4. Connect digital multimeter probe between GND pin 20 and the selected pin.

5. After entering the voltage level 25Volts and then pressing enter, the entered voltage level should be verified on multimeter. If there are any deviations, the VPP2 DAC adjustment screw (VR3) should be adjusted accordingly. Please remove the cover of PC-UPROG programmer unit and turn VR3 clockwise to increase DAC's voltage or counter-clockwise to decrease. Please refer to Fig. 1. The VR1, VR2, VR3 position.

To verify VPP2 source risetime is correct, perform the following:

1. Use 'Set GND pin 20 ON/OFF' command to select pin 20 as ground pin.

2. When this command is selected, the user will be prompt to enter voltage level between 5 and 25 volts and select pin number to be tested. Enter the maximum VPP1 source voltage which is 25 volts and pin No. to be tested.

3. Connect digital oscilloscope probe to GND pin 20 and selected pin.

4. Set the trigger level of oscilloscope to 3 volts.

5. Set time base of oscilloscope to 10us/div.

6. Set voltage/div of oscilloscope to 5V/div.

7. Upon pressing Enter the oscilloscope should have been trigger, and you can read the risetime of VPP2 source DAC. The time from 0 volt to 25 volts should be verified at 30us +/- 10us

4.6. Pulse VCC pins with VCC DAC voltage

Use this command to verify that the VCC pulse generator is operating correctly. To verify VCC pulse, perform the following steps:

1. Use 'Set GND pin 20 ON/OFF' command to select pin 20 as ground pin.

2. Upon selecting this command, you will be prompted to enter a voltage and pulse width value. Enter maximum the source voltage which is 10 volts and pulse width of 500us.

3. Connect 500ohm resister between GND pin 20 and VCC pin to be tested. Pins 27, 28, 29, 30, 32, 34, 36, and 40 are driven by VCC DAC.

4. Connect digital oscilloscope probe to GND pin 20 and pin No. to be tested.

5. Set the trigger level of oscilloscope to 3 volts and continuous trigger mode.

6. Set time base of oscilloscope to 100us/div.

7. Set voltage/div of oscilloscope to 5V/div.

8. Upon pressing ENTER the scope should be triggered and the risetime from 0 to 10 volts should be measured at about 100us +/- 30us. The pulse width from start of rise to fall should measurement at 500us +/- 20us.

4.7. Pulse VPP1 pins with VPP1 DAC voltage

Use this command to verify that the VPP1 pulse generator is operating correctly. To verify VPP1 pulse, perform the following steps:

1. Use 'Set GND pin 20 ON/OFF' command to select pin 20 as ground pin.

2. Upon selecting this command, you will be prompted to enter a voltage and pulse width value. Enter the source voltage of 15V and pulse width of 100us.

3. Connect digital oscilloscope probe to GND pin 20 and pin to be tested.

4. Set the trigger level of oscilloscope to 3 volts and continuous trigger mode.

5. Set time base of oscilloscope to 100us/div.

6. Set voltage/div of oscilloscope to 5V/div.

7. Upon pressing "ENTER" the oscilloscope should begin triggering and the pulse width from start of rise to fall should measurement at 100us +/- 10us.

4.8. Pulse VPP2 pins with VPP2 DAC voltage

Use this command to verify that the VPP2 pulse generator is operating correctly. To verify VPP2 pulse, perform the following steps:

1. Use 'Set GND pin 20 ON/OFF' command to select pin 20 as ground pin.

2. Upon selecting this command, you will be prompted to enter a voltage and pulse width value. Enter the source voltage of 15V and pulse width of 100us.

3. Connect digital oscilloscope probe to GND pin 20 and pin to be tested.

4. Set the trigger level of oscilloscope to 3 volts and continuous trigger mode.

5. Set time base of oscilloscope to 100us/div.

6. Set voltage/div of oscilloscope to 5V/div.

7. Upon pressing "ENTER" the oscilloscope should begin triggering and the pulse width from start of rise to fall should measurement at 100us +/- 10us.

4.9. Set VPP1 and VPP2 source risetimes FAST or SLOW

Toggles the VPP1 & VPP2 source DACs risetimes between FAST (1.5V/us) and SLOW (25us/V). VPP1 & VPP2 will always have the same risetime). To verify that risetime is correct, do the following:

1. Use 'Set GND pin 20 ON/OFF' command to select pin 20 as ground pin.

2. Connect digital oscilloscope probe to GND pin 20 and any other of 40 pins.

3. Set the trigger level of oscilloscope to 3 volts.

4. Set time base of oscilloscope to 100us/div (SLOW) or 10us/div (FAST).

5. Execute 'Check VPP1 or VPP2 source voltage and risetime' commands.

6. You will then be prompted to enter a voltage. Enter the maximum source voltage which is 25.0 volts.

7. Upon pressing ENTER the oscilloscope should have been trigger, and you can read the risetime of VPP1 or VPP2 source DACs.

8. The time from 0 volts to 25 volts should be verified at about 35us +/- 5us FAST or 625us +/- 60us (SLOW).

4.10. Set CLK pins 2 & 3 ON/OFF

Use this command to enable or disable the 4MHz clock driving pins 2 & 3.

4.11. Set CLK pins 18 & 19 ON/OFF

Use this command to enable or disable the 2MHz clock driving pins 18 & 19.

4.12. Set ground pin 20 ON/OFF

Use this command to connect or disconnect the pin 20 ground relay.

4.13. Set ground pins 11 & 30 ON/OFF

Use this command to connect or disconnect the pin 11 & 30 ground relay.

4.14. Set ground pin 27 and VCC pin 13 ON/OFF

Use this command to connect or disconnect the ground pin 27 and VCC pin 13 relay.

4.15. Set I/O port base

Use this command to change to I/O port base address. When this command is selected, a menu of valid port base addresses will be displayed. After the new port base address is selected, PC-UPROG will automatically verify that there is no I/O conflict.

APPENDIX A. MESSAGES

ASCII mode not allowed with 4-bit device.

Might be displayed if user tries to enter ASCII mode while editing the memory buffer of 4-bit device. Since the ASCII format uses 8-bits, ASCII characters would be irrelevant to 4-bit devices.

BLANKCHECK ERROR.

Might be display after executing 'Blankcheck' command, if the device in socket is not blank. Some devices do not have a predefined blank state, in which case this message would be displayed whether device was blank or not. For these devices, a random checksum would indicate that the device is blank (floating).

CHECKSUM ERROR: RAM sum = xxxx File sum = xxxx.

During the 'Input from disk' command, if a (logic device) file is being loaded, and the calculated checksum does not match the file checksum, this message would be displayed.

DATA CHECKSUM ERROR.

During the 'Input from disk' command, if a (memory device) file is being loaded, and the calculated checksum does not match the file checksum, this message would be displayed.

DATA ERROR: Some record address were out of range and not loaded.

During the 'Input from disk' command, if a (memory device) file is being loaded and some of the records are out of range specified by FROM MEMORY ADDRESS and TO MEMORY ADDRESS.

DEVICE BLANKCHECKED OK.

Is displayed after executing 'Blankcheck' command if socketed device is blank.

DEVICE PASSED FUNCTIONAL TEST.

Is displayed after executing 'Functional test' command if all test vectors have passed.

DEVICE PROGRAMMED OK.
Is displayed after executing 'Program device' command if the socketed device has programmed correctly.

DEVICE READ OK.
Is displayed after executing 'Read device' command if the socketed device has loaded correctly.

DEVICE SPECIFIC ERROR: Could not PROGRAM initialization array.
Some devices such as ICT/AMI/GOULD PEEL153/253 have an initialization array which must be programmed for JEDEC fusemap compatibility with other similar devices. If this message is displayed it may indicate that the device is damaged and unusable.

DEVICE SPECIFIC ERROR: Could not program TEST array.
Some SIGNETICS bipolar devices have test arrays, which are not part of the JEDEC fusemap, however must be programmed so they don't interfere with the normal array. If this message is displayed, it may indicate that the device is damaged and unusable.

DEVICE SPECIFIC ERROR: Device code does not match.
Might be displayed while loading, programming, or verifying a LATTICE GAL22V10 device, if the wrong device has been inserted, or the device has been damaged.

DEVICE SPECIFIC ERROR: Device revision code does not match.
Might be displayed while loading, programming, or verifying an AMD PALCE device, if the wrong device has been inserted, the device has been damaged, or the new revision is not supported.

DEVICE SPECIFIC ERROR: Illegal algorithm revision.
Might be displayed while loading, programming, or verifying an LATTICE GAL devices, if the wrong device has been inserted, the device has been damaged, or the new revision is not supported.

DEVICE SPECIFIC ERROR: Manufacturer code does not match.
Might be displayed while loading, programming, or verifying an LATTICE GAL devices, if the wrong device has been inserted, or the device has been damaged.

DEVICE SPECIFIC ERROR: MES failed to program.
Might be displayed while programming LATTICE GAL devices and indicates that device may be damaged and unusable.

DEVICE SPECIFIC ERROR: Output registers not PRELOADed correctly.
Might be displayed while executing 'Functional test' command on a logic device that supports PRELOAD. See 'Source of functional test errors' section for details.

DEVICE SPECIFIC ERROR: TEST array has not been programmed.
Some SIGNETICS bipolar devices have test arrays, which are not part of the JEDEC fusemap, however must be programmed so they don't interfere with the normal array. This message might be displayed while verifying a device which has not yet had these fuses programmed. Execute the programming sequence, and these fuses will automatically be programmed.

DEVICE VERIFIED OK.
Is displayed after executing 'Verify device' command if the device's data matches edit buffer data.

DRIVE NOT READY.: Please check that drive door is closed.
Might be displayed during the 'Input from disk' or 'Output to disk' commands, if the user tries to read from or write to one of the floppy drive when it's drive door is open, or the diskette is not inserted properly.

FILE ERROR: Could not OPEN file.
Might be displayed during the 'Input from disk' or 'Output to disk' commands, if the user tries to read from or write to a file that has been corrupted, or tries to enter an illegal filename, etc.

FILE ERROR: File or path name not found.
Might be displayed during the 'Input from disk' or 'Output to disk' commands, if the user specifies a filename or pathname that does not exist.

FILE ERROR: No files found.
During the 'Input from disk' or 'Output to disk' commands, the user may enter wildcard characters in the filename, to display a menu of all files that match the wildcard argument. If there aren't any file that match this argument, this message will be displayed.

FILE ERROR: Path name specifies a directory or a read-only file.
Might be displayed during the 'Input from disk' or 'Output to disk' commands if the user enters a read-only file as the filename during 'Output to disk' command or a directory as the filename in either command.

FILE ERROR: System file names are illegal.
Is displayed if the user specifies a system file ('pc-uprog.xxx') as the filename during either 'Input from disk' or 'Output to disk' commands.

FILE ERROR: Unexpected end of file reached.
Might be displayed during the 'Input from disk' command if file specified by filename is not in the proper data translation format, or the file has been corrupted.

FUNCTIONAL TEST ERROR: Vector# xx Pin # xx
During the 'Functional test' command, if a vector fails the functional test, this message will be displayed.

HARDWARE ERROR: Stuck on HIGH at pin # xx.
During the 'Hardware test' -> 'TTL level' command, if a pin is unable to change from high to low, this message will be displayed.

HARDWARE ERROR: Stuck on LOW at pin # xx.
During the 'Hardware test' -> 'TTL level' command, if a pin is unable to change from low to high, this message will be displayed.

IO ERROR: Bad connection or device in socket.
This message might be displayed by installation utility if there is a problem with the PC adapter card or the programmer unit.

IO ERROR: I/O Port Address Conflict.
This message might be displayed during installation or during the 'Hardware test' -> 'Set I/O port' command, if the I/O port base address does not match PC adapter card's I/O port base address, or there is a conflicting add-on card.

IO ERROR: Serial # Mismatch.
This message might be displayed during installation or during the 'Hardware test' -> 'Set I/O port' command, if the Hardware is an Illegal copy or the ID chip has been damaged.

No test vectors to execute. Please create some.:
Upon executing 'Functional test' command, this message would be displayed if no test vectors were created or loaded.

OPERATION COMPLETE.
Indicates that the operation has been successfully completed.

OPERATION COMPLETE. Checksum = xxxx.
Would be display upon successful completion of 'F8:Checksum' command of 'Edit data' (memory device) function.

PROGRAM ERROR.
Might be displayed during the 'Program device' command, if the socketed device failed to program correctly. It indicates that the device failed the initial program verify.

SEEK ERROR. Please check that drive is connected properly.
Might be displayed during 'Input from disk' or 'Output to disk' commands if the drive specified in filename has a problem.

SORRY. Buried Register PRELOAD not supported for this device.:
Might be displayed during the 'Functional test' command if a Buried Register PRELOAD vector is encountered. It indicates that either the device does not support this function or that PC-UPROG does not support this function for this device.

SORRY. Register PRELOAD not supported for this device.
Might be displayed during the 'Functional test' command if a Register PRELOAD vector is encountered. It indicates that either the device does not support this function or that PC-UPROG does not support this function for this device.

String not found.
Might be displayed during the 'F4:Search' function of 'Edit data' (memory device) command, if the search string was not found.

USER ERROR: ILLEGAL KEY PRESSED.
Indicates that an illegal key was pressed.

USER ERROR: Illegal parameter entered.
Indicates that an invalid parameter was entered.

USER ERROR: Parameters out of range.
Indicates that the parameter entered, is out of range.

USER ERROR: Uninitialized fuse cell may not be edited.
Might be displayed during 'Edit data' (logic device) command, if the JEDEC buffer had not been initialized by loading a device from socket, loading a file from the disk, or using 'F5:Fill' command.

VERIFY ERROR (VCC High).
Might be displayed during the 'Verify device' command, when 'Verify passes' equals 'W', if the socketed device failed to verify correctly. It indicates that the device failed on VCC high verify pass.

VERIFY ERROR (VCC Low).
Might be displayed during the 'Verify device' command, when 'Verify passes' equals 'W', if the socketed device failed to verify correctly. It indicates that the device failed on VCC low verify pass.

VERIFY ERROR (VCC Normal).
Might be displayed during the 'Verify device' command, when 'Verify passes' equals 'S', if the socketed device failed to verify correctly.

INTERNAL ERROR: xxxxxxxxxxxxxxxxxxxxxxxxxxxx.
If this error is displayed, please write down the sequence that caused this error, and contact ADVANTECH Technical Support Department.