SECTION III
THEORY OF OPERATION

3-1. MAGNETIC CORE STORAGE.

3-2. CHARACTERISTICS OF CORES.

The primary storage element is a lithium ferrite core whose principal characteristic is a rectangular hysteresis loop, idealized in Figure 3-1. H is the magnetizing force applied to the core, and B is the magnetic flux produced by force H. If force H_1 is applied to the core and removed, the core is left with the remanent flux B_1 and is in the ONE state. If the magnetizing force is applied in the opposite direction ($-H_1$) the remanent flux is $-B_1$ and the core is in the ZERO state. Designations ZERO and ONE, with respect to the magnetization of the core, are arbitrary.

Magnetizing forces less than those required to saturate the core in either direction will not materially change the magnetic flux of the core. Abrupt reversal of flux direction results when the magnetizing force exceeds a critical value, and the core switches to the other of its two stable states. It will remain indefinitely in either state until switched back by a sufficient magnetizing force applied in the direction opposite to the force that set it initially.

Coincident current type operation is characterized by coincidence of two partial magnetizing forces $\frac{H1}{2}$ (or $-\frac{H1}{2}$) neither of which is sufficient to drive the core past the knee of the curve. The two partial magnetizing forces, acting simultaneously, will switch the core to a new state. These two forces are supplied by two drive half-currents applied along X and Y drive lines respectively (Figure 3-2). Switching can be prevented by application of an inhibit current, equal in value but opposite in direction, to

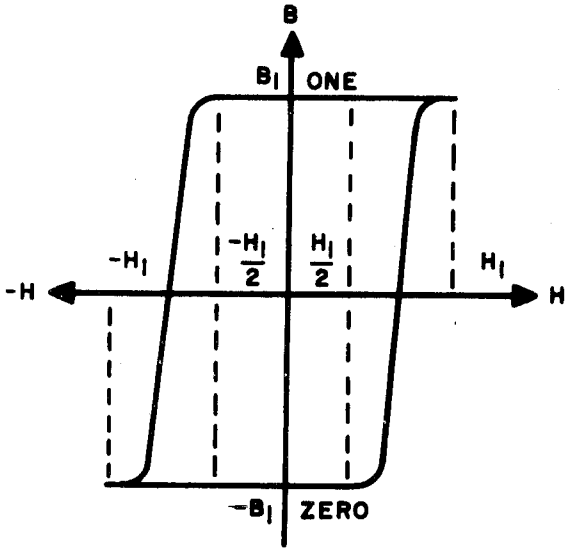


Figure 3-1.
Hysteresis Loop

either of the write drive half-currents. With the core in the ZERO state, it will switch to ONE with application of write half-drive currents to the X and Y drive lines; it will remain at ZERO when the inhibit current is applied simultaneously with the X and Y drive currents.

The state of a core is determined by application of read drive half-currents in a direction that would switch the core to the ZERO state. If the core is already in the ZERO state, it is driven minutely into saturation, producing a small flux variation. If the core is in the ONE state, switching to ZERO reverses the magnetic flux, and produces a large flux variation. In either case, the flux variations will appear in the form of a voltage induced in the sense winding.

3-3. MAGNETIC CORE ARRAYS.

Magnetic cores are mounted on intersecting drive lines in a matrix (mat). In a 4096 word memory, each mat has 64 X and 64 Y intersecting drive lines, with a magnetic core located at each drive line interesection (4096 cores per mat). A mat represents one bit of the data word. The sense line is threaded through each of the cores on the mat, with the ends of the line connected to a preamplifier, and thence to a sense amplifier. An inhibit winding is threaded through the cores on the mat, with its ends connected to an inhibit driver.

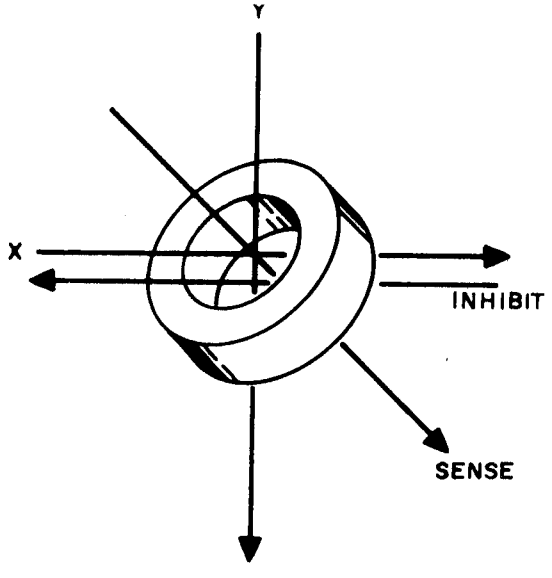


Figure 3-2.
Core Windings

The number of mats required by a memory is determined by the number of bits in the data word, with one mat for each data bit. Normally, four mats are mounted on one side of an array to provide a single-sided array, or four mats are mounted on each side of the array to provide a double-sided array.

3-4. MAGNETIC STACK.

The number of arrays making up the magnetic stack is a function of the data word length. For example, a 12-bit data word indicates one double-sided array (8 bits) and one single-sided array (4 bits). A 14-bit data word would necessitate one double-sided array, a second array with

four mats mounted on one side, and two mats mounted on the opposite side.

As it is possible to vary the number of bits in the data word, it is likewise possible to secure flexibility in the number of data words the system will process. In a 2048 word memory, 2048 cores are mounted on a mat, intersected by 32 X lines and 64 Y lines; in a 1024 word memory, the 1024 cores on a mat are intersected by 32 X lines and 32 Y lines; in a 512 word memory, the 512 cores are intersected by 16 X lines and 32 Y lines.

3-5. GENERAL THEORY.

3-6. INTRODUCTION.

The function of the equipment is to store binary data received from an external source, and to transmit this data to the external source upon receipt of the proper command. The system has five basic operational modes.

3-7. OPERATIONAL MODES.

The system is capable of two modes of operation as a memory, clear-write and read-restore; two modes of operation as a buffer, buffer-load and buffer-unload; and read-modify-write mode.

3-8. CLEAR-WRITE CYCLE. A clear-write cycle first clears the cores (resets them to ZERO) at the selected address. The external source having applied the data word to the data register, the word is written into the core storage at the cleared address.

3-9. READ-RESTORE CYCLE. A read-restore cycle first reads the data word out of core storage at the selected address and into the data register. The data word is then transmitted to the external source. Since a read operation destroys the information at the selected address (resets cores to ZERO), it is necessary to restore the data word from the data register to the core storage to complete the cycle.

3-10. BUFFER-LOAD. A buffer-load (write only) cycle writes information from the external source into core storage at the selected location. It requires that the cores at the selected address have been cleared (set to ZERO) by a preceding buffer-unload (read only) cycle.

3-11. BUFFER-UNLOAD. A buffer-unload cycle requires no previous preparation of the memory cores, so long as the desired data is stored

therein. At the conclusion of a buffer-unload cycle, the cores at the selected address remain in the reset (ZERO) state.

A buffer operation is initiated by application of the proper command to the memory/buffer control, and either SIC or SOC as determined by whether a buffer-load or buffer-unload operation is desired.

3-12. READ-MODIFY-WRITE OR SPLIT CYCLE. A read-modify-write cycle is initiated by application of a positive level to the read-modify-write control circuit, and the SOC command. This initiates a normal read operation in which the data word is read out of the cores at the selected address, is stored in the data register and transmitted to the external source. Following its modification there, the data word is applied to the data register, and upon receipt of the SIC command, the modified data word is written into the core memory at the original address. The only difference between a Buffer and a read-modify-write cycle is that the write portion of the latter does not generate an internal address transfer pulse.

3-13. FUNCTIONAL ELEMENTS.

The memory employs core matrices, integrated modules, and special solid state circuits to form the functional elements shown in Figure 3-3, which is a functional block diagram. The following paragraphs give a brief description of the functional elements.

3-14. TIMING AND CONTROL CIRCUITS. The timing and control circuits consist of gating circuits, flip-flops and one-shot multivibrators. These are employed to generate a series of timing signals which provide for an orderly progression through the steps involved in the mode of operation determined by the command input signals. Included in these timing signals are address strobe, data strobe, read and write timing, sense strobe and inhibit timing. Circuits are also provided to generate such output signals as Data Available, Memory Busy and End-of-Cycle.

3-15. ADDRESS REGISTER. The address register is composed of one flip-flop for each bit of the address word. A 4096 word memory requires 12 address register flip-flops. The address is temporarily stored in the flip-flops when the address strobe is applied.

3-16. ADDRESS DECODERS. Address decoders are binary-to-octal decoders to which the TRUE and FALSE outputs of three address register flip-flops are applied. For any three-bit binary segment, the decoder generates one TRUE and seven FALSE outputs. Four address decoders are used.

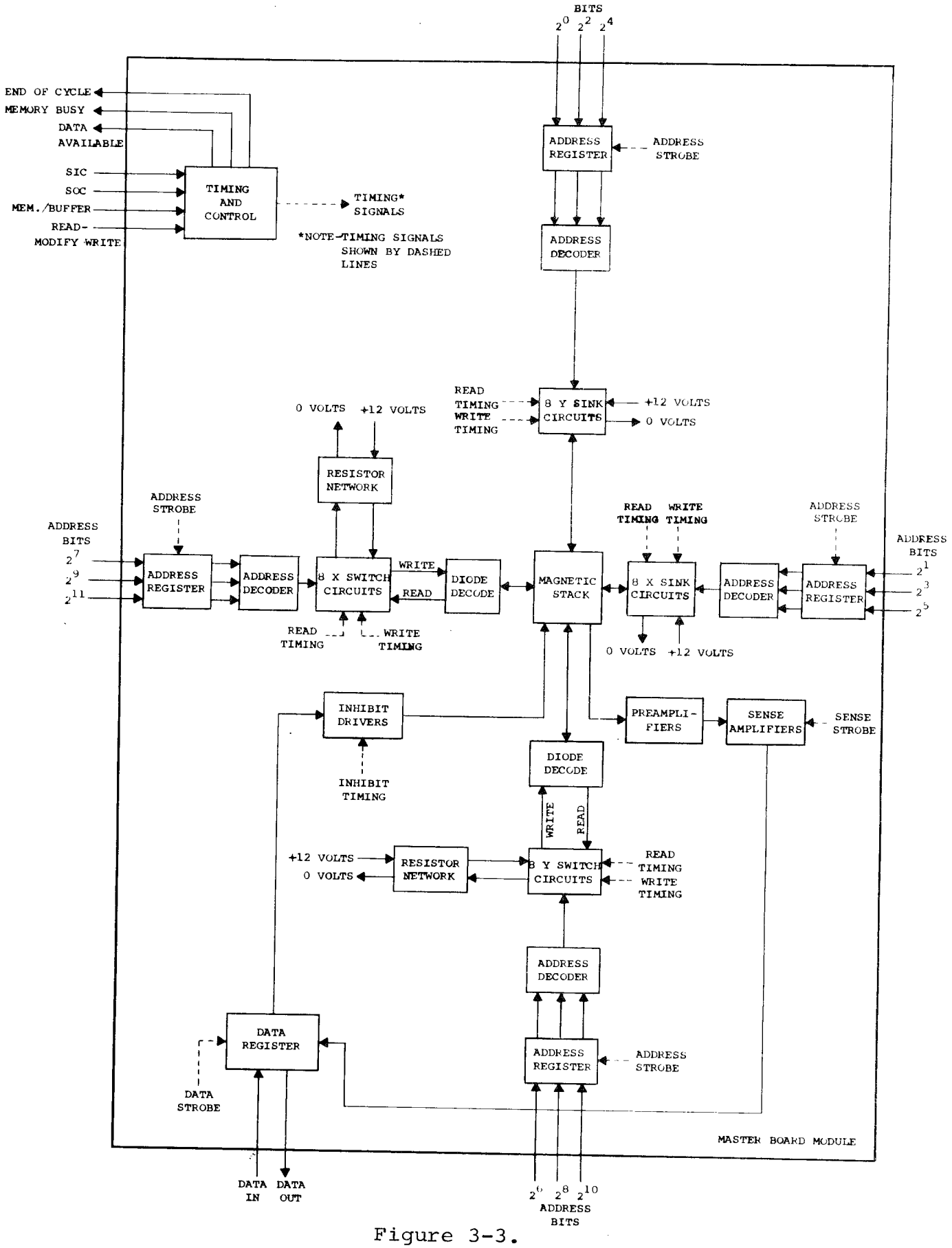


Figure 3-3.
Functional Block Diagram

3-17. SWITCH AND SINK CIRCUITS. These circuits are electronic switches, used to apply voltages to the X and Y drive lines of such a polarity as to produce read and write drive currents through them. In a 4096 word memory, there are eight X and eight Y switches, eight X and eight Y sinks. Each group of eight circuits is driven by one address decoder output. Each circuit is connected to eight drive lines.

3-18. DIODE DECODE. These diodes are used to steer the read and write drive currents through the proper X drive line and Y drive line, from the total of 64 X and 64 Y drive lines for a maximum address of 4096 words. They are inserted between the switch circuits and the drive lines.

3-19. INHIBIT DRIVERS. Each inhibit driver receives an enabling or disabling signal from an associated data register flip-flop and an inhibit timing signal. The writing or restoring of ONEs and ZEROs in core storage is controlled by the inhibit drivers in response to these signals.

3-20. PREAMPLIFIERS. Each preamplifier receives core turnover signals from the sense winding of one core matrix. Common mode signals are rejected. Core turnover signals are amplified and applied to sense amplifiers.

3-21. SENSE AMPLIFIERS. Each sense amplifier receives a core turnover signal from a preamplifier. In a read-restore or a buffer-unload cycle, at the time which provides maximum discrimination between the readout of a ZERO and of a ONE, the sense amplifier receives a sense strobe. This applies the input to the corresponding data register flip-flop.

3-22. DATA REGISTER. The data register is composed of one flip-flop for each data bit. The flip-flop temporarily stores a data bit transmitted from the external source or read out of core storage. The data strobe gates the data into the data register from the external source.

3-23. POWER SUPPLY. One solid state power supply furnishes all the DC voltages and currents required for the system. Control circuits are provided for shutdown in the event of over-voltage, over-current or for AC Fail signal generation in case of AC power failure.

3-24. FUNCTIONAL THEORY OF OPERATION.

3-25. USE OF LOGIC DIAGRAMS. In the pages which follow, logic diagrams are employed to illustrate operation of all system components. Normally, the system employs negative TRUE logic, with a nominal 0

volts (low level) representing ONE, and nominal +4 volts (high level) representing ZERO. However, employment of a small circle ("bubble") at an input or the output of a gate to indicate the most negative of two voltage levels permits shifting from negative to positive TRUE logic, without confusion. Basically, the logic symbols conform to MIL-STD-806B.

As an example of the use of the logic diagrams to indicate signal flow, turn to Dwg. No. 3225210, Address to Switch "X" Schematic It is evident that micrologic unit IC1 is composed of two AND gate-inverters. If a low level (ONE) signal is applied to input 1, the gate is enabled when the low-level Address Strobe signal is applied to input 2, producing a high level output voltage at lead 7. However, if a high level (ZERO) is applied to input 1, output 7 is a low level. This is applied to input 5, and the Address Strobe at lead 3 produces a high level output at lead 6. Whether the address input be ONE or ZERO, one AND gate is enabled and the other is disabled.

Proceeding to micrologic unit IC4, it is evident that the two OR gate-inverters form a conventional flip-flop. A high level voltage to lead 3 produces a low level voltage at lead 4. With this voltage also applied to lead 6, output 9 is high level, since this OR gate is disabled. Application of a high level voltage to lead 8 produces a low level signal from lead 9, and a high level signal from lead 4. The two OR gate-inverters in micrologic unit IC11 serve as conventional inverters, since each is driven by a single input.

3-26. INTEGRATED CIRCUITS. Two types of subminiature, encapsulated, integrated circuits are used in the system. Both are logically represented in the drawing referenced above. The schematic and assembly of Micrologic Dual Three-Input Gate, Part No. 586-008 (IC4) is presented on drawing PCD6040. The schematic and assembly of Micrologic Dual Two-Input Gate, Part No. 586-007 (IC1) is presented on drawing PCD6039. The leads for these micrologic circuits are soldered to the mother board. Various logical configurations are achieved by permanently jumpering between leads at the mother board. When Part No. 586-008 is used, lead 10 is always tied to +4 volts DC, and lead 5 is tied to ground. When Part No. 586-007 is used, lead 8 is always tied to +4 volts DC, and lead 4 is tied to ground.

3-27. ADDRESS SELECTION. (See Dwg. Nos. 3225210, 3225213, 3225216 and 3225219, Address to Switch/Sink Schematics.)

The number of binary bits comprising the address word is determined by the data word capacity of the system; a 4096-word memory requires a 12-bit address word. Single-ended address words are applied

to the memory register flip-flops, with a ONE represented by nominal +4 volts, and a ZERO represented by nominal 0 volts.

The address register flip-flops are capable of jam transfer. This means that with the application of the negative-going (+1.5 to 0 volts) address strobe to the input AND gates, the current address is stored in the flip-flops, regardless of their previous state. In the set (ONE) state, the TRUE output of a flip-flop is 0 volts and the FALSE output is +1.5 volts; in the reset (ZERO) state, polarity of the two outputs is reversed.

TRUE and FALSE outputs of three address registers are connected to eight AND gates in such a manner that a three-bit address segment is decoded to an octal equivalent. For any combination of the three bits, one gate is enabled, producing a +1.5 volt output, while the remaining seven gates are disabled, with their outputs at 0 volts.

Since the components making up the circuit are identical, the designation of a switch circuit or a sink circuit is functional only. In the overall system picture (Figure 3-3), a switch circuit drives the diode decode circuit, whereas a sink circuit is located at the opposite end of the drive lines. Using conventional current flow, the read current flows from a switch circuit through the selected drive line and into the sink circuit, while the write current flows from a sink circuit through the selected drive line and into the switch circuit.

To accomplish this reversal of current flow, a circuit is so designed that when an enabling inverted high level signal is received from an enabled decoder, the switch output is driven to either +12 volts or 0 volts. As shown in the schematics, a read timing pulse provides 0 volts at the switch circuit end and +12 volts at the sink circuit end of the drive line. A write timing pulse provides +12 volts at the switch circuit end and 0 volts at the sink circuit end of the drive line.

3-28. DRIVE LINE OPERATION. (See Dwg. No. 3225222, RF Drive System Schematic.)

As indicated in the schematic, the address is decoded and the switch and sink circuits are enabled, to select and steer drive currents through one of 64 X drive lines, and one of 64 Y drive lines, in a 4096 word memory. In a full memory cycle, the read drive current occurs during the first half of the cycle, and the write drive current follows during the last half of the cycle.

In a 4096-word memory, AR11, AR9 and AR7 address bits are decoded to select one of eight X drive circuits; AR5, AR3 and AR1 are decoded to select one of eight X sink circuits. Similarly, AR10, AR8 and AR6 are decoded to select one of eight Y drive circuits; AR4, AR2 and AR0 are decoded to select one of eight Y sink circuits. After selection, the four circuits are enabled, first by a read timing signal, and then by a write timing signal.

Shown on the schematic are the 16 diode decode circuits, which are used to steer the outputs of the switch circuits to the proper X and Y drive lines. Figure 3-4 is a simplified schematic, showing a typical X switch circuit, representative diode decoders, the selected drive line and a typical X sink circuit. Operation of the Y switch and sink circuits and diode decode circuits is identical to that shown.

Each X switch is connected to eight drive lines (two shown) so that the eight X switch circuits are connected to a total of 64 X drive lines. Similarly, each X sink circuit is connected to eight drive lines so that the eight X sink circuits are connected to 64 X drive lines. Diode decoding steers current through the proper line.

In the quiescent state, Q8, Q9, Q10 and Q11 are cut off and present open circuits to the drive lines. CR7, CR8, CR9 and CR10 are typical of the 16 decode diodes with which a switch circuit is connected. With +12 volts applied through R3, and +6 volts applied through R5, CR7 and CR8 are back-biased. Similarly, with R4 tied to ground, CR9 and CR10 are back-biased.

Enabling of the address decoder short circuits to ground the voltage applied to the emitters of Q1, Q2, Q6 and Q7. A positive-going read timing pulse drives Q2 to saturation, and the voltage through T1 drives Q9 to saturation. At the same time, the read timing pulse drives Q6 to saturation, and the voltage through T3 drives Q10 to saturation. With +12 volts at Q10 emitter, CR7 is forward-biased and read current flows through the 64 cores on the drive line. The current flows to ground through Q9 and R2. CR8 is back-biased, and the status of CR9 and CR10 remains unchanged.

Q3, Q4 and Q4 and their associated circuits, comprise a turn-off switch, employed to realize a uniform turn-off time for the drive modules. The output of the turn-off switch circuit is diode-coupled to the transformer primaries. CR3 and CR4 represent diode networks which hold the output at +9.3 volts, but permit a positive swing to +13.4 volts upon application of a positive signal to C1.

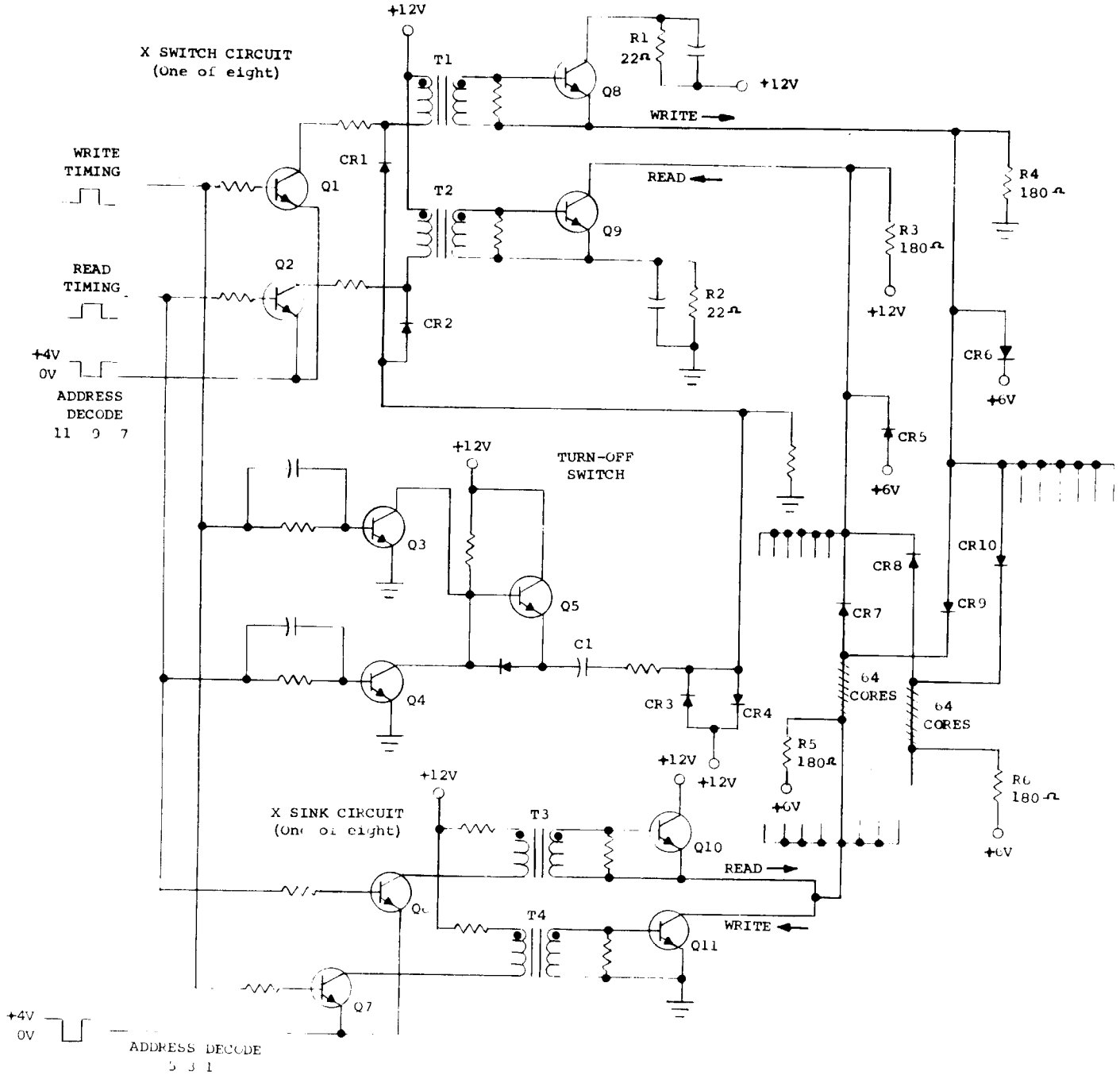


Figure 3-4.
X Drive Line Operation, Simplified Schematic

With the collapse of the read or write timing signal, the switch and sink input transistors are cut off. Additionally, either Q3 or Q4 is cut off. This drives Q5 to saturation, and applies a positive-going signal to C1. With the output rising to +13.4 volts, the transformer-coupling diode is forward-biased, and the current through the transformer primary is reversed. This immediately cuts off the switch transistor.

Continuing the description of drive line operation, application of a write timing signal drives Q1 to saturation, and this in turn drives Q8 to saturation. Similarly, Q6 and Q11 are driven to saturation. This places the collector of Q11 at 0 volts, with a positive potential of approximately +12 volts at the emitter of Q8. CR9 is forward-biased and write drive current flows through the 64 cores on the X drive line. CR10 remains back-biased, with CR7 and CR8 unaffected. Collapse of the write timing signal cuts off the write drive current, as explained in the preceding paragraph.

CR5 and CR6 are not normally employed as clamping diodes, but can operate to suppress transient voltages.

3-29. DATA CIRCUIT OPERATION. (See Dwg. No. 3225228, RF Data Channel Schematic.)

The schematic shows the circuits which temporarily store data, write data into the core storage, and read data out of the core storage. These circuits include (for each bit of the data word) a preamplifier, sense amplifier, data register flip-flop, data interface, and inhibit driver.

The data register flip-flop is identical with an address register flip-flop, and has the same jam transfer characteristics when enabled by a data strobe signal. The data word is a nominal +1.5 volt for ONE and 0 volts for ZERO. In the set (ONE) state, the TRUE output of the flip-flop is 0 volts and the FALSE output is +1.5 volts; in the reset (ZERO) state, polarity of the outputs is reversed.

The preamplifier consists of direct-coupled differential amplifier 1Q1 with 1Q2 controlling amplifier current. The two inputs are connected to each end of the sense line which threads the cores of a mat. V_S is adjusted to -4 volts with a potentiometer on the power supply printed circuit card. 1Q2 supplies constant current to 1Q1, causing the amplifier to suppress common mode noise.

The sense amplifier circuit, consisting of Q1 through Q6 is a limited class A amplifier which amplifies and rectifies core turnover

signals received from the preamplifier, when the rectifiers are enabled by a sense strobe pulse. The output of the preamplifier is direct-coupled to inverters 1Q1 and their outputs are direct-coupled to Q2 and Q3. Q6 provides a biasing threshold voltage for the rectifiers (Q4 and Q5), having been driven by clipping voltage V_{CL}.

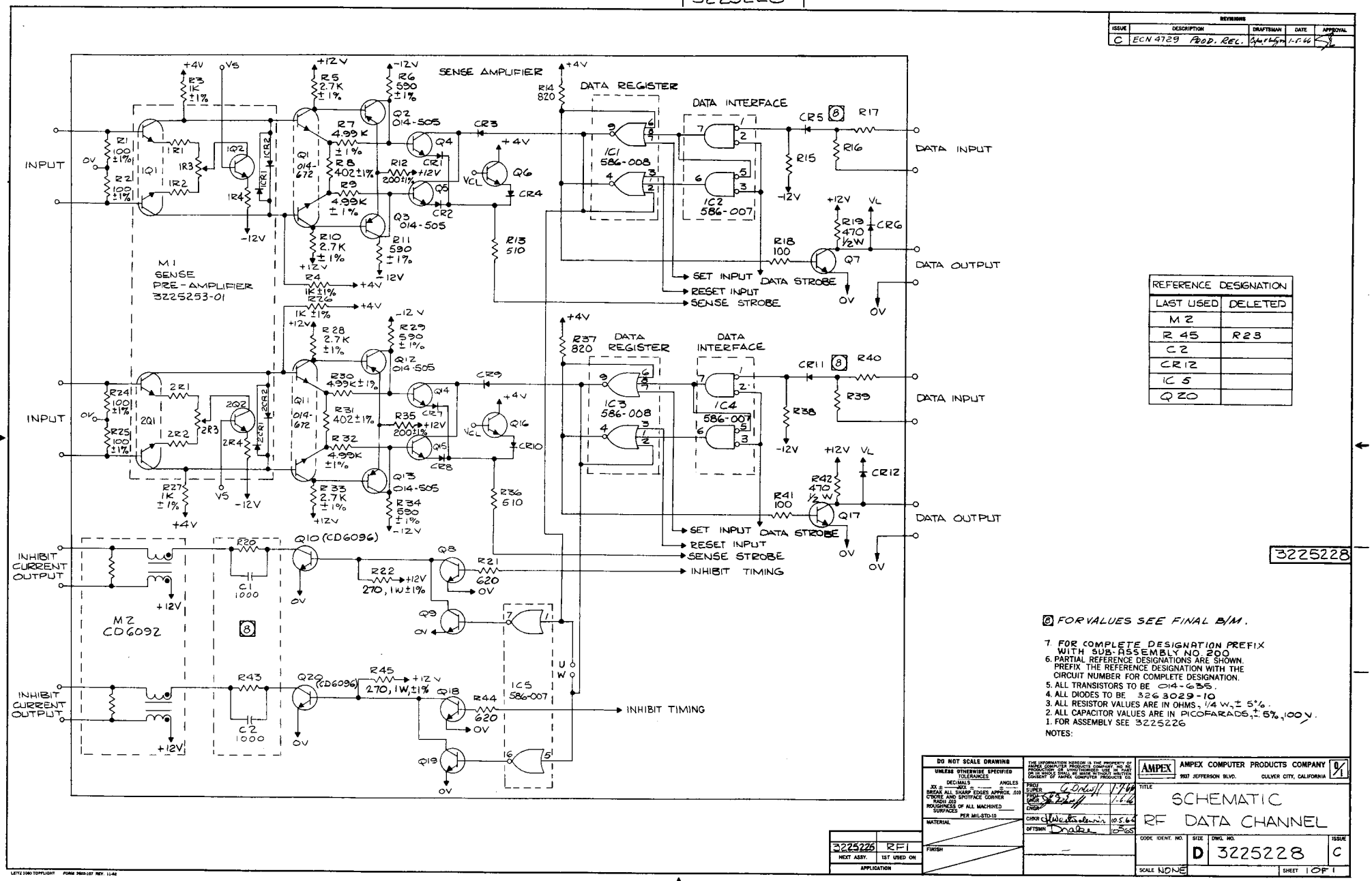
Application of an amplified core turnover signal to the base of Q4 or Q5, and simultaneous application of a negative-going (+4 to -12 volts) sense strobe to their emitters causes one of the transistors to conduct, and applies a negative-going signal to the reset input of the data register flip-flop. This sets the flip-flop to the ONE state. A positive-going reset input signal will reset the flip-flop to the ZERO state.

Q7 is a line driver which is driven by the FALSE output of the data register flip-flop. If the flip-flop is in the ONE state, the transistor is driven to saturation, producing 0 volts on the data output line. If the flip-flop is in the ZERO state, Q7 is cut off, and CR6 clamps the output voltage to V_L. This voltage can be varied between +2 and +6 volts with a potentiometer on the power supply printed circuit board.

The inhibit driver is enabled whenever writing ZERO (inhibiting the X and Y drive currents in a selected core from driving it to the ONE state) is necessary. A typical inhibit driver is composed of Q8, Q9 and Q10, with associated circuits. In the quiescent state, Q8 and Q9 are conducting at saturation, and Q10 is cut off. This presents an open circuit to the +12 volts applied to the inhibit winding, preventing the flow of inhibit current.

When the data register is in the reset (ZERO) state, the +4 volt TRUE output is inverted and applied to the base of Q9, biasing the transistor to cutoff. Application of a negative-going (+4 to 0 volts) inhibit timing signal to the base of Q8 likewise cuts off this transistor. It is only when Q8 and Q9 are both cut off that Q10 is driven to saturation, permitting current to flow through the inhibit winding for the duration of the inhibit timing signal. A balun transformer symmetrically drives both ends of the inhibit winding, improving common mode noise rejection in the winding.

In the read portion of a read-restore cycle, read current drives the cores to ZERO, and where there is a core turnover it is applied to the preamplifier and sense amplifier. The sense amplifier is strobed and the data register is set to the ONE state. The line driver (Q7) applies the ONE to the data output line. In the restore portion of



REFERENCE DESIGNATION	
LAST USED	DELETED
M 2	
R 45	R 23
C 2	
CR 12	
IC 5	
Q 20	

3225228

[8] FOR VALUES SEE FINAL B/M.

7. FOR COMPLETE DESIGNATION PREFIX WITH SUB-ASSEMBLY NO. 200
6. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX THE REFERENCE DESIGNATION WITH THE CIRCUIT NUMBER FOR COMPLETE DESIGNATION.
5. ALL TRANSISTORS TO BE 014-635.
4. ALL DIODES TO BE 326 3029-10.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4 W, ± 5%.
2. ALL CAPACITOR VALUES ARE IN PICOFARADS, ± 5%, 100 V.
1. FOR ASSEMBLY SEE 3225226

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the cycle, if the data register flip-flop is in the ONE state, the inhibit driver (Q10) is disabled, and the write current switches the core back to the ONE state.

In the clear portion of a clear-write cycle, read current drives the cores to ZERO, but although core turnover signals are applied to preamplifier and sense circuits, no sense strobe is generated and the core turnover signal is not applied to the data register flip-flops. A data strobe inserts the data word into the data register flip-flops.

If the data bit is ONE, the inhibit driver is disabled as explained above. However, if the data bit is ZERO, the data register flip-flop is in the reset state. Application of an inhibit timing pulse enables the inhibit driver, producing the inhibit current which prevents the core from switching to the ONE state when the X and Y write currents are applied.

3-30. RF TIMING. (See Dwg. No. 3225225, RF Timing Schematic; also, Waveforms in Section V.)

The RF timing circuits receive control inputs from the external source, determining the modes of operation. Circuits then generate timing pulses for internal and external control. Duration of the timing signals is controlled by one-shot multivibrators, with the length of time established by a fixed RC time constant, or varied with a potentiometer. All timing signals are factory-adjusted and normally do not require any readjustment in the field, with the exception of the data strobe timing.

One-shot multivibrators are also employed to introduce time delays. In this case, it is the trailing edge of the positive-going output signal which triggers a succeeding transistor circuit. The delay introduced is determined by the duration of the multivibrator output signal. Typical of such applications are the Sense Delay and Write Current Delay multivibrators.

It will be noted on the drawing that there are numerous AND gate-inverters and OR gate-inverters, each designated by a number. These are integrated circuits, referenced in paragraph 3-26. The numbers can be used to physically locate the integrated circuits on the assembly drawing, and the number presentation indicates the type of circuit. Plain numbers represent Type 586-007; encircled numbers indicate Type 586-008. For example, on the drawing, OR gate-inverter 1 is a Type 586-007 integrated circuit, whereas OR gate-inverter (22) is a Type 586-008 integrated circuit.

Table 3-1 is a truth table which illustrates the RF control logic. There are three control inputs. The M/B (memory/buffer) control determines whether the system will operate as a memory or as a buffer. When the RMW (read-modify-write) control is TRUE (ONE), the system, operating in the memory mode, performs a read-modify-write operation. The initiate signal must always be either SOC (start output cycle), or SIC (start input cycle). Seven internal control and three output control signals are characteristic of normal system operation. However, all control signals are not TRUE for every mode. For example, DATA STROBE is ZERO for both the read and write portions of a read-restore memory cycle, and SENSE STROBE is ZERO for read and write portions of a clear-write memory cycle.

The following logic equations explain the generation of the principal control signals.

$$\overline{F} = M/B + RMW$$

$$F = \overline{\overline{F}} = \overline{M/B + RMW}$$

$$I = SIC + SOC$$

$$READ = I \cdot F + SOC \cdot \overline{F} = SIC \cdot F + SOC$$

$$WRITE = END\ OF\ READ \cdot F + SIC \cdot \overline{F}$$

$$DATA\ CLEAR = SOC$$

$$ADDRESS\ STROBE = I \cdot \overline{RMW} + SOC \cdot RMW = SIC\ \overline{RMW} + SOC$$

$$DATA\ STROBE = SIC \cdot F\ (delayed) + SIC \cdot \overline{F}$$

$$SENSE\ STROBE = SOC\ (delayed)$$

$$MEMORY\ BUSY = I$$

$$\overline{MEMORY\ BUSY} = (END\ OF\ WRITE_{mem} \cdot F + END\ OF\ WRITE_{buff} \cdot \overline{F} + END\ OF\ READ_{buff} \cdot \overline{F} + CLEAR) \cdot \overline{AC\ FAILURE}$$

The schematic illustrates how gating circuits are employed to implement the above equations and generate the required control pulses. Bus B represents M/B + RMW ($\overline{F}$), Bus C is $\overline{RMW}$, and Bus D is $\overline{M/B + RMW}$ (F). SIC and SOC are gated with the TRUE output of the Memory Busy flip-flop, and applied to SIC 1, SIC 2, SOC 1, and SOC 2. This can only occur when the flip-flop is in the reset state (End-of-Cycle). During a cycle, with the flip-flop in the set state, AND gates 2 are disabled, preventing the initiation of a new cycle while one is currently in progress.

TABLE 3-1.
RF CONTROL LOGIC

		MEMORY CYCLE				BUFFER CYCLE		READ-MODIFY WRITE	
		READ-RESTORE		CLEAR-WRITE					
		READ	WRITE	READ	WRITE	READ	WRITE	READ	WRITE
Control Inputs	Initiate Signal	SOC	0	SIC	0	SOC	SIC	SOC	SIC
	RMW Control	0	0	0	0	0	0	1	1
	Mem./Buffer Control	0	0	0	0	1	1	0	0
	$\overline{F} = M/B + RMW$	F	F	F	F	$\overline{F}$	$\overline{F}$	$\overline{F}$	$\overline{F}$
Internal Control	Address Strobe	1	0	1	0	1	1	1	0
	Data Strobe	0	0	1	0	0	1	0	1
	Sense Strobe	1	0	0	0	1	0	1	0
	Read Current	1	0	1	0	1	0	1	0
	Write Current	0	1	0	1	0	1	0	1
	Inhibit Current	0	1	0	1	0	1	0	1
	Data Clear	1	0	0	0	1	0	1	0
Output Control	Memory Busy	1	1	1	1	1	1	1	1
	End-of-Cycle	0	1	0	1	1	1	1	1
	Data Available	1	0	0	0	1	0	1	0

The Memory Busy flip-flop is set by receipt of a SIC or SOC signal, and reset as shown in $\overline{\text{MEMORY BUSY}}$ equations above. When power is first turned on, the Clear flip-flop momentarily goes to the set state, and its FALSE output will reset the Memory Busy flip-flop, if it is not already in that state. An AC Failure signal inhibits the resetting of the Memory Busy flip-flop. Initiating a new cycle is prevented, since SIC or SOC is gated with the flip-flop output. Refer to paragraph 2.4 of the Product Specification, Section II, for a description of nondestructive power shutdown.

3-31. READ TIMING. The Read Timing signal is initiated by ORing SIC and F, or SOC in OR gate 17. The enabled output is a negative-going signal which is current-amplified and drives a one-shot multivibrator. Duration of the multivibrator output is determined by setting potentiometer R37. The inverted signal is applied to AND gate 19, together with the write current signal which should be OFF (low). This is a safety feature, preventing simultaneous occurrence of read and write timing pulses. The positive-going output of AND gate 19 is applied to Q27 and Q28, driving Q27 to saturation and cutting off Q28. This produces a read timing signal which is positive-going (0 to +4 volts)

as long as the multivibrator is enabled. When SIC/SOC = T_0, nominal initial time of this signal is T_0 + 250 nsec.

3-32. SENSE STROBE AND DATA AVAILABLE. The Sense Strobe is tapped off the Read Timing input. However, Q11 and Q12 serve as an AND gate, which can be enabled only when the Read/Write flip-flop is in the set state. This flip-flop is set by SOC and reset by SIC. With the flip-flop reset, Q11 is driven to saturation, inhibiting any output from the sense delay. This prevents a Sense Strobe during the clear portion of a clear-write memory cycle. A one-shot multivibrator introduces a sense delay before application of the tapped Read Timing input signal to the AND gate. Data Available is initiated at the same time as Sense Strobe, since it is tapped off the sense strobe output. Sense Strobe is a negative-going (+4 to -12 volts) signal, and Data Available is a negative-going (V_L to 0 volts) signal, or can be positive-going if the output terminals are so connected to the external equipment. The nominal initial time of Sense Strobe is T_0 + 450 nsec and of Data Available is T_0 + 600 nsec.

3-33. WRITE TIMING. The Write Timing signal is initiated by ORing END OF READ and F, or SIC and $\overline{F}$ at C14 to cut off Q16. A write current delay is introduced by a fixed one-shot multivibrator, and duration of the timing signal is controlled with a variable one-shot multivibrator. Coincidence with a Read Timing signal is inhibited by AND gate 28. The Write Timing signal is positive-going (0 to +4 volts), and nominal initial time is T_0 + 1050 nsec.

3-34. INHIBIT TIMING. Inhibit Timing is initiated coincidentally with the Write Timing signal. However, due to absence of a current delay circuit, the Inhibit Timing (+4 to 0 volts) signal is applied to the system prior to the Write Timing signal. Nominal initial time is T_0 + 800 nsec.

3-35. ADDRESS STROBE. The Address Strobe is initiated by ORing SIC and $\overline{RMW}$, or SOC in OR gate 22. This gating inhibits the Address Strobe during the Write portion of a Read-Modify-Write operation, ensuring that modified data will be written at the original address. The Address Strobe is a negative-going signal. Nominal initial time is T_0 + 25 nsec. Circuitry is also provided for optional control of the address strobe, upon application of a positive-going signal to the External Address Transfer circuit.

3-36. DATA STROBE. The Data Strobe is initiated by ORing SIC and $\overline{F}$, or SIC and F after a multivibrator delay (Data Strobe Delay) in OR gate 25. This provides Data Strobe turn-on time adjustable between T_0 +250-700 nsec (nominal T_0 + 350 nsec) during a clear-write memory cycle, or a nominal initial time of T_0 + 50 nsec during a buffer or RMW cycle. Parallel Data Strobe outputs composed of negative-going signals are generated. Circuitry is also provided for external control of the Data Strobe signals, upon application to the Data External Transfer of a positive-going pulse.

3-37. END OF CYCLE. When the Memory Busy flip-flop is in the set state, it produces a Memory Busy output signal. When the flip-flop enters the reset state, the Memory Busy signal is cut off and an End of Cycle signal is generated. This signal continues until application of SIC or SOC initiates a new cycle. In a Memory Cycle, the nominal initial time is T_0 + 1800 nsec. In a Read-Modify-Write cycle, the End of Cycle signal is generated at the end of the Read portion and again at the end of the Write portion of the cycle. The signal is negative-going (V_L to 0 volts).

3-38. DATA REGISTER RESET. With the Memory Busy flip-flop reset, application of the SOC signal to the system results in generating a positive-going Data Register Reset signal. Nominal initial time is T_0 + 50 nsec.

3-39. RF-1 POWER SUPPLY. (See Dwg. No. 3225249, Power Supply.)

The RF-1 power supply is composed of three full-wave rectifiers (+12, +4 and -12 volts) driven by 115/230 volts, 48-420 cps AC, from which are derived seven regulated DC voltages required to operate the system. These voltages are +12V, +6V, +4V, -12V, V_L (+2 to +6V), V_L (nominal +5.5V) and V_S (nominal -4V).

The major components, such as the power transformer, rectifiers, relay, and filter capacitors are mounted on the chassis. Also included is a cooling fan which operates when power is applied to the system and the circuit breaker is closed. The circuit breaker, along with ON and OFF pushbutton switches, and ON and OFF lights, is mounted on the front panel. The voltage regulator circuits are mounted on a printed circuit card, which plugs into the chassis.

The voltage regulator circuits are conventional, in that a difference amplifier is employed to sense any voltage error. This is

transmitted by emitter followers to one or more transistors serving as series regulators, and the error voltage is applied to the base or bases. This prescribes the voltage drop across the series regulator and restores the output voltage to its proper value. Each voltage regulator circuit is equipped with a potentiometer which is adjusted to produce the required output voltage.

The power supply is provided with circuits, including a relay, which will energize or deenergize the rectifier circuits in a sequence which ensures against the loss of information in the system during normal shutdown or turn on. This involves applying the +12 volt drive voltage to the system last during turn on, and removing it first during turn off, with no transition time in either instance.

With AC power applied to J1, and the circuit breaker closed, the DC OFF lamp glows. Momentarily depressing the DC ON switch applies AC power to the primary of the power transformer. This immediately energizes the -12 volt supply. The relay is still deenergized, and the -12 volts is applied to the base of Q2 through contacts 5-6. This provides an operating bias for the +12 volt series regulators Q1-Q6, and produces a +12 volt output to the inhibit and logic circuits. Operation of the +12 volt supply provides drive voltage for Q10, and the +4 volt series regulators Q8-Q9 are driven to conduction. This provides a bias for Q1 on the printed circuit card, driving it to saturation. With the supplying of a ground for K1, the relay is enabled. This latches contacts 11-9, applying AC power continuously to the transformer, and opens 11-8 to turn off the DC OFF light. The DC ON light, in parallel with K1, is now lighted. Contact 5-6 is open, but is no longer required as long as all power supplies are operating. Closing of contacts 1-3 provides a +12 volt X/Y Driver output to the system.

Depressing the DC OFF switch deenergizes the relay, immediately cutting off the +12 volt X/Y Driver output by opening contacts 1-3. The opening of contacts 11-8 removes AC power from the power transformer primary, and the +12 and -12 volt outputs decay as their filter capacitors discharge through bleeders. It may be seen that the X/Y Drivers are the last to receive power during turn-on, and the first to have power removed during turn-off.

The +12, +4, +6 and V_L regulators are tied to an over-voltage sensing circuit composed of CR1 through CR4, VR1 and associated resistors. Should the +12, +4, +6 or V_L supply lose regulation, i.e. the output voltage becomes exceedingly high, possibly damaging memory

SECTION IV
INSTALLATION

4-1. UNPACKING AND HANDLING.

The RF-1 Magnetic Core Memory is shipped in a packing case provided with ample padding to prevent damage under normal handling conditions. When the optional power supply is also ordered, the two are shipped as an integral unit ready for panel mounting.

Upon receipt, carefully unpack the equipment, examine it and immediately report to the shipping company any damage noted.

4-2. INSTALLATION INSTRUCTIONS.

When mounting the memory in a rack, a minimum clearance of one-half inch should be allowed between the top of the unit and the bottom of an adjacent unit. This is necessary to permit the free flow of cooling air through the unit.

4-3. INPUT-OUTPUT CABLING.

4-4. DC POWER. When the optional power supply is part of the customer order, the power requirements are 115-230 volt 50-60 cps AC. DC power requirements of the memory are satisfied by a cable connecting TB1 of the power supply to connectors J3 and J4. (See Dwg. No. 3225205.) If the power supply is not part of the order, the customer must connect the required DC voltages to the proper pins on the connectors.

4-5. INTERFACE CONNECTIONS. Tables 4-1 and 4-2 list the signal and command interface connections to J5 and J6, which are 75-pin Burndy connectors, mounted on the rear panel of the power supply. Connectors J5 and J6 are shown on Dwg. No. 3225120, Mechanical Assembly, and Dwg. No. 3225255, Cable Harness, Interface and Power Distribution Assembly.

TABLE 4-1.
ADDRESS, CONTROL AND DATA INPUT CONNECTOR J5

CONN.	TERM.	SIGNAL TYPE	CONN.	TERM.	SIGNAL TYPE
J5	(35 38	Data 0 In	J5	(3 7	Data 8 In
	(41 44	Data 1 In		(11 14	Data 9 In
	(47 50	Data 2 In		(17 21	Data 10 In
	(53 56	Data 3 In		(24 27	Data 11 In
	(23 26	SOC (Start Output Cycle)		(73 76	Address 11 In
	(16 20	SIC (Start Input Cycle)		(58 62	Address 9 In
	(59 63	Data 4 In		(46 49	Address 7 In
	(66 71	Data 5 In		(30 33	Data 12 In
	(1 4	Address 0 In		(36 39	Data 13 In
	(15 18	Address 2 In		(8 12	Address 1 In
	(28 31	Address 4 In		(22 25	Address 3 In
	(74 77	Data 6 In		(34 37	Address 5 In
J5	(80 79	Data 7 In	J5	(42 45	Data 14 In

(Indicates twisted pair with signal on white wire, and grey wire at signal ground.

TABLE 4-1.
ADDRESS, CONTROL AND DATA INPUT CONNECTOR J5 (Continued)

CONN.	TERM.	SIGNAL TYPE	CONN.	TERM.	SIGNAL TYPE
J5 ↑	(48 51	Data 15 In	J5 ↑	(54 57	Data 16 In
	(65 70	Address 10 In		(60 64	Data 17 In
100	(52 55	Address 8 In	220	(67 72	M/B (Logic 1)
22 ↓ J5	(40 43	Address 6 In	210 ↓ J5	(2 5	RMW (Logic 2)

(Indicates twisted pair with signal on white wire, and grey wire at signal ground.

TABLE 4-2.
DATA AND SIGNAL OUTPUT CONNECTOR J6

CONN.	TERM.	SIGNAL TYPE	CONN.	TERM.	SIGNAL TYPE
J6	(52 55	Data 0 Out	J6	(66 71	Data 14 Out
	(58 62	Data 1 Out		(74 77	Data 15 Out
	(65 70	Data 2 Out		(80 79	Data 16 Out
	(73 76	Data 3 Out		(3 7	Data 17 Out
	(2 5	Data 4 Out		(54 57	End of Cycle
	(10 13	Data 5 Out		(60 64	Data Available
	(16 20	Data 6 Out		(67 72	Memory Busy
	(23 26	Data 7 Out		(36 39	AC Failure
	(29 32	Data 8 Out		(30 33	Ext. Data Reg. Reset
	(35 38	Data 9 Out		(48 51	Ext. Data Transfer
	(41 44	Data 10 Out		(42 45	Ext. Address Transfer
J6	(47 50	Data 11 Out		(1 4	Ext. Address Set
			J6	(8 12	Ext. Address Reset

(Indicates twisted pair with signal on white wire, grey wire at signal ground.

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

This section of the manual, covering the maintenance of the system, is divided into five primary categories. They include reference waveforms and timing, preventive maintenance (to be performed every three months), procedures for localizing trouble, component replacement procedures, and worst pattern checks.

Table 5-1 lists the test equipment required to service the memory.

TABLE 5-1.
TEST EQUIPMENT REQUIRED

ITEM	SPECIFICATION
Oscilloscope	Tektronix, Inc., Type 551, or equivalent
Dual-Trace Preamplifier	Tektronix, Inc., Type CA, or equivalent
Differential Preamplifier	Tektronix, Inc., Type G, or equivalent
Multimeter	Simpson, Type 260, or equivalent
Digital Voltmeter	Maximum reading accuracy: 0.01 volts input impedance: More than 1 megohm
Alligator Clips and Insulators	Clips: Mueller #30, or equivalent Insulators: Mueller #32, or equivalent
Extender Board	Ampex Part No. 3225285-01
Current Probe	Tektronix, Inc., Type P6016 or equivalent
Current Probe	Tektronix, Inc., Type 131 or equivalent

All clip leads and test probes used in testing and troubleshooting must be insulated to prevent accidental shorting of components.

CAUTION

Use care in handling test probes; shorting adjacent components may cause damage.

5-2. REFERENCE WAVEFORMS AND TIMING.

Table 5-2 presents reference waveforms and timing for the RF-1 Magnetic Core Memory.

It should be realized that the waveforms and timing for a specific system may vary slightly from those shown in the table, but the information contained therein should prove invaluable in troubleshooting the system. All timing shown in the waveforms results from memory mode operation.

Unless otherwise specified on a waveform, cycle initiate time (T0) is represented by the first vertical grid line.

When precise timing settings are required, it is advisable to follow the final timing adjustment procedures outlined in Table 5-3.

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING

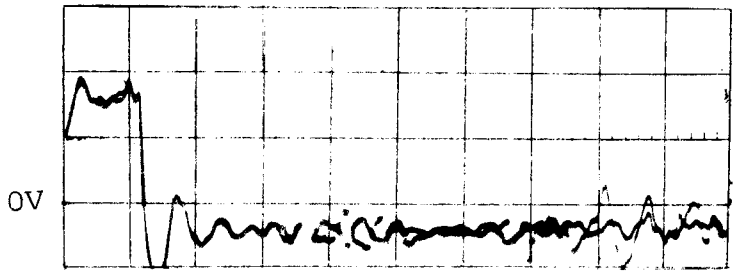
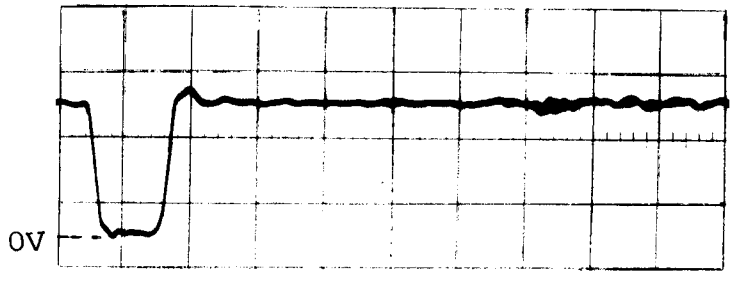
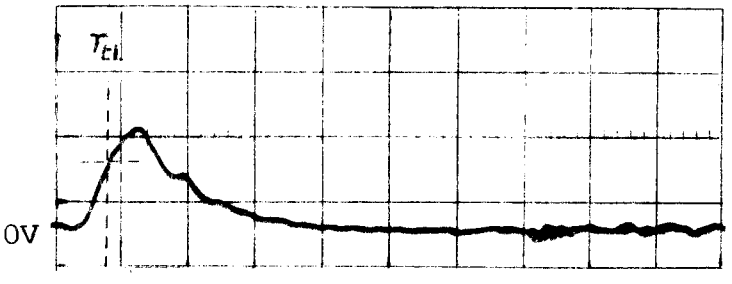
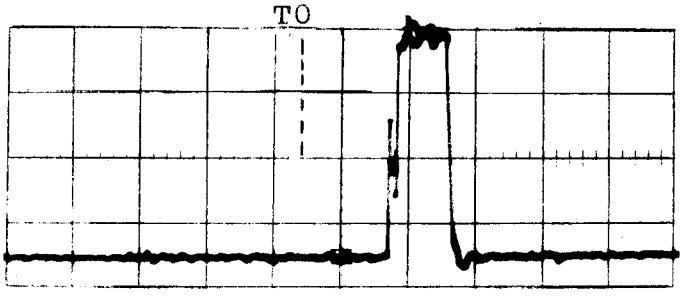
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
1	Memory Input	 200 nsec/cm; 1 v/cm	Start Cycle (SIC/SOC)
2	Pin 6 of IC3 or TP1 Pin 7 of IC4 or TP2 Dwg. No. 3225225	 100 nsec/cm; 0.5 v/cm	Internal SIC or SOC
3	Pin 8 of IC7 (SIC) Pin 7 of IC7 (SOC) Dwg. No. 3225225	 Approximate trigger time (T_{t1}) 100 nsec/cm; 0.5 v/cm	Delayed SIC/SOC triggers Memory Busy flip-flop
4	Pin J4-B25 or at R105 Dwg. No. 3225225	 400 nsec/cm; 1 v/cm	Data Available signal at memory output

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

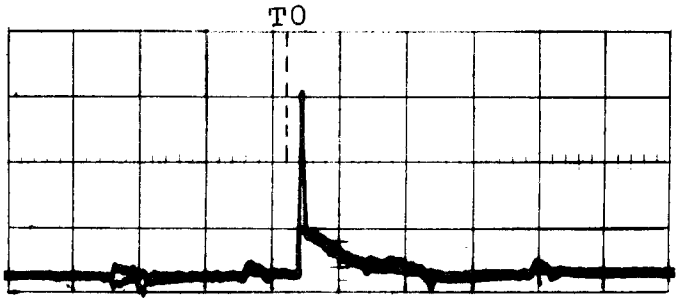
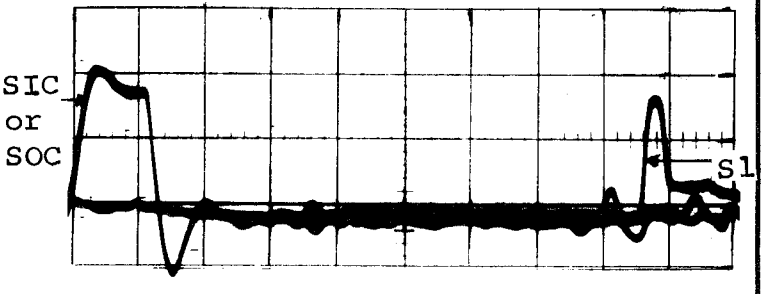
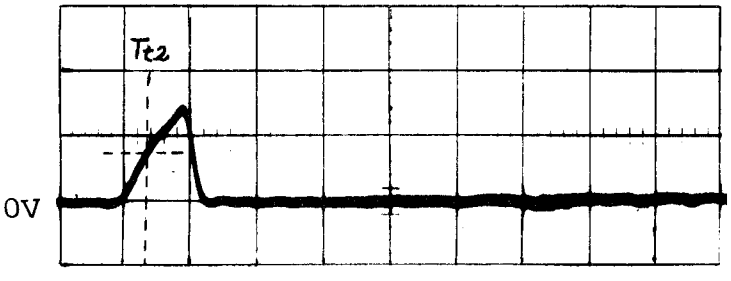
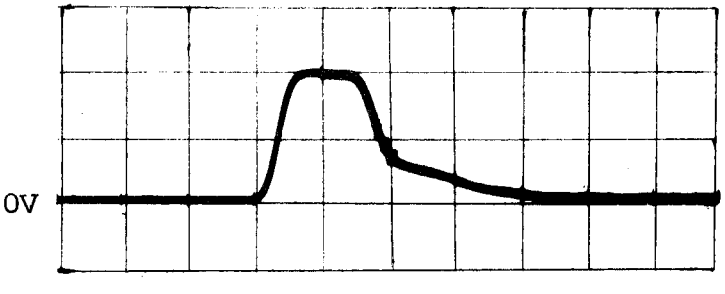
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
5	Q4 Collector Dwg. No. 3225225	 400 nsec/cm; 1 v/cm	Data flip-flop reset pulse, at beginning of read cycle
6	Pin 6 IC11 Dwg. No. 3225225	 200 nsec/cm; 1 v/cm	Time from initiate pulse to S1 signal which resets Memory Busy flip-flop at end of memory cycle
7	Pin 6 IC18 Dwg. No. 3225225	 Approximate time (T_{t2}) to trigger IC18 100 nsec/cm; 1 v/cm	Waveform in delay circuit to provide delay for address decoding
8	R32 Dwg. No. 3225225	 40 nsec/cm; 2 v/cm	Trigger pulse to initiate read current

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

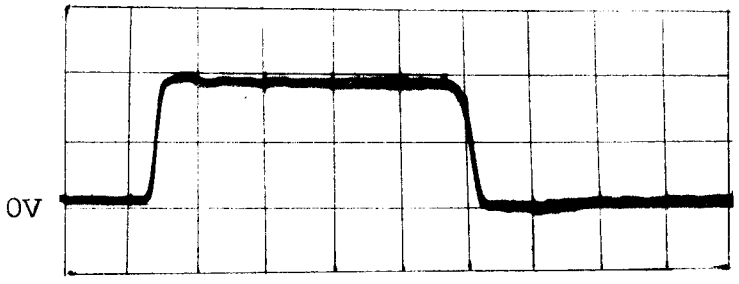
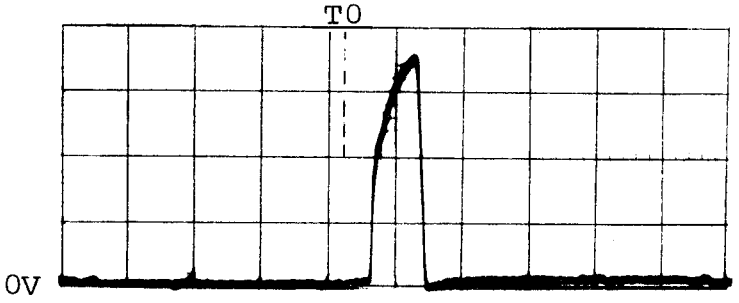
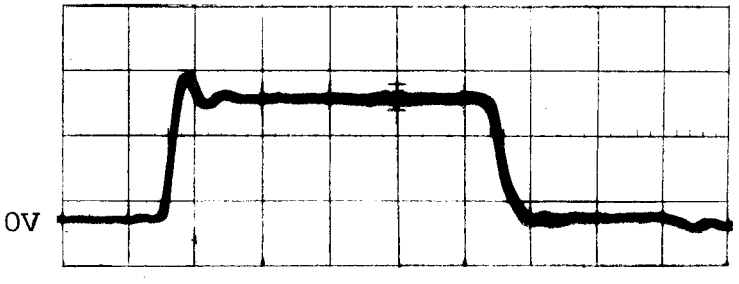
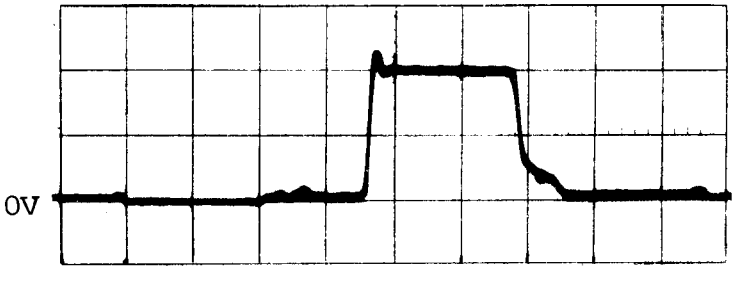
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
9	Pin 1 of IC19 Dwg. No. 3225225	 100 nsec/cm; 1 v/cm	Read Current Output
10	C11 Input Dwg. No. 3225225	 400 nsec/cm; 1 v/cm	Sense Delay Output
11	TP12 or R94 Dwg. No. 3225225	 100 nsec/cm; 2 v/cm	Read Timing Output
12	TP15 or R138 Dwg. No. 3225225	 200 nsec/cm; 2 v/cm	Write Timing Output

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

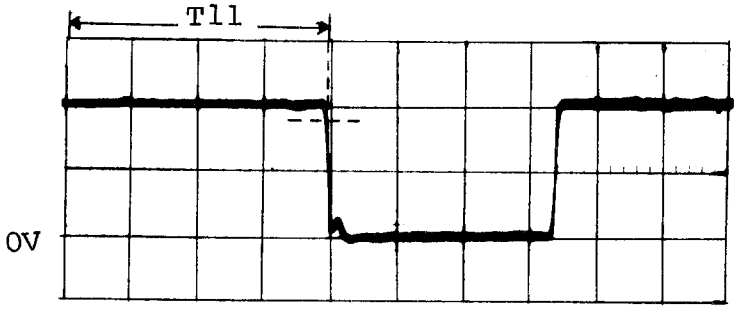
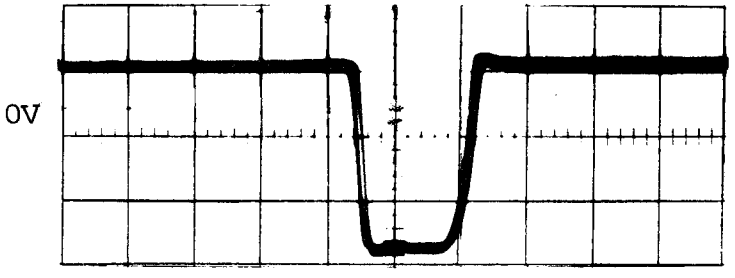
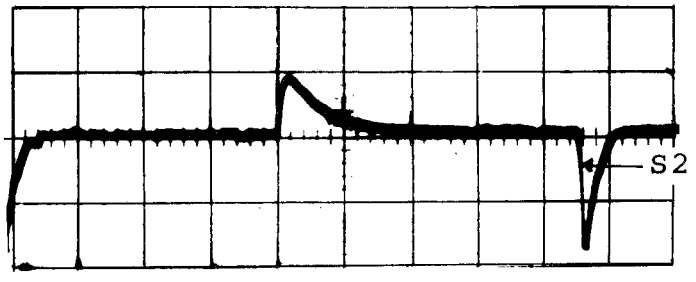
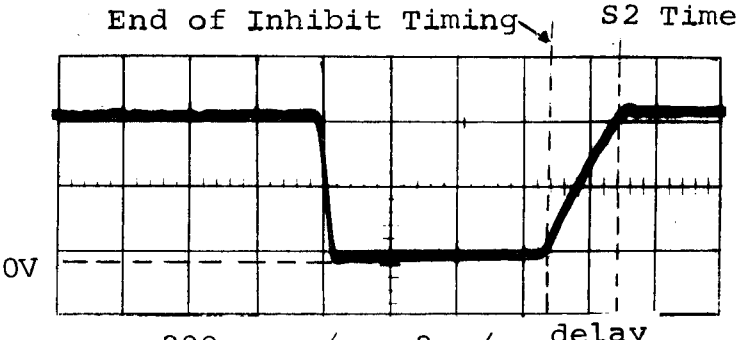
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
13	TP14 or R117 Dwg. No. 3225225	 200 nsec/cm; 2 v/cm	Inhibit Timing Output
14	TP13 or Q31 Emitter Dwg. No. 3225225	 100 nsec/cm; 5 v/cm	Sense Strobe Output
15	Pin 3 of IC14 Dwg. No. 3225225	 200 nsec/cm; 1 v/cm	S2, generated from end of inhibit timing, used to reset Memory Busy flip-flop at end of cycle.
16	Q42 base Dwg. No. 3225225	 200 nsec/cm; 2 v/cm	Delay circuit waveform, defining S2 time from end of inhibit timing

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

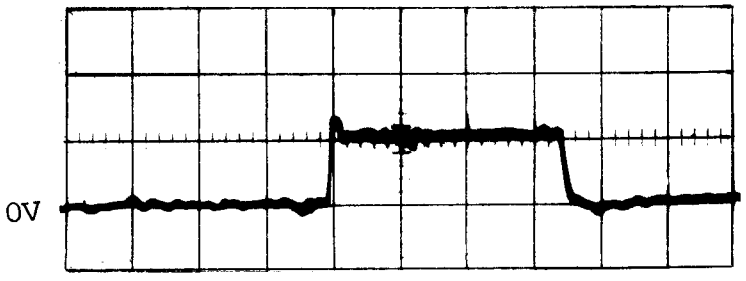
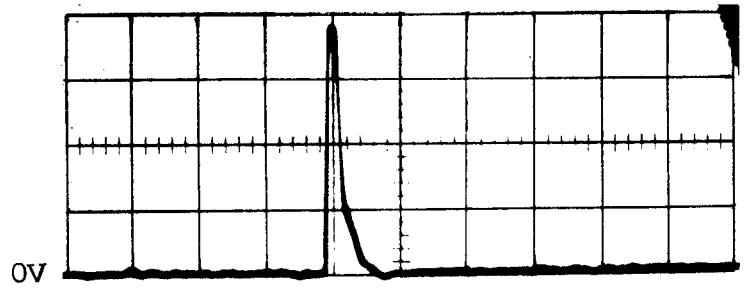
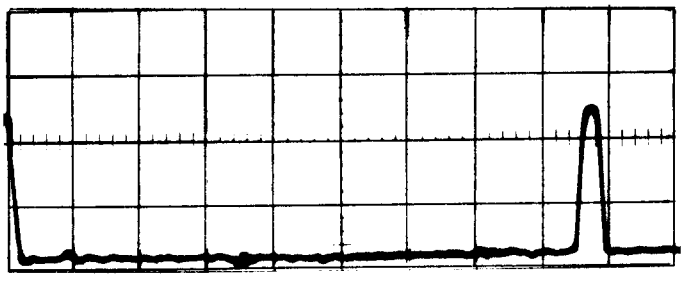
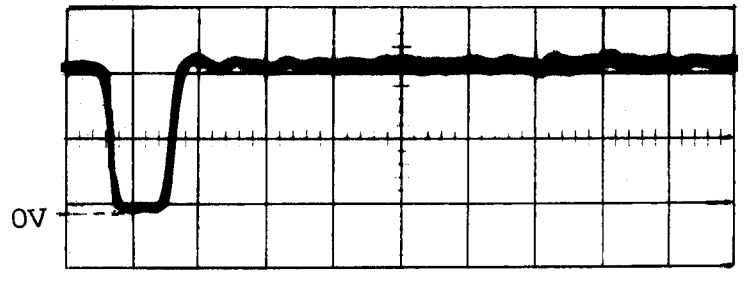
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
17	R61 Dwg. No. 3225225	 100 nsec/cm; 0.5 v/cm	Inhibit Current O/S Output
18	R55 Dwg. No. 3225225	 200 nsec/cm; 1 v/cm	Trigger pulse for inhibit current O/S and inhibit current delay O/S
19	Pin 6 of IC14 Dwg. No. 3225225	 100 nsec/cm; 1 v/cm	Memory Busy flip-flop reset pulses
20	TP8 & TP9 or R78 & R80 Dwg. No. 3225225	 100 nsec/cm; 0.5 v/cm	Address Strobe

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

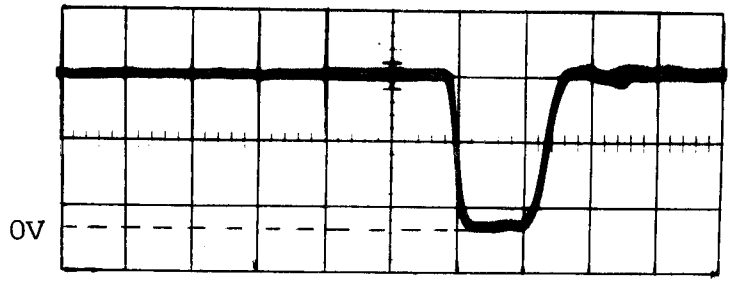
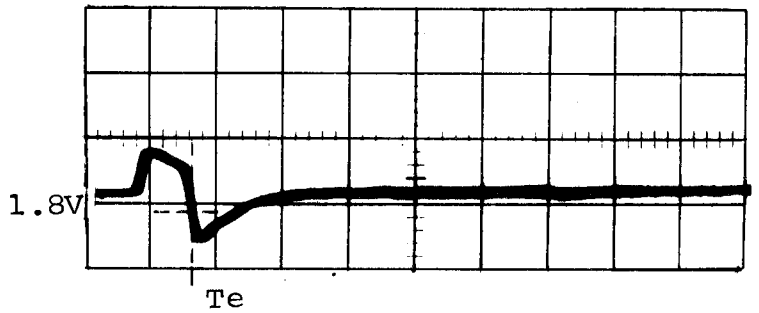
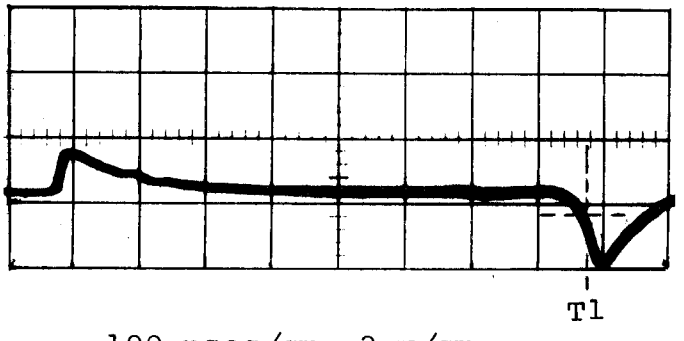
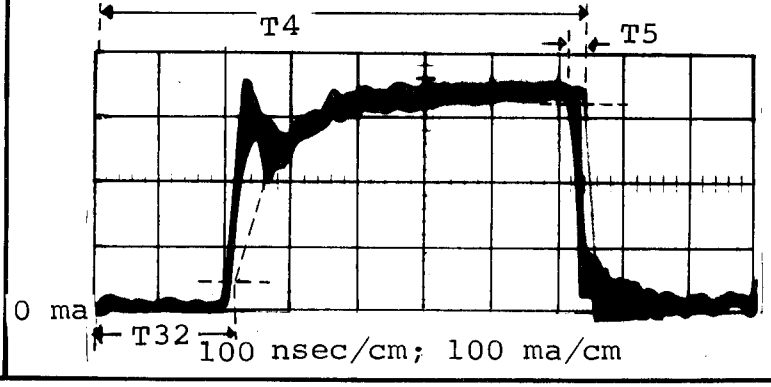
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
21	TP10 or TP11 Dwg. No. 3225225	 100 nsec/cm; 1 v/cm	Data Strobe; adjustable by data strobe delay o/s. Minimum and maximum timing shown in waveforms 22 & 23
22	Pin 3 of IC25 Dwg. No. 3225225	 100 nsec/cm; 2 v/cm	Earliest time (Te) for differentiated output of data strobe delay flip-flop
23	Pin 3 of IC25 Dwg. No. 3225225	 100 nsec/cm; 2 v/cm	Latest time (T1) for differentiated output of data strobe delay flip-flop
24	X Read or Y Read test loop (as marked on the board)	 100 nsec/cm; 100 ma/cm	Read current; dotted line indicates true current in drive line

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

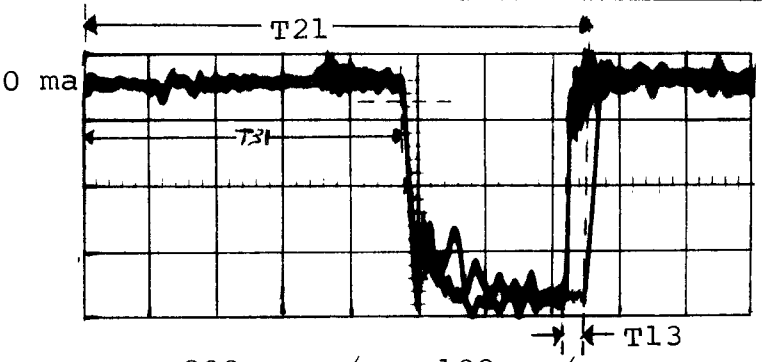
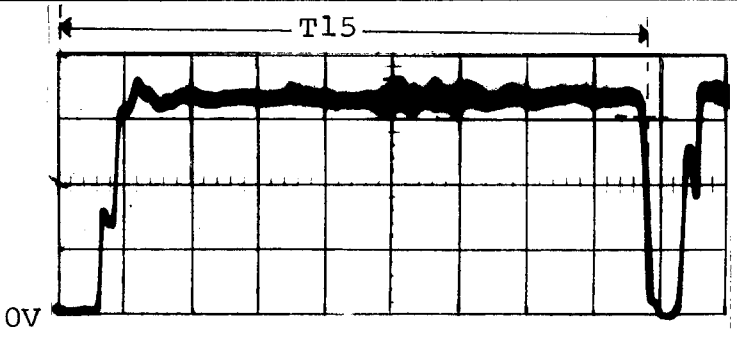
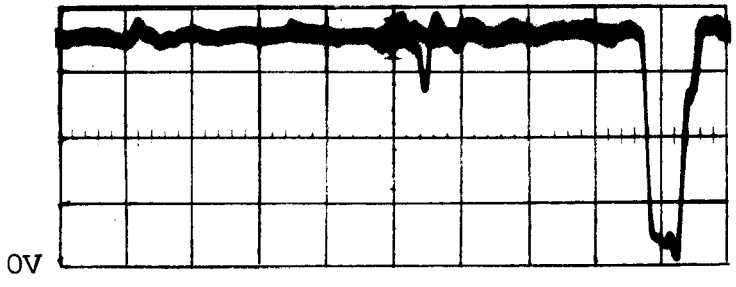
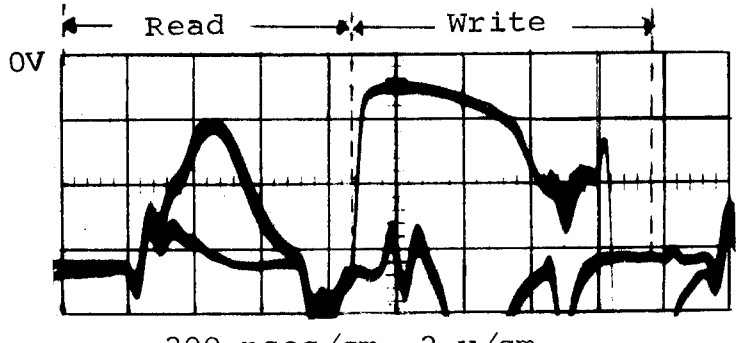
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
25	X Write or Y Write test loop (as marked on the board)	 200 nsec/cm; 100 ma/cm	Write Current
26	Pin J4-B35 or R15 Dwg. No. 3225225	 200 nsec/cm; 1 v/cm	Memory Busy output (memory cycle)
27	Pin J4-17B or R13 Dwg. No. 3225225	 200 nsec/cm; 1 v/cm	End of Cycle output (memory cycle)
28	TP17 or R11 Dwg. No. 3225228	 200 nsec/cm; 2 v/cm	Sense Amplifier output (memory mode, worst pattern)

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

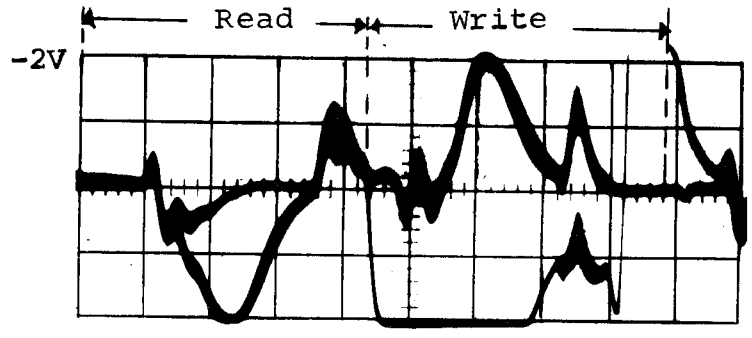
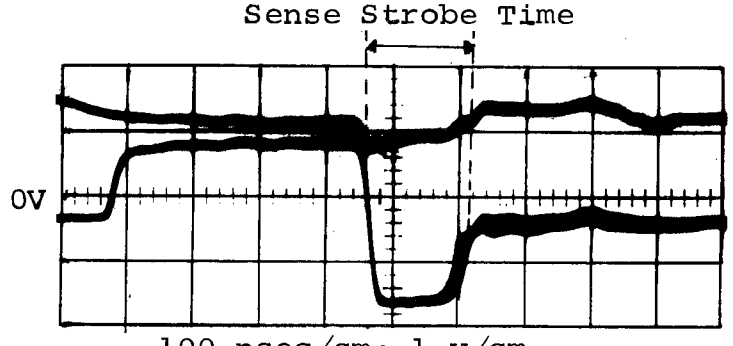
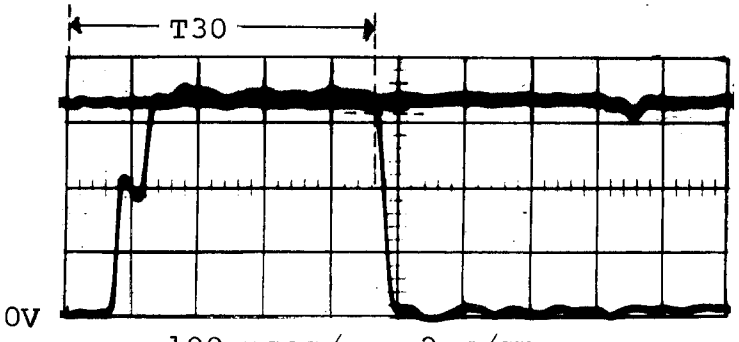
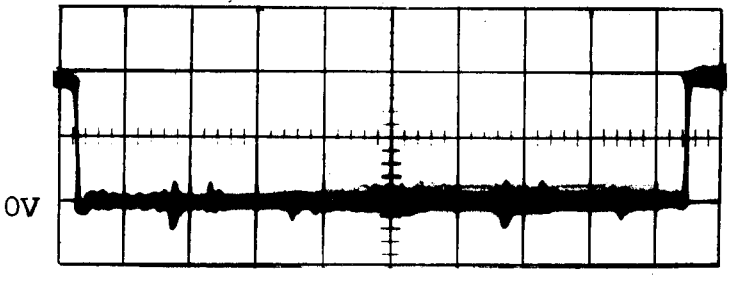
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
29	TP16 or R6 Dwg. No. 3225228	 200 nsec/cm; 2 v/cm	Sense Amplifier output (memory mode, worst pattern, complement side of differential output)
30	Q4 and Q5 collector Dwg. No. 3225228	 100 nsec/cm; 1 v/cm	Sense Amplifier discriminator output (worst pattern)
31	Output connector	 100 nsec/cm; 2 v/cm	Data output (worst pattern, loaded by 12' twisted pair with 560 ohm termination resistor, 6V nominal output level)
32	Pin 4 of IC6 Dwg. No. 3225219	 400 nsec/cm; 0.5 v/cm	Address Register output (AR0)

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

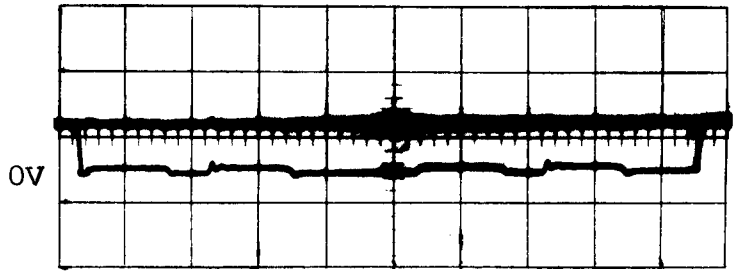
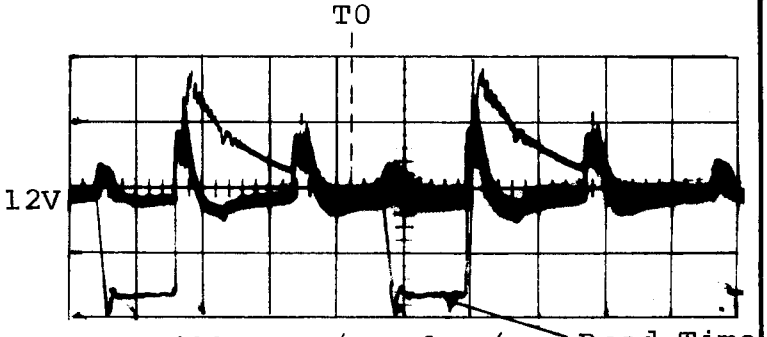
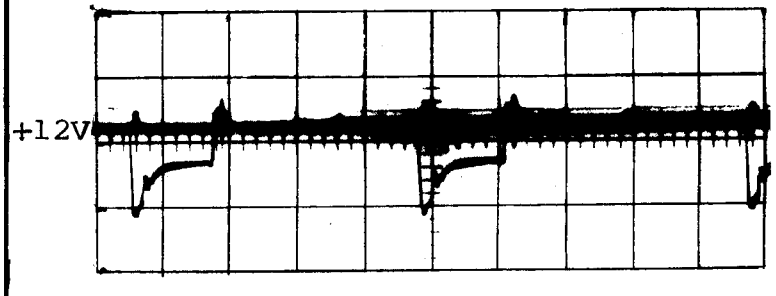
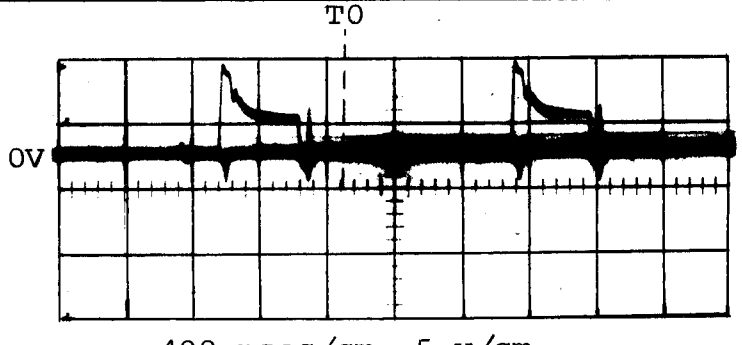
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
33	Pin 7 of IC13 Dwg. No. 3225219	 400 nsec/cm; 5 v/cm	Address Decoder output (AR0, AR2, AR4)
34	M1, Pin 3 Dwg. No. 3225213	 400 nsec/cm; 1 v/cm	Typical waveform at read switch module input
35	Common connection of read diode cluster	 400 nsec/cm; 5 v/cm	Read switch module output (X DR or Y DR as marked on the board, with counting address)
36	Common connection of write diode cluster	 400 nsec/cm; 5 v/cm	Write switch module output (X S or Y S, as marked on the board, with counting address)

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

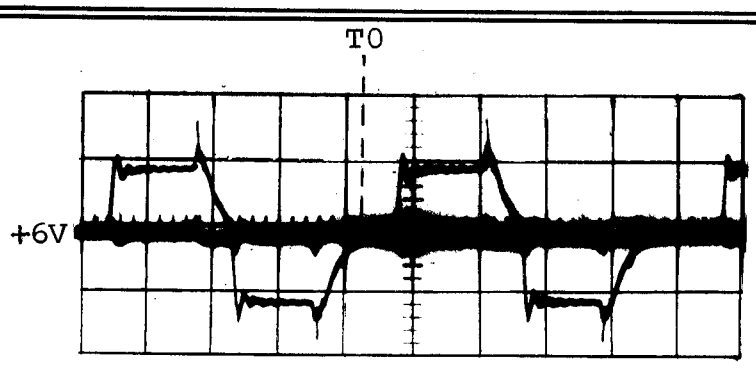
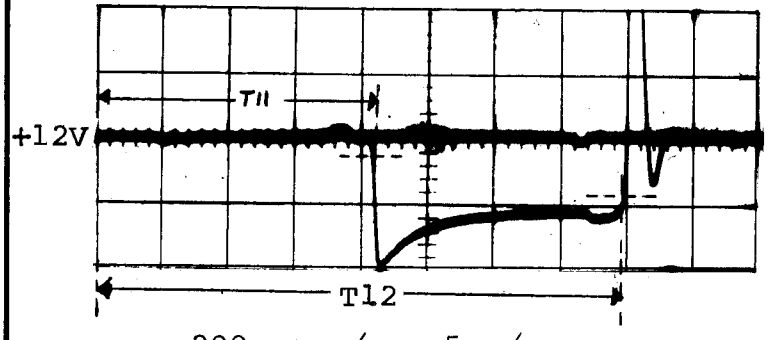
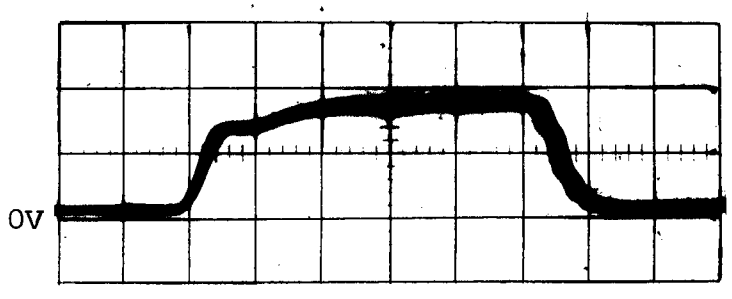
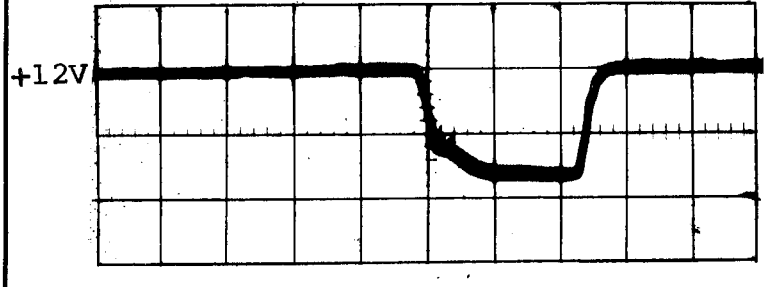
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
37	XS or YS, as marked on the board, with counting address	 400 nsec/cm; 5 v/cm	Sink module output (read-write combined)
38	See description	 200 nsec/cm; 5 v/cm	Voltage measured at the far side of inhibit resistor R20 or R43, from inhibit transistor Q10 or Q20 (Dwg. No. 3225228)
39	See description	 100 nsec/cm; 5 v/cm	Voltage measured at end of read current limiting resistor (marked X READ or Y READ)
40	See description	 200 nsec/cm; 5 v/cm	Voltage measured at end of write current limiting resistor (marked X WRITE or Y WRITE)

TABLE 5-2.
REFERENCE WAVEFORMS AND TIMING (Continued)

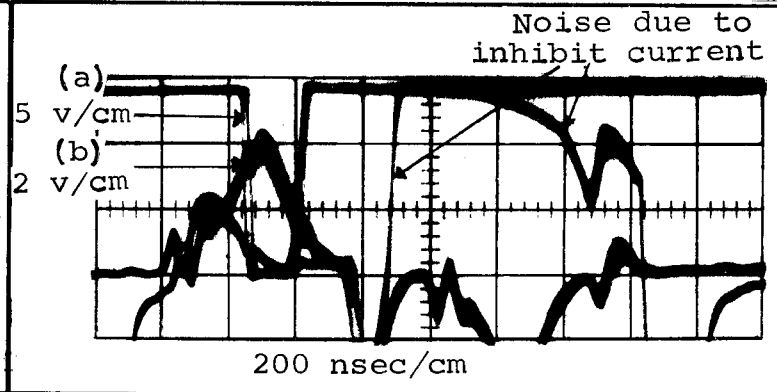
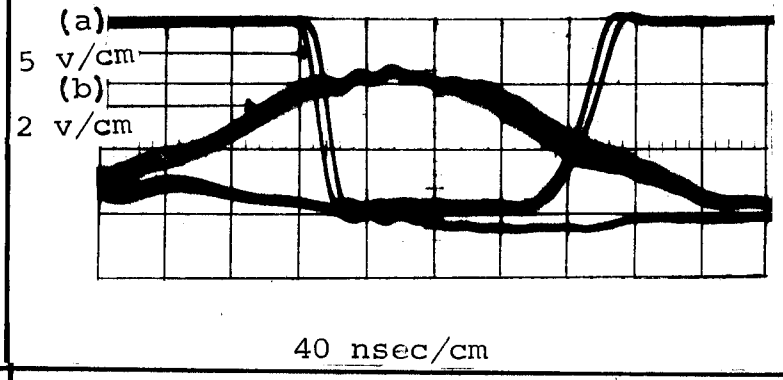
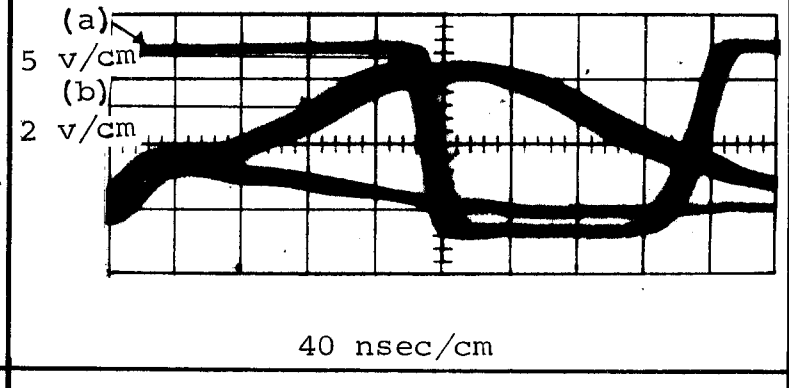
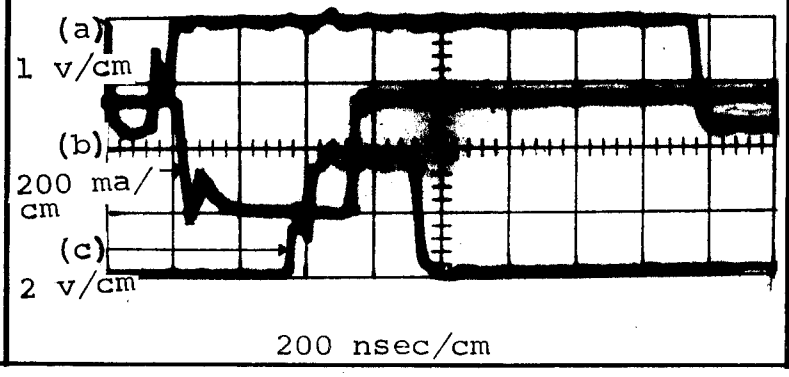
NO.	TEST POINT	NORMAL INDICATION	DESCRIPTION
41	(a) Q31 emitter or TP13 Dwg. No. 3225225(b) Q2,Q3 collector or TP16, TP17 Dwg. No. 3225228		At 25°C, Sense strobe timing (a) relative to core turn-over signal (b)
42	(a) Q31 emitter or TP13 Dwg. No. 3225225(b) Q2,Q3 collector or TP16, TP17 Dwg. No. 3225228		At 0°C, Sense strobe timing (a) relative to core turn-over signal (b)
43	(a) Q31 emitter or TP13 Dwg. No. 3225225(b) Q2,Q3 col- TP16, TP17 Dwg. No. 3225228		At 50°C, Sense strobe timing (a) relative to core turn-over signal (b)
44	(a)J4-B35 (b)74-B25 (c)X READ or Y READ test loop on the board		At 25°C, Memory Busy (a), read current (b) and Data Available (c) signals

TABLE 5-3.
FINAL ADJUSTMENT OF TIMING

STEP NO.	OPERATION OBJECTIVE	MODE OF OPERATION	POTENTIOMETER TO BE ADJUSTED	MONITORED AT	CRITERION	WAVEFORM NUMBER
1	Check read current termination time	Memory Mode (C-W then R-R)	READ (R37) CURRENT	X READ & Y READ	T_4 = 750ns (max)	24
2	Observe spread of read and write current termination		--	X READ & Y READ	T_5 < 70ns T_{13} < 70ns	24 25
3	Observe data available output		--	Data Available Output J4-25	T_7 < 600ns	44
4	Observe data output respect to data available		--	Data Available Output J4-25	T_7 > T30	44 31
5	Check leading edge of inhibit timing signal		E/R (MEM) (R52)	TP12 on as marked "Inhibit Timing"	T_{11} = 800ns	13
6	Check memory busy output for memory cycle		INH (R62)	Memory Busy Output J4-35	T_{15} = 1760ns	26
7	Check memory busy output for buffer-read cycle	Buffer-read	E/R (R112)	Memory Busy Output J4-35	T_{16} = 960ns	Similar to 26
8	Check memory busy output for buffer-write cycle	Buffer-write	E of W (R128)	Memory Busy Output J4-35	T_{16} = 960ns	Similar to 26
9	Check write current termination time	Memory on buffer-write	WRITE (R122)	X WRITE & Y WRITE	T_{21} = 1500ns (max)	25
10	Check data strobe time	Memory (C-W)	DSD (R86)	TP10, TP11	Adjust T_{17} to specified value. If not specified, 350ns.	
11	Check minimum read current duration	--	--	X&Y READ	T_4 (min) to T_{32} (max) > 400ns	24
12	Check minimum write current duration	--	--	X&Y WRITE	T_{21} (min) to T_{31} (max) > 400ns	25
13	Check that inhibit current overlaps write current	--	--	R20 or R43 Dwg. No. (3225228) and X&Y Write	T_{12} (min to T_{21} (max) > 20ns T_{31} (min) to T_{11} (max) > 100ns	38 25

5-3. PREVENTIVE MAINTENANCE.

Preventive maintenance procedures are designed to anticipate possible sources of system malfunction, and to apply corrective measures before trouble develops. Experience has proven that, due to the aging of circuit components, the following procedures should be applied at intervals of not more than three months.

The five procedures required are as follows:

5-4. SENSE AMPLIFIER BALANCE.

The following paragraph explains the proper procedure for checking and adjusting sense amplifier balance.

DC quiescent points of sense amplifier differential outputs should be adjusted to equal voltage (or balanced) by means of trimmers 1R3 or 2R3 mounted on preamplifier board. No specific input signal is needed for this adjustment. The output voltage must be balanced such that the difference between the two output voltages becomes less than 100 mv. The output voltages are monitored at transistor cans Q2 and Q3. The test setup is shown in Figure 5-1.

The quiescent output (after balancing) voltages V_Q must be between -5.5 and -6.5 volts.

5-5. CHECKING AND ADJUSTING TIMING.

Follow the steps outlined in Table 5-3 to check the timing and make the proper adjustment wherever it is required.

5-6. CHECKING AND ADJUSTING POWER SUPPLY VOLTAGES.

Follow the steps outlined in Table 5-4 to check the power supply voltages, making the proper adjustment wherever it is required.

5-7. DRIVE CURRENT MARGIN TEST.

While writing and reading worst pattern complement, adjust the +12 volt supply ±0.3 volt from the specified voltage at 25°C. Worst pattern complement is described in paragraph 5-14.

Operate the system at the maximum and minimum voltage specified above, for three minutes each. If there is a malfunction during the test period, take corrective action as indicated in the Troubleshooting Procedure.

5-8. V_{CL} MARGIN TEST.

While writing and reading worst pattern complement, adjust the V_{CL} supply ±0.3 volt from the specified voltage at 25°C.

Operate the system at the maximum and minimum voltage specified above, for three minutes each. If there is a malfunction during the test period, take corrective action as indicated in the Troubleshooting Procedure.

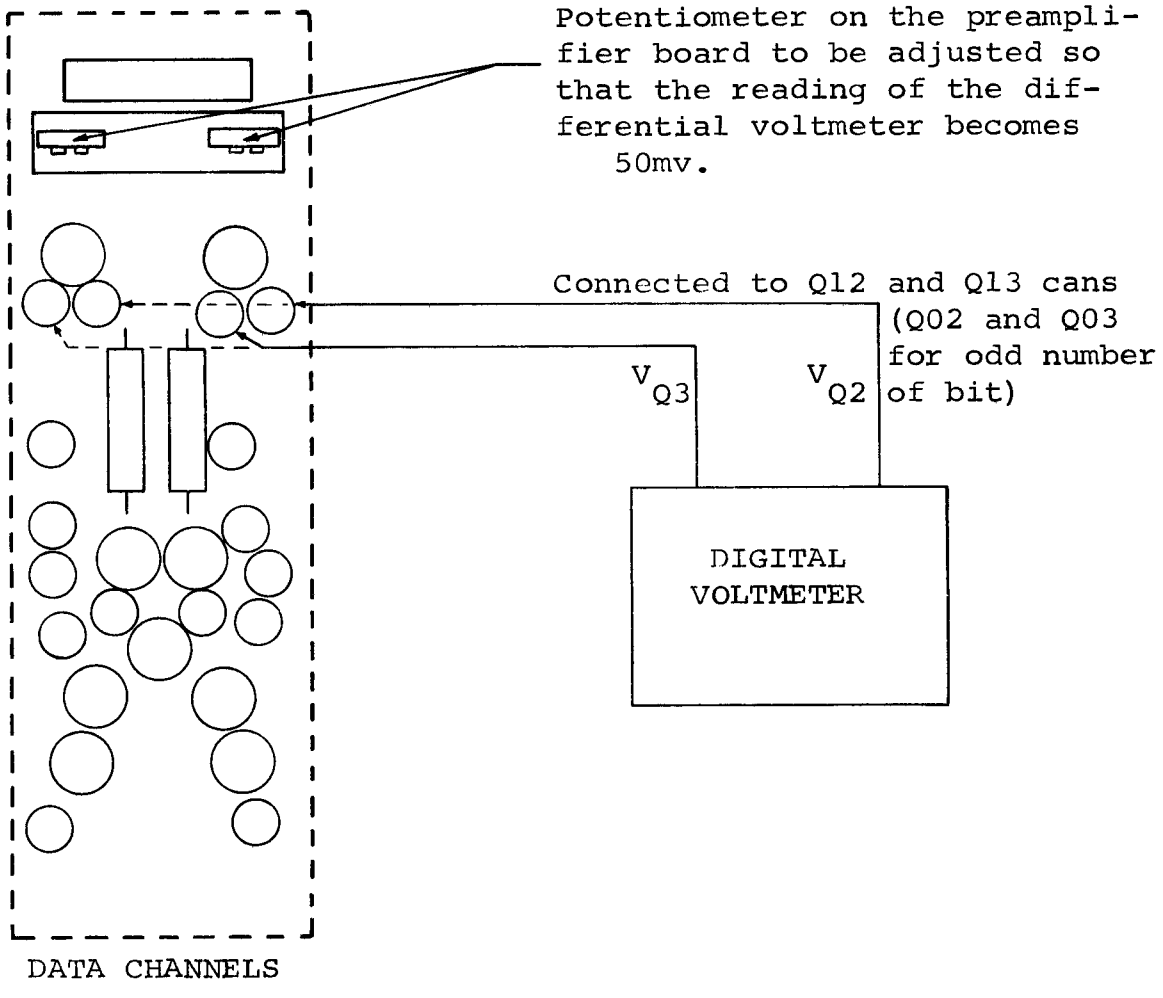


Figure 5-1.
Sense Amplifier Balancing Test Setup

TABLE 5-4.
POWER SUPPLY VOLTAGE SETTINGS

VOLTAGE	MONITORING POINT*	POTENTIOMETER TO ADJUSTED*	ADJUST TO
+12V (nominal) supply	Red	(8)	***
+6V (nominal) supply	Blue	(7)	+6V ±0.01V
+4V (nominal) supply	Yellow	(4)	+4V ±0.01V
-12V (nominal) supply	Green	(2)	-12V ±0.01V
Output clamp voltage (V_L)	White	(6)	**V_{Out} ±0.01V
Sense Amplifier Source Voltage (V_S)	Orange	(1)	-4V ±0.01V
Discriminator Clipping Level (V_{CL})	Brown	(9)	***
0V (ground)	Black		
Over voltage (over V)		(5)	DO NOT ADJUST
Over current (over I)		(3)	DO NOT ADJUST

* Locations of potentiometers and corresponding monitoring points are shown in Figure 5-2.

** V_{Out} is measured at End of Cycle output (J4-17) which rests on higher level (positive voltage) when the memory is in static condition.

*** Specified value on the final test report (V11-C-QE048).

5-9. TROUBLESHOOTING PROCEDURE.

Assuming that the first three steps contained in Preventive Maintenance have each been carried out, and a malfunction persists, the next step required is to localize the malfunction to a specific module or component.

The best approach to the problem is to employ a systematic method of signal tracing, determining which system to employ by observation of major symptoms. Four major areas are explored in Figures 5-3 through 5-6.

In the figures, the seven-digit numbers in parenthesis refer to applicable schematics, which are printed elsewhere in this manual. Employment of "WFxx" refers to the applicable waveform or waveforms, presented in Table 5-2.

It should be realized that the troubleshooting flow charts are presented only as an aid to localizing the malfunction. It is not possible in such a flow chart to itemize the troubles which could arise in a single component or module. However, tests to determine if a specific component or module is capable of functioning properly are common knowledge among personnel capable of maintaining and repairing solid state circuitry at the level of data processing systems.

5-10. COMPONENT REPLACEMENT.

Because of the possibility of introducing further malfunctions through inept replacement of components, special techniques, which are outlined below, are recommended for use with this system.

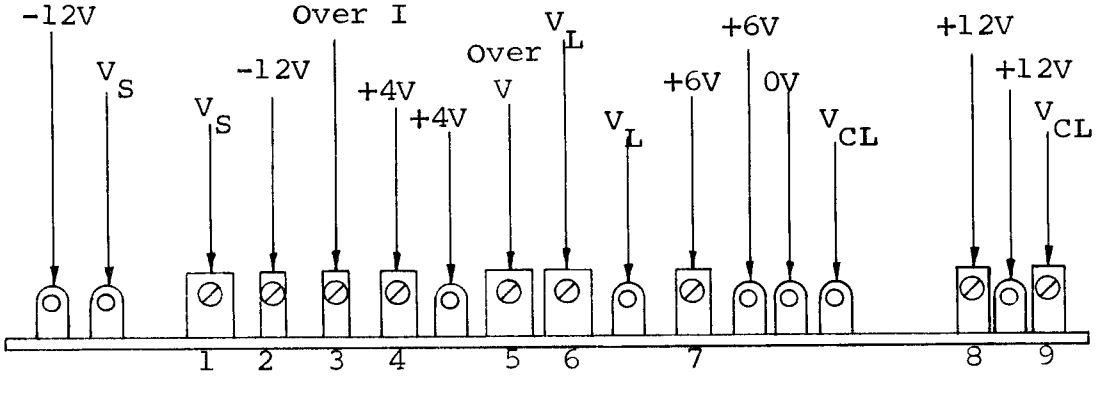


Figure 5-2.
Rear View of Power Supply Adjustments

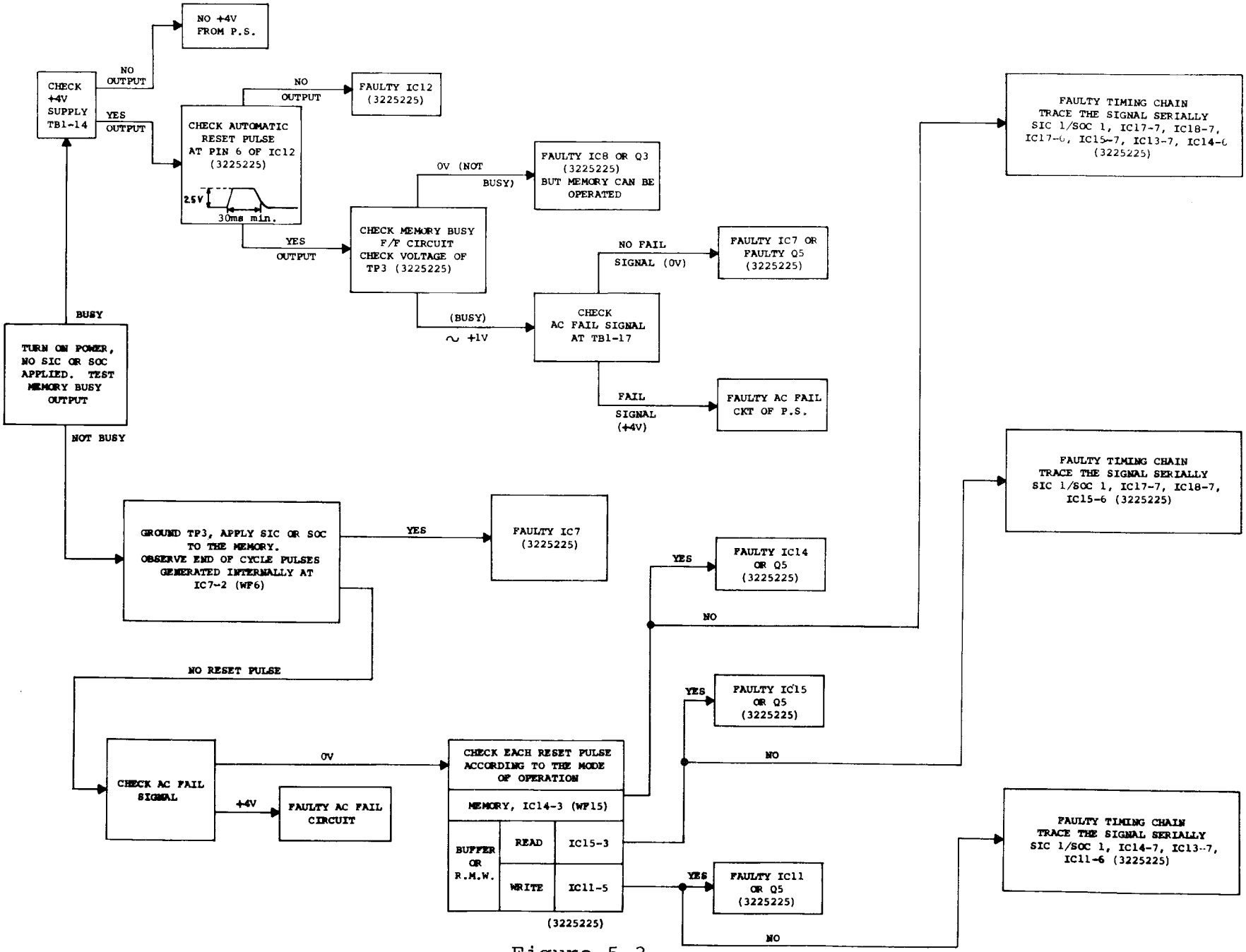


Figure 5-3.
TROUBLESHOOTING CHART. Case 1: Power is "ON" But Cycle Cannot be Initiated

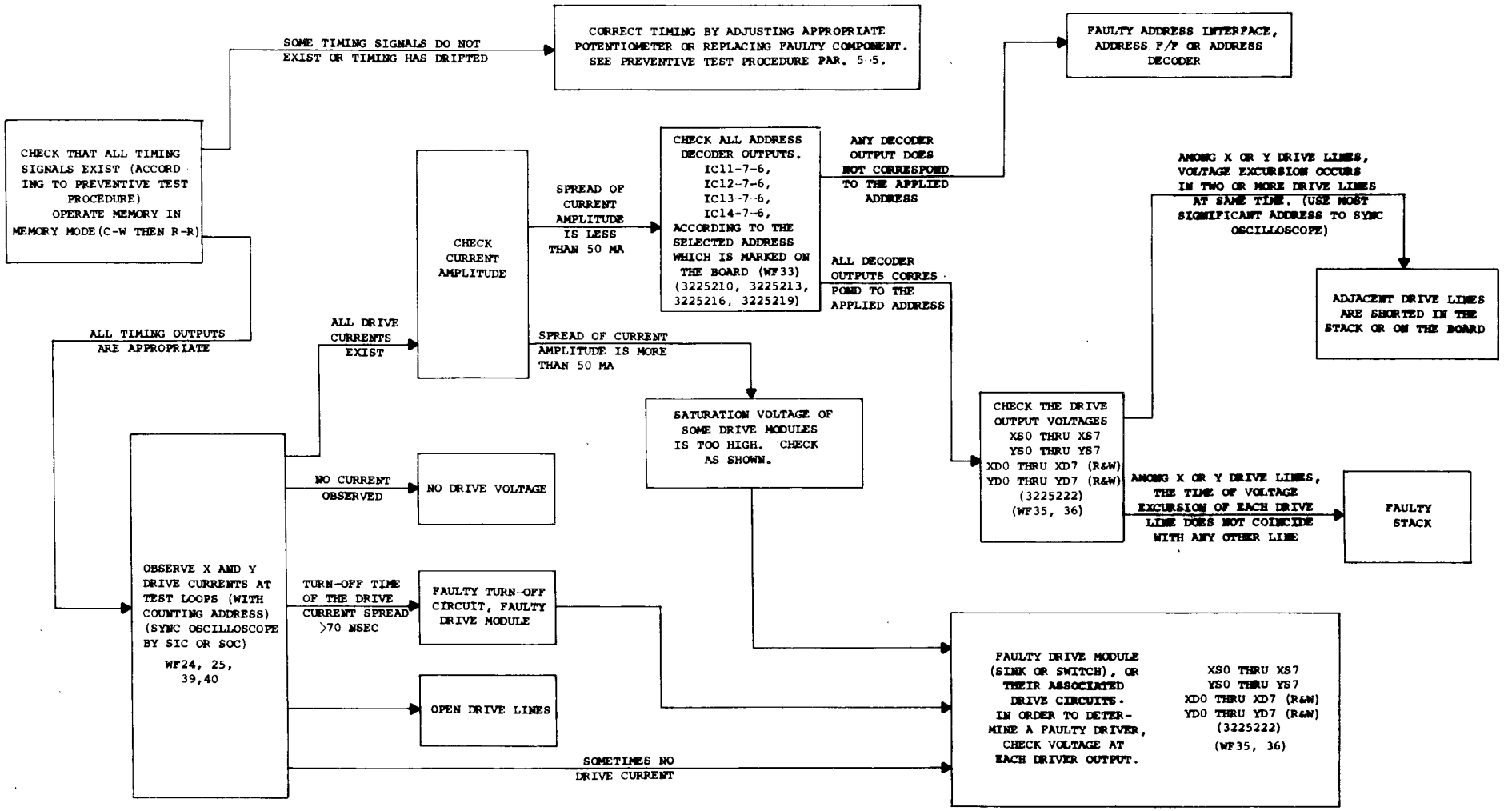


Figure 5-4.
TROUBLESHOOTING CHART. Case 2: Memory Busy Signal is OK, But All Bits Fail

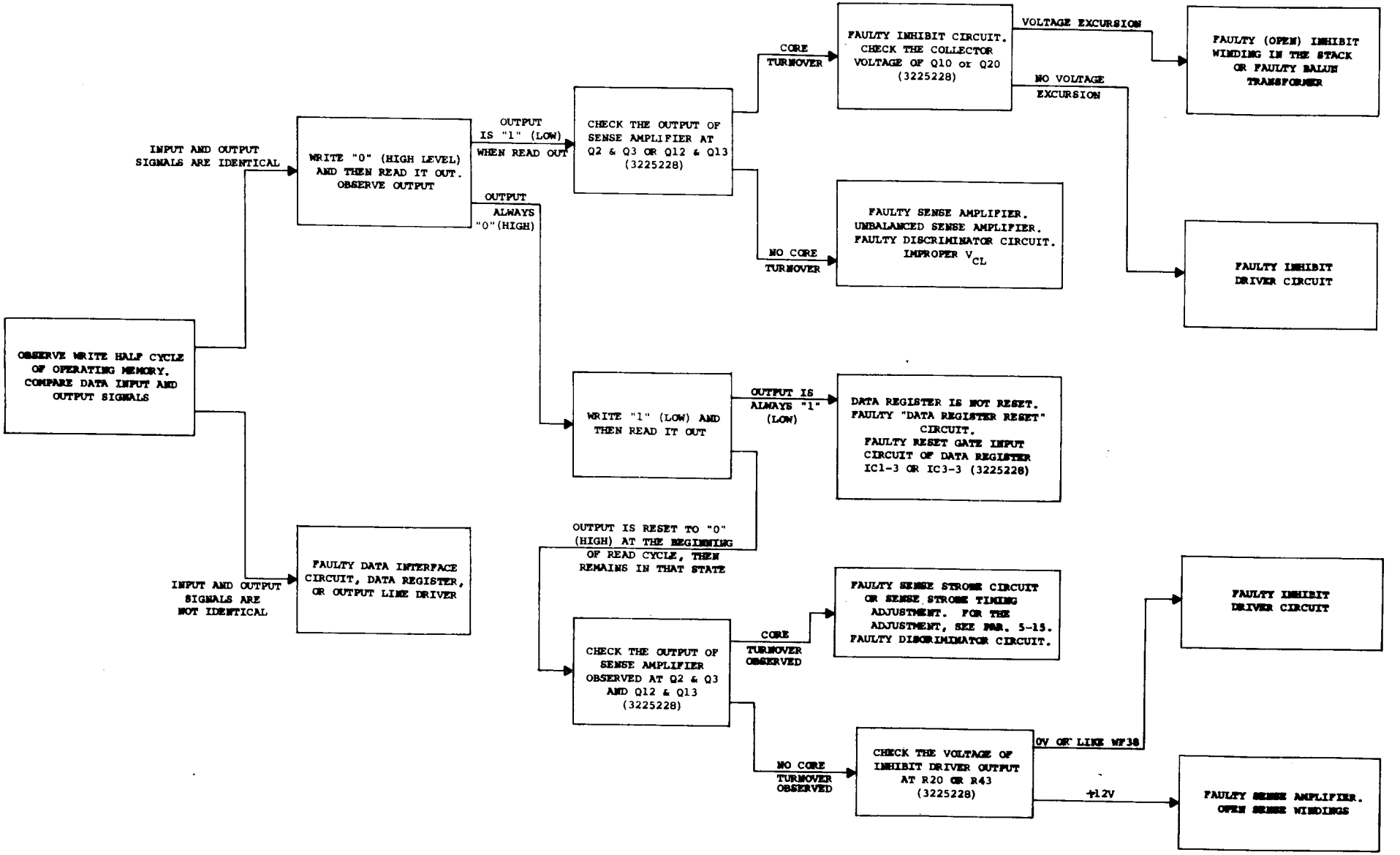


Figure 5-5.
TROUBLESHOOTING CHART. Case 3: Some Bits Show Errors (With the Pattern ONE or ZERO)

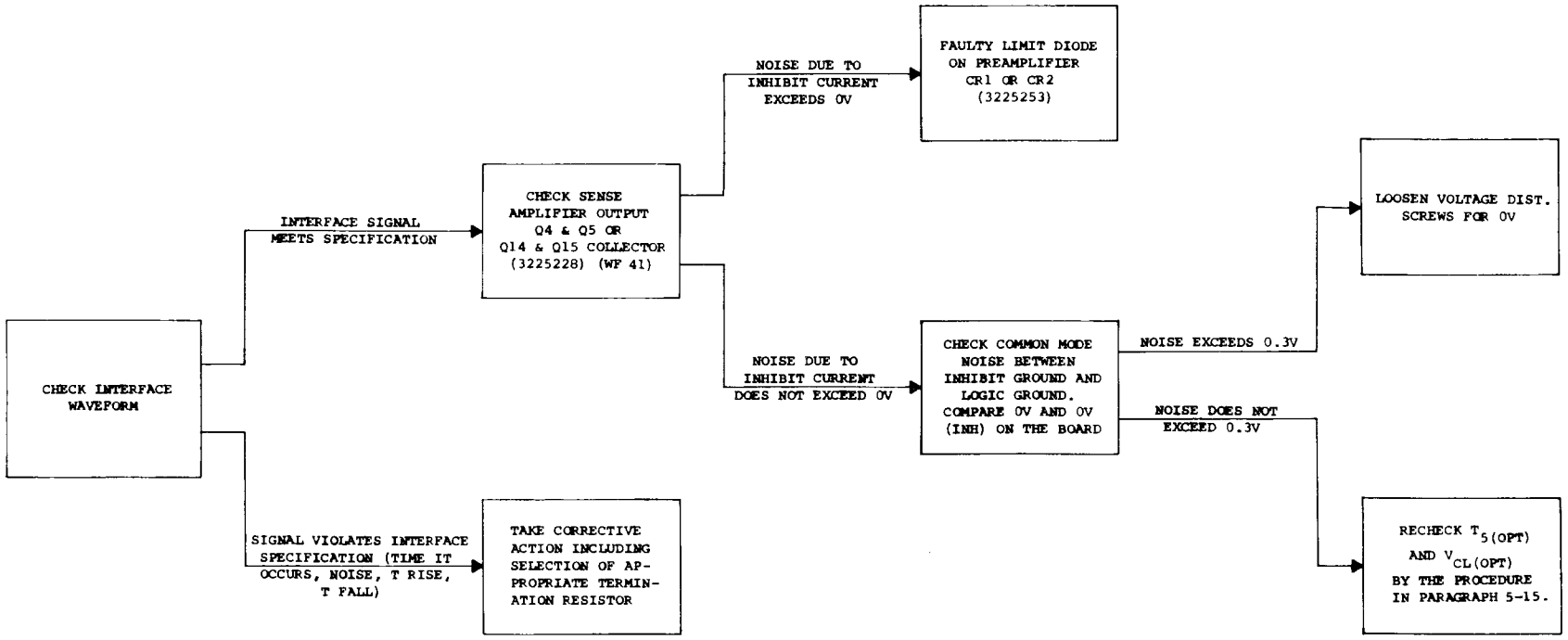


Figure 5-6.
TROUBLESHOOTING CHART. Case 4: Error with Worst Pattern. (If error occurs with worst pattern, although test procedures for Case 1-3 are satisfied, use this test sequence)

5-11. REPLACEMENT OF INTEGRATED CIRCUIT, DIODE, RESISTOR OR PRE-AMPLIFIER.

When replacing one of the above components, perform the following steps:

(a) From the component side of the board, clip all leads of the defective component and discard it.

(b) On the dip side of the board, use a small soldering iron to apply heat to each lead in turn, pushing the lead through from the component side until it may be grasped on the dip side by a long-nose plier and removed.

(c) From the dip side, continue to apply heat to each eyelet, using a solder sucker to remove solder.

(d) Insert leads on replacement from the component side, solder them into the eyelets, and clip off excess lengths.

5-12. REPLACEMENT OF DRIVE MODULE, BALUN TRANSFORMER OR TRANSISTOR.

When replacing one of the above components, perform the following steps:

(a) Use a solder iron to apply heat from the dip side, using a solder sucker to remove solder from the leads and eyelets.

(b) Move the leads around in the eyelets until they are free after the circuit has cooled.

(c) From the component side, grasp and remove the defective component.

(d) Insert the replacement from the component side, solder the leads in the eyelets, applying heat from the dip side.

5-13. MAGNETIC CORE STACK.

No attempt should be made to effect repairs within the stack. If an internal malfunction is detected, the master module should be returned to the factory for stack repair.

5-14. WORST PATTERN CHECKS.

This check consists of writing the worst pattern or its complement into the memory and operating the equipment under normal conditions. The following paragraphs explain matrix noise and worst pattern.

The sense winding links the cores of a matrix in such a manner that maximum cancellation of disturb noise is effected at the output of the sense winding. However, if the noise produced by a core in the ZERO state is not exactly equal to that produced by a core in the ONE state, a difference noise signal is generated. Thus, if all cores that produce negative signals at the output terminals of a sense winding contain ONEs and all others contain ZEROs, the maximum noise is produced on the sense winding when reading from any address. This is worst pattern.

NOTE

This noise is the result of the matrix data content, and is not due to the electrostatic coupling between the inhibit and sense windings.

The worst pattern is the array of ONEs and ZEROs in a matrix which will produce the maximum resultant delta noise at the output of the sense winding. Two patterns exist which can be called worst pattern, with one the complement of the other. One of these patterns is arbitrarily called worst pattern and the other is called worst pattern complement. Figure 5-7 shows the loading of ONEs and ZEROs into a typical 4096-word memory for worst pattern.

Table 5-5 presents the worst pattern and worst pattern complement logic equations for a 4096-word memory. Loading is determined by address bits AR0, AR1 and AR11. Worst pattern consists in storing a data word consisting of all ONEs at each address where the address bits agree with the logic shown, and a data word consisting of all ZEROs at all other addresses.

In a memory having a capacity of less than 4096 words, worst pattern and worst pattern complement loading are determined by address bits AR0, AR1 and the most significant odd address bit. In Table 5-5, the most significant odd address bit replaces the AR11 address bit shown.

5-15. OPTIMAL SENSE STROBE TIMING AND V_{CL} (25°C) (See Figures 5-5/5-6.)

First of all, T_s which is measured from the strobe at test point (TP13 on sense strobe) to the peak time of the core turnover signal (TP16 or TP17) should be adjusted approximately 20 ns (with

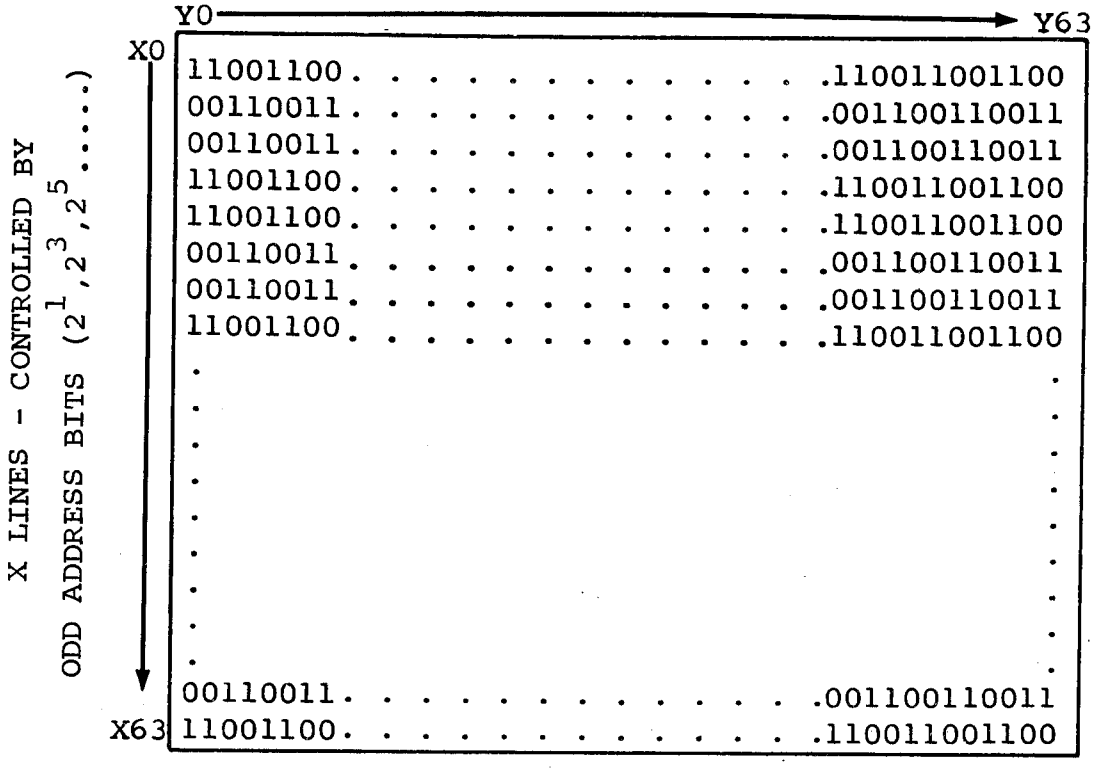


Figure 5-7.
Worst Pattern in 4096-Word Memory

the test signal pattern to be set as WP/$\overline{WP}$ alternating). Then vary the sense strobe timing and find the optimum timing of the sense strobe with respect to the core turnover signal. The optimum time $T_{s(opt)}$ is defined as follows:

$$\text{At } T_{s(opt)} \rightarrow \Delta V_{CL} \text{ is maximum}$$

where, $\Delta V_{CL} = \overline{V}_{CL} - \underline{V}_{CL}$

moreover, V_{CL} and $\underline{V}_{CL}$ are maximum and minimum values of

V_{CL} with which the memory operates.

TABLE 5-5.
WORST PATTERN AND WORST PATTERN COMPLEMENT LOGIC
FOR 4096-WORD MEMORY

Worst Pattern Logic	$AR11 \cdot AR1 \cdot \overline{AR0}$ $+\overline{AR11} \cdot \overline{AR1} \cdot \overline{AR0}$ $+\overline{AR11} \cdot AR1 \cdot AR0$ $+AR11 \cdot \overline{AR1} \cdot AR0$
Worst Pattern Complement Logic	$AR11 \cdot AR1 \cdot AR0$ $+\overline{AR11} \cdot \overline{AR1} \cdot AR0$ $+\overline{AR11} \cdot AR1 \cdot \overline{AR0}$ $+AR11 \cdot \overline{AR1} \cdot \overline{AR0}$

Furthermore, $T_{s(opt)}$ must be

$$0 \text{ ns} < T_{s(opt)} < 40 \text{ ns}.$$

Optimal V_{CL} ($V_{CL(opt)}$ may be obtained as

$$V_{CL(opt)} = \underline{V}_{CL} + \frac{\Delta V_{CL}}{2}$$

Where $\underline{V}_{CL}$ and ΔV_{CL} are measured at $T_{s(opt)}$.

If WP/$\overline{WP}$ alternating is not available, determine $T_{s(opt)}$ and V_{CL} for each worst pattern and worst pattern complement, and take the average value.

5-16. MASTER MODULE INPUT-OUTPUT CONNECTIONS.

The master module plugs into two input-output connectors, J3 and J4. Each connector is composed of 65 pairs of pins. The top row, on the component side of the master module, is designated the Upper Level; the bottom row, on the dip side of the master module, is called the Lower Level.

Table 5-6 shows all signal and DC voltages to input-output connectors J3 and J4.

5-17. RECOMMENDED SPARE PARTS LIST.

Table 5-7 presents a list of spare parts recommended for one RF-1 Magnetic Core Memory.

TABLE 5-6.
MASTER MODULE INPUT-OUTPUT CONNECTIONS

CONN.	PIN NO.	UPPER LEVEL (COMPONENT SIDE)	LOWER LEVEL (DIP SIDE)
J4	1	IN	GRD
	2	A.C. FAILURE	
	3	+4V (Timing)	+4V (Timing)
	4	Data 0 Out	GRD
	5	Data 0 In	GRD
	6	Data 1 In	GRD
	7	Data 1 Out	GRD
	8	External Data Register Set	GRD
	9	External Data Register Reset	GRD
	10	Logic 2	GRD
	11	Spare	Spare
	12	V_L	V_L
	13	Spare	Spare
	14	Logic 1	GRD
	15	External Data Transfer	GRD
	16	External Address Transfer	GRD
	17	End of Cycle	GRD
	18	+12V (Inh)	+12V (Inh)
	19	+12V (Inh)	+12V (Inh)
	20	+12V (Inh)	+12V (Inh)
	21	Data 2 Out	GRD
	22	Data 2 In	GRD
	23	Data 3 In	GRD
J4	24	Spare	Spare

TABLE 5-6.
MASTER MODULE INPUT-OUTPUT CONNECTIONS (Continued)

CONN.	PIN NO.	UPPER LEVEL (COMPONENT SIDE)	LOWER LEVEL (DIP SIDE)
J4	25	Data Available	GRD
	26	SOC	GRD
	27	SIC	GRD
	28	External Address Set	GRD
	29	External Address Reset	GRD
	30	+4V	+4V
	31	+4V	+4V
	32	+4V	+4V
	33	Data 3 Out	GRD
	34	Temp. Sensing 1	Temp. Sensing 2
	35	Memory Busy	GRD
	36	GRD	GRD
	37	GRD	GRD
	38	Data 4 Out	GRD
	39	Data 4 In	GRD
	40	Data 5 In	GRD
	41	-12V	-12V
	42	-12V	-12V
	43	Data Out 5	GRD
	44	Spare	Spare
	45	Add. 0 Out Reset	GRD
	46	Add. 0 Out Set	GRD
	47	Add. 0 In	GRD
	48	Add. 2 Out Reset	GRD
	49	Add. 2 Out Set	GRD
J4	50	Add. 2 In	GRD

TABLE 5-6.
MASTER MODULE INPUT-OUTPUT CONNECTIONS (Continued)

CONN.	PIN NO.	UPPER LEVEL (COMPONENT SIDE)	LOWER LEVEL (DIP SIDE)
J4	51	Add. 4 Out Reset	GRD
	52	Add. 4 Out Set	GRD
	53	Add. 4 In	GRD
	54	0V (Inh)	0V (Inh)
	55	0V (Inh)	0V (Inh)
	56	0V (Inh)	0V (Inh)
	57	Data Out 6	GRD
	58	Data In 6	GRD
	59	Data In 7	GRD
	60	Data Out 7	GRD
	61	Data Out 8	GRD
	62	Data In 8	GRD
	63	Data In 9	GRD
	64	+12V	+12V
J4	65	+12V	+12V
J3	1	+12V (Inh)	+12V (Inh)
	2	+12V (Inh)	+12V (Inh)
	3	+12V (Inh)	+12V (Inh)
	4	Data 9 Out	GRD
	5	Data 10 Out	GRD
	6	Data 10 In	GRD
	7	Data 11 In	GRD
	8	Add. 11 Out Reset	GRD
	9	Add. 11 Out Set	GRD
	10	Add. 11 In	GRD
	11	Add. 9 Out Reset	GRD
J3	12	Add. 9 Out Set	GRD

TABLE 5-6.
MASTER MODULE INPUT-OUTPUT CONNECTIONS (Continued)

CONN.	PIN NO.	UPPER LEVEL (COMPONENT SIDE)	LOWER LEVEL (DIP SIDE)
J3	13	Add. 9 In	GRD
	14	Add. 7 Out Reset	GRD
	15	Add. 7 Out Set	GRD
	16	Add. 7 In	GRD
	17	Logic 0V	Logic 0V
	18	Logic 0V	Logic 0V
	19	Logic 0V	Logic 0V
	20	Logic 0V	Logic 0V
	21	Data 11 Out	GRD
	22	Data 12 Out	GRD
	23	Data 12 In	GRD
	24	Data 13 In	GRD
	25	Data 13 Out	GRD
	26	Spare	Spare
	27	Add. 1 Out Reset	GRD
	28	Add. 1 Out Set	GRD
	29	Add. 1 In	GRD
	30	Add. 3 Out Reset	GRD
	31	Add. 3 Out Set	GRD
	32	Add. 3 In	GRD
	33	Add. 5 Out Reset	GRD
	34	Add. 5 Out Set	GRD
	35	Add. 5 In	GRD
	36	+6V	+6V
	37	+6V	+6V
	38	Data 14 Out	GRD
J3	39	Data 14 In	GRD

TABLE 5-6.
MASTER MODULE INPUT-OUTPUT CONNECTIONS (Continued)

CONN.	PIN NO.	UPPER LEVEL (COMPONENT SIDE)	LOWER LEVEL (DIP SIDE)
J3	40	Data 15 In	GRD
	41	Data 15 Out	GRD
	42	Inh 0V	Inh 0V
	43	Inh 0V	Inh 0V
	44	Inh 0V	Inh 0V
	45	Spare	Spare
	46	Spare	Spare
	47	Spare	Spare
	48	Add. 10 Out Reset	GRD
	49	Add. 10 Out Set	GRD
	50	Add. 10 In	GRD
	51	Add. 8 Out Reset	GRD
	52	Add. 8 Out Set	GRD
	53	Add. 8 In	GRD
	54	Add. 6 Out Reset	GRD
	55	Add. 6 Out Set	GRD
	56	Add. 6 In	GRD
	57	Data 16 Out	GRD
	58	Data 16 In	GRD
	59	Data 17 In	GRD
	60	Data 17 Out	GRD
	61	+4V	+4V
	62	+4V	+4V
	63	+4V	+4V
	64	V_{CL}	
J3	65		V_S

TABLE 5-7.
RECOMMENDED SPARE PARTS LIST

DESCRIPTION	PART NUMBER	QTY. SPARES REC'D
Transistor	014-364	1
Transistor	014-505	3
Transistor	014-588	2
Transistor	014-631	2
Transistor	014-633	2
Transistor	014-634	4
Transistor	014-635	12
Transistor	014-636	2
Transistor	014-669	2
Transistor Pair	014-672	3
Zener Diode	013-332	2
Zener Diode	013-383	2
Zener Diode	013-625	2
Stabistor	013-696	2
Transistor	3201116-10	3
Diode	3263029-10	10
Integrated Circuit	586-007	6
Integrated Circuit	586-008	6
Module	586-026	4
Module	560-232	3
Variable Potentiometer	044-934	1
Transformer	560-224	1
Diode Cluster, Common Anode (4)	3225140-01	2
Diode Cluster, Common Anode (8)	3225141-01	2
Diode Cluster, Common Cathode (4)	3225142-01	2
Diode Cluster, Common Cathode (8)	3225143-01	2
Circuit Board Assy. Sense Pre-Amp	3225253-01	2
Extender Board	3225285-10	1

5-18. TROUBLESHOOTING THE STACK.

When it is suspected that there is a malfunction within the stack, i.e., in one or more of the drive lines, it may become necessary to physically locate a specific drive line or a pair of lines, as determined by the address at which the malfunction occurs. The RF Drive System Schematic, Dwg. No. 3225222, in the Theory of Operation, illustrates the method of numbering the X and Y drive lines in a 4096-word memory. The paragraphs which follow can be used to determine lines to be tested, as well as providing supplementary information on the application of worst pattern and worst pattern complement for testing purposes.

In the tables which follow, it should be borne in mind that address as well as data inputs are expressed in negative true logic. This means that a logical ONE is represented by application of the more negative of two input levels, so that application of such a level will produce core turnover.

As explained in the theory of operation, in a 4096-word memory the decoding of six odd-number address bits will select one of 64 X drive lines, and the decoding of six even-number address bits will select one of 64 X drive lines. Table 5-8 can be used to determine the numbers of the selected X and Y lines for any 12-bit address.

Table 5-9 is a truth table which presents address information used to select specific lines. Its further purpose is to determine whether ONE or ZERO is to be loaded in generating a worst pattern or worst pattern complement. The logic equations are:

$$PX = AR11 \cdot AR1 + \overline{AR11} \cdot \overline{AR1}. \quad PY = \overline{AR0}$$

$$\begin{aligned}\text{Worst Pattern} = PX \cdot PY + \overline{PX} \cdot \overline{PY} &= (AR11 \cdot AR1 + \overline{AR11} \cdot \overline{AR1})\ \overline{AR0} \\ &+ (\overline{AR11} \cdot AR1 + AR11 + \overline{AR1})\ AR0 \\ &= AR11 \cdot AR1 \cdot \overline{AR0} + \overline{AR11} \cdot \overline{AR1} \cdot \overline{AR0} \\ &+ \overline{AR11} \cdot AR1 \cdot AR0 + AR11 \cdot \overline{AR1} \cdot AR0\end{aligned}$$

$$\begin{aligned}\text{Worst Pattern Complement} = PX \cdot \overline{PY} + \overline{PX} \cdot PY &= (AR11 \cdot AR1 + \overline{AR11} \cdot \overline{AR1})\ AR0 \\ &+ (\overline{AR11} \cdot AR1 + AR11 \cdot \overline{AR1})\ \overline{AR0} \\ &= AR11 \cdot AR1 \cdot AR0 + \overline{AR11} \cdot \overline{AR1} \cdot AR0 \\ &+ \overline{AR11} \cdot AR1 \cdot \overline{AR0} + AR11 \cdot \overline{AR1} \cdot \overline{AR0}\end{aligned}$$

TABLE 5-8.
SELECTION OF X AND Y DRIVE LINES

SINK CIRCUIT / SWITCH CIRCUIT											
			AR1	0	1	0	1	0	1	0	1
			AR3	0	0	1	1	0	0	1	1
			AR5	0	0	0	0	1	1	1	1
AR 11	AR 9	AR 7	XS / XD	0	1	2	3	4	5	6	7
0	0	0	0	X7	X5	X3	X1	X15	X13	X11	X9
0	0	1	1	X23	X21	X19	X17	X31	X29	X27	X25
0	1	0	2	X39	X37	X35	X33	X47	X45	X43	X41
0	1	1	3	X55	X53	X51	X49	X63	X61	X59	X57
1	0	0	4	X54	X52	X50	X48	X62	X60	X58	X56
1	0	1	5	X38	X36	X34	X32	X46	X44	X42	X40
1	1	0	6	X22	X20	X18	X16	X30	X28	X26	X24
1	1	1	7	X6	X4	X2	X0	X14	X12	X10	X8

X DRIVE LINES

TABLE 5-8.
SELECTION OF X AND Y DRIVE LINES (Continued)

SWITCH CIRCUIT / SINK CIRCUIT										
			AR0	0	1	0	1	0	1	0	1
			AR2	0	0	1	1	0	0	1	1
			AR4	0	0	0	0	1	1	1	1
AR 10	AR 8	AR 6	YS / YD	0	1	2	3	4	5	6	7
0	0	0	0	Y8	Y10	Y12	Y14	Y0	Y2	Y4	Y6
0	0	1	1	Y24	Y26	Y28	Y30	Y16	Y18	Y20	Y22
0	1	0	2	Y40	Y42	Y44	Y46	Y32	Y34	Y36	Y38
0	1	1	3	Y56	Y58	Y60	Y62	Y48	Y50	Y52	Y54
1	0	0	4	Y57	Y59	Y61	Y63	Y49	Y51	Y53	Y55
1	0	1	5	Y41	Y43	Y45	Y47	Y33	Y35	Y37	Y39
1	1	0	6	Y25	Y27	Y29	Y31	Y17	Y19	Y21	Y23
1	1	1	7	Y9	Y11	Y13	Y15	Y1	Y3	Y5	Y7

Y DRIVE LINES

TABLE 5-9.
GENERATION OF WORST PATTERN

X DRIVE LINE	ADDRESS REGISTER (AR) 11 9 7 5 3 1	PX
X0	1 1 1 0 1 1	1
X1	0 0 0 0 1 1	0
X2	1 1 1 0 1 0	0
X3	0 0 0 0 1 0	1
X4	1 1 1 0 0 1	1
X5	0 0 0 0 0 1	0
X6	1 1 1 0 0 0	0
X7	0 0 0 0 0 0	1
X8	1 1 1 1 1 1	1
X9	0 0 0 1 1 1	0
X10	1 1 1 1 1 0	0
X11	0 0 0 1 1 0	1
X12	1 1 1 1 0 1	1
X13	0 0 0 1 0 1	0
X14	1 1 1 1 0 0	0
X15	0 0 0 1 0 0	1
X16	1 1 0 0 1 1	1
X17	0 0 1 0 1 1	0
X18	1 1 0 0 1 0	0
X19	0 0 1 0 1 0	1
X20	1 1 0 0 0 1	1
X21	0 0 1 0 0 1	0
X22	1 1 0 0 0 0	0
X23	0 0 1 0 0 0	1
X24	1 1 0 1 1 1	1
X25	0 0 1 1 1 1	0
X26	1 1 0 1 1 0	0
X27	0 0 1 1 1 0	1
X28	1 1 0 1 0 1	1
X29	0 0 1 1 0 1	0
X30	1 1 0 1 0 0	0
X31	0 0 1 1 0 0	1

X DRIVE LINE	ADDRESS REGISTER (AR) 11 9 7 5 3 1	PX
X32	1 0 1 0 1 1	1
X33	0 1 0 0 1 1	0
X34	1 0 1 0 1 0	0
X35	0 1 0 0 1 0	1
X36	1 0 1 0 0 1	1
X37	0 1 0 0 0 1	0
X38	1 0 1 0 0 0	0
X39	0 1 0 0 0 0	1
X40	1 0 1 1 1 1	1
X41	0 1 0 1 1 1	0
X42	1 0 1 1 1 0	0
X43	0 1 0 1 1 0	1
X44	1 0 1 1 0 1	1
X45	0 1 0 1 0 1	0
X46	1 0 1 1 0 0	0
X47	0 1 0 1 0 0	1
X48	1 0 0 0 1 1	1
X49	0 1 1 0 1 1	0
X50	1 0 0 0 1 0	0
X51	0 1 1 0 1 0	1
X52	1 0 0 0 0 1	1
X53	0 1 1 0 0 1	0
X54	1 0 0 0 0 0	0
X55	0 1 1 0 0 0	1
X56	1 0 0 1 1 1	1
X57	0 1 1 1 1 1	0
X58	1 0 0 1 1 0	0
X59	0 1 1 1 1 0	1
X60	1 0 0 1 0 1	1
X61	0 1 1 1 0 1	0
X62	1 0 0 1 0 0	0
X63	0 1 1 1 0 0	1

TABLE 5-9.
GENERATION OF WORST PATTERN (Continued)

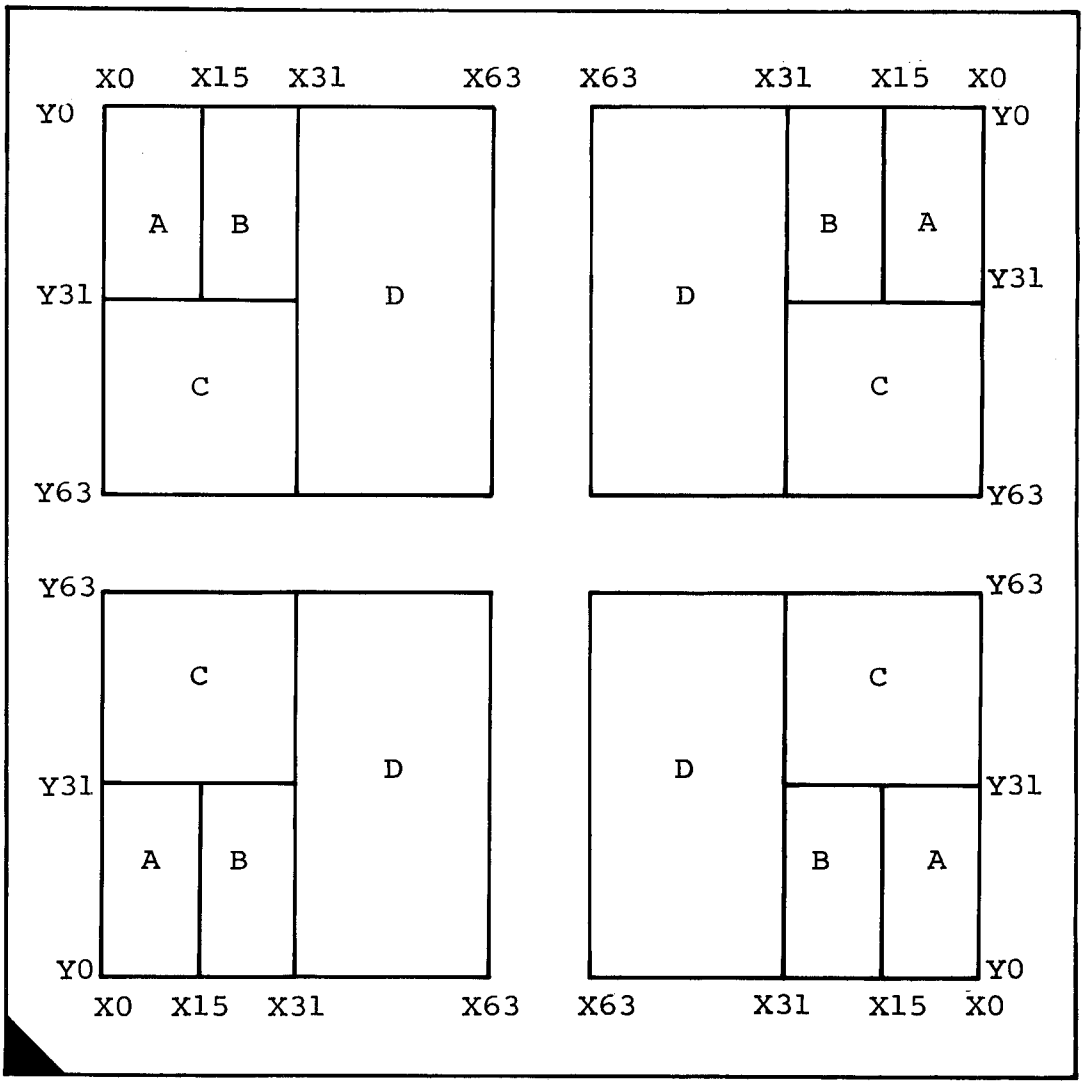
Y DRIVE LINE	ADDRESS REGISTER (AR) 10 8 6 4 2 0	PY
Y0	0 0 0 1 0 0	1
Y1	1 1 1 1 0 0	1
Y2	0 0 0 1 0 1	0
Y3	1 1 1 1 0 1	0
Y4	0 0 0 1 1 0	1
Y5	1 1 1 1 1 0	1
Y6	0 0 0 1 1 1	0
Y7	1 1 1 1 1 1	0
Y8	0 0 0 0 0 0	1
Y9	1 1 1 0 0 0	1
Y10	0 0 0 0 0 1	0
Y11	1 1 1 0 0 1	0
Y12	0 0 0 0 1 0	1
Y13	1 1 1 0 1 0	1
Y14	0 0 0 0 1 1	0
Y15	1 1 1 0 1 1	0
Y16	0 0 1 1 0 0	1
Y17	1 1 0 1 0 0	1
Y18	0 0 1 1 0 1	0
Y19	1 1 0 1 0 1	0
Y20	0 0 1 1 1 0	1
Y21	1 1 0 1 1 0	1
Y22	0 0 1 1 1 1	0
Y23	1 1 0 1 1 1	0
Y24	0 0 1 0 0 0	1
Y25	1 1 0 0 0 0	1
Y26	0 0 1 0 0 1	0
Y27	1 1 0 0 0 1	0
Y28	0 0 1 0 1 0	1
Y29	1 1 0 0 1 0	1
Y30	0 0 1 0 1 1	0
Y31	1 1 0 0 1 1	0

Y DRIVE LINE	ADDRESS REGISTER (AR) 10 8 6 4 2 0	PY
Y32	0 1 0 1 0 0	1
Y33	1 0 1 1 0 0	1
Y34	0 1 0 1 0 1	0
Y35	1 0 1 1 0 1	0
Y36	0 1 0 1 1 0	1
Y37	1 0 1 1 1 0	1
Y38	0 1 0 1 1 1	0
Y39	1 0 1 1 1 1	0
Y40	0 1 0 0 0 0	1
Y41	1 0 1 0 0 0	1
Y42	0 1 0 0 0 1	0
Y43	1 0 1 0 0 1	0
Y44	0 1 0 0 1 0	1
Y45	1 0 1 0 1 0	1
Y46	0 1 0 0 1 1	0
Y47	1 0 1 0 1 1	0
Y48	0 1 1 1 0 0	1
Y49	1 0 0 1 0 0	1
Y50	0 1 1 1 0 1	0
Y51	1 0 0 1 0 1	0
Y52	0 1 1 1 1 0	1
Y53	1 0 0 1 1 0	1
Y54	0 1 1 1 1 1	0
Y55	1 0 0 1 1 1	0
Y56	0 1 1 0 0 0	1
Y57	1 0 0 0 0 0	1
Y58	0 1 1 0 0 1	0
Y59	1 0 0 0 0 1	0
Y60	0 1 1 0 1 0	1
Y61	1 0 0 0 1 0	1
Y62	0 1 1 0 1 1	0
Y63	1 0 0 0 1 1	0

It is to be noted that the above equations are identical to those presented in Table 5-5.

Thus far, the discussion has centered around a memory with a capacity of 4096 words. However, the customer has the option of securing a memory containing 2048 words, 1024 words or 512 words. When one of these options is exercised, the number of X and Y lines on a matrix is reduced. The various configurations are illustrated in Figure 5-8. Shown are the four matrices (providing for four data bits) mounted on one side of an array.

As indicated in Figure 5-8, the number of X and Y drive lines varies with the word capacity of the stack. Similarly, the number of address bits decreases as the word capacity of the stack is reduced. Table 5-10 shows the effect of decreasing the most significant bits of address on the number of line drivers (switches) employed. It should be appreciated that a change in the number of address bits also has an effect upon the worst pattern and worst pattern complement equations. Accordingly, the table shows logic equations for each of the optional stack configurations. These equations in turn can be employed as they apply to Table 5-9.



WORD COMBINATIONS

4K = A + B + C + D
2K = A + B + C
1K = A + B
1/2K = A

Figure 5-8.
Optional Stack Configurations