MC6801/03 PORT EXPANSION

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MC6801/MC6803 PORT EXPANSION

The I/O capabilities of the MC6801/03 can be easily expanded. In effect, the number of I/O ports available can be increased to accomodate user needs with simple designs utilizing relatively inexpensive parts.

This application note describes several methods of port expansion.

MC6801/03 EXPANDED MULTIPLEXED MODE PORT EXPANSION

Figure 1 illustrates several methods for increasing the I/O capability of the MC6801/03 in the expanded multiplexed modes.* All these methods utilize ICs interfaced to the data bus.

Figure 1a shows a means of using the SN74LS374 as a latched input port. A strobe from a remote peripheral or MPU is used to latch data into the LS374. The MC6801/03 can read the latched contents of the LS374 by pulling $\overline{O.E.}$ low utilizing E·I/O Select as shown. When not selected the LS374 is held in a high-impedance state, thus eliminating data bus contention.

The SN74LS374 can also be used as a latched output port, as shown in Figure 1b. Data from the MC6801/03 is latched into the LS374 on the falling edge of E when I/O Select is high. Latched data can be continuously presented to the remote peripheral or MPU by tying $\overline{O.E.}$ low, as shown, or can be gated by the remote peripheral by an appropriate "I/O Select" logic control of $\overline{O.E.}$

An unlatched input port can be designed using a SN74LS244, as shown in Figure 1c. The octal three-state buffer presents data to the data bus with E·I/O Select and is particularly suited for MPU read of switches using polling. Once again, when not "selected," this peripheral is held in a high-impedance state, thus eliminating bus contention on the data bus.

A more straightforward approach to port expansion is illustrated in Figure 1d. Here an MC6821 is used to yield a net gain of two handshaking bidirectional ports. The MC6801/03 is compatible with all 6800 family peripherals, including the MC6821. Programming, pinout, and interface information for the MC6821 is provided in its data sheet, readily available from Motorola field offices and distributors.

*The MC6803 is limited to expanded multiplexed (modes 2 and 3) operation.

MC6801/03 SCI PORT EXPANSION

Port expansion is possible using the MC6801/03 SCI (Serial Communications Interface) operated in the standard NRZ format. This format consists of a start bit (low), eight data bits, and one stop bit (high). When no data is being sent the line is held high, indicating an idle line.

All the SCI port expansion schemes described in this application note utilize the SCI clock brought out externally from the MC6801/03 as provided by a software option.

SCI PORT OUTPUT EXPANSION

Figure 2 shows a means of expanding the SCI to 16 sets of 4-bit nibbles yielding 64 I/O output lines.

The key element of this circuit is the start-bit recognition system. The serial bit stream is inverted before reaching the SN74LS164 serial-in, parallel-out shift register. An idle line, therefore, loads the shift register and the two LS74's (U2, U3) with zeros. The SN74LS154 decoder is consequently disabled with $\overline{E}$ high, keeping its outputs high. During this time no clocking is provided to the SN74LS175's, and their data outputs are unchanged.

Data transmitted out of the SCI is preceded by a start bit. This low start bit is inverted and clocked through the LS164 and the LS74's as a high. One-half clock time after the start bit is clocked into F/F U2, it is clocked into F/F U3. At this time the eight SCI data bits are in the LS164. The LS154 is enabled and decodes the four SLB's of the data (transmitted first). The four MSB's of the SCI data byte are I/O output data and are tied to all LS175's with appropriate buffering.

Decoding by the LS154 clocks the addressed 175, latching in the data.

One-half SCI clock time later, the LS164 is cleared by driving the $\overline{MR}$ pin low. F/F U2 is also cleared. The system is now ready for another SCI data byte. If no more data is transmitted, 1's are transmitted indicating an idle line and output data remains unchanged.

Figure 3 illustrates a scheme for expanding the SCI port to an 8-bit output port.

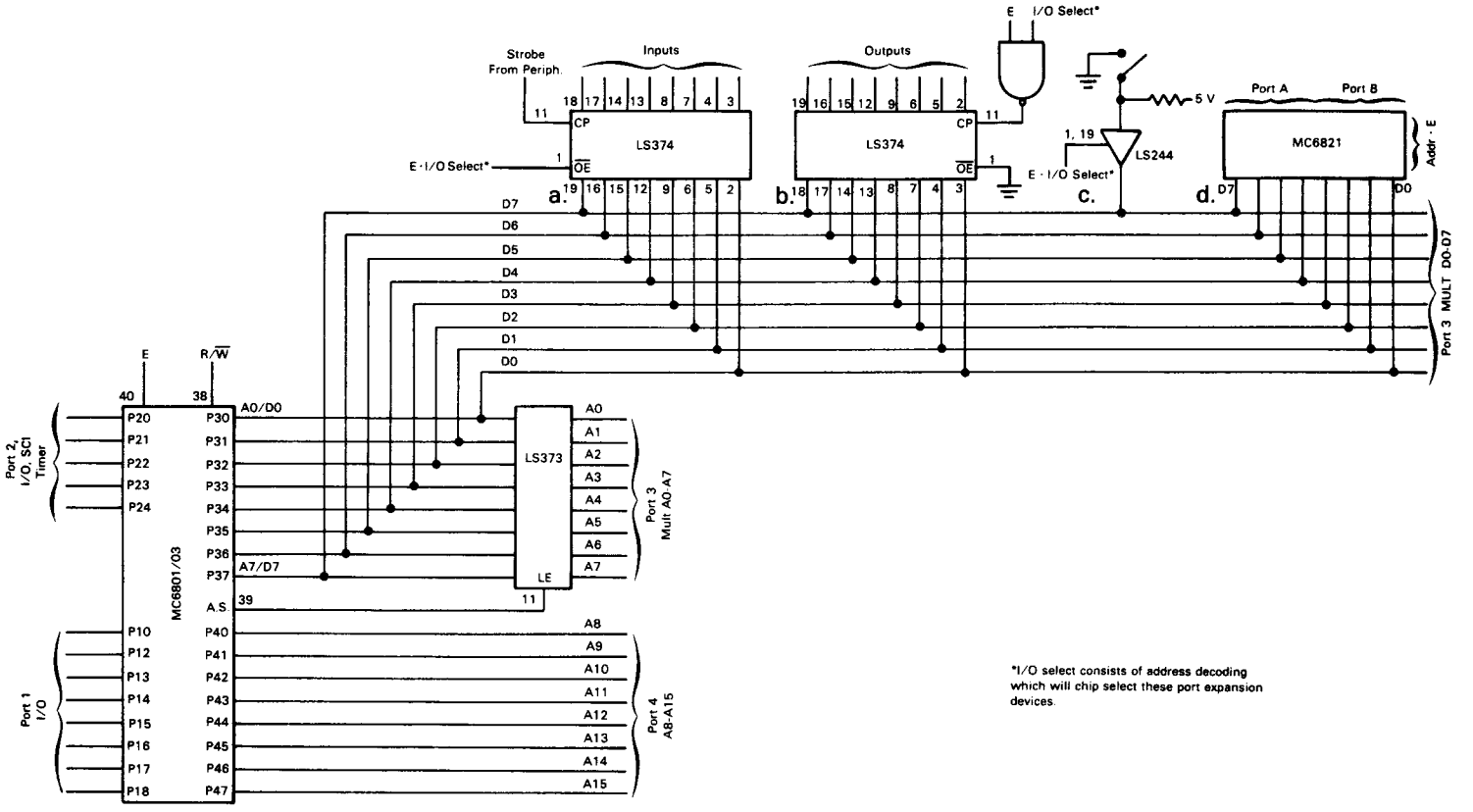


FIGURE 1 — MC6801/MC6803 Expanded Multiplexed Mode Port Expansion

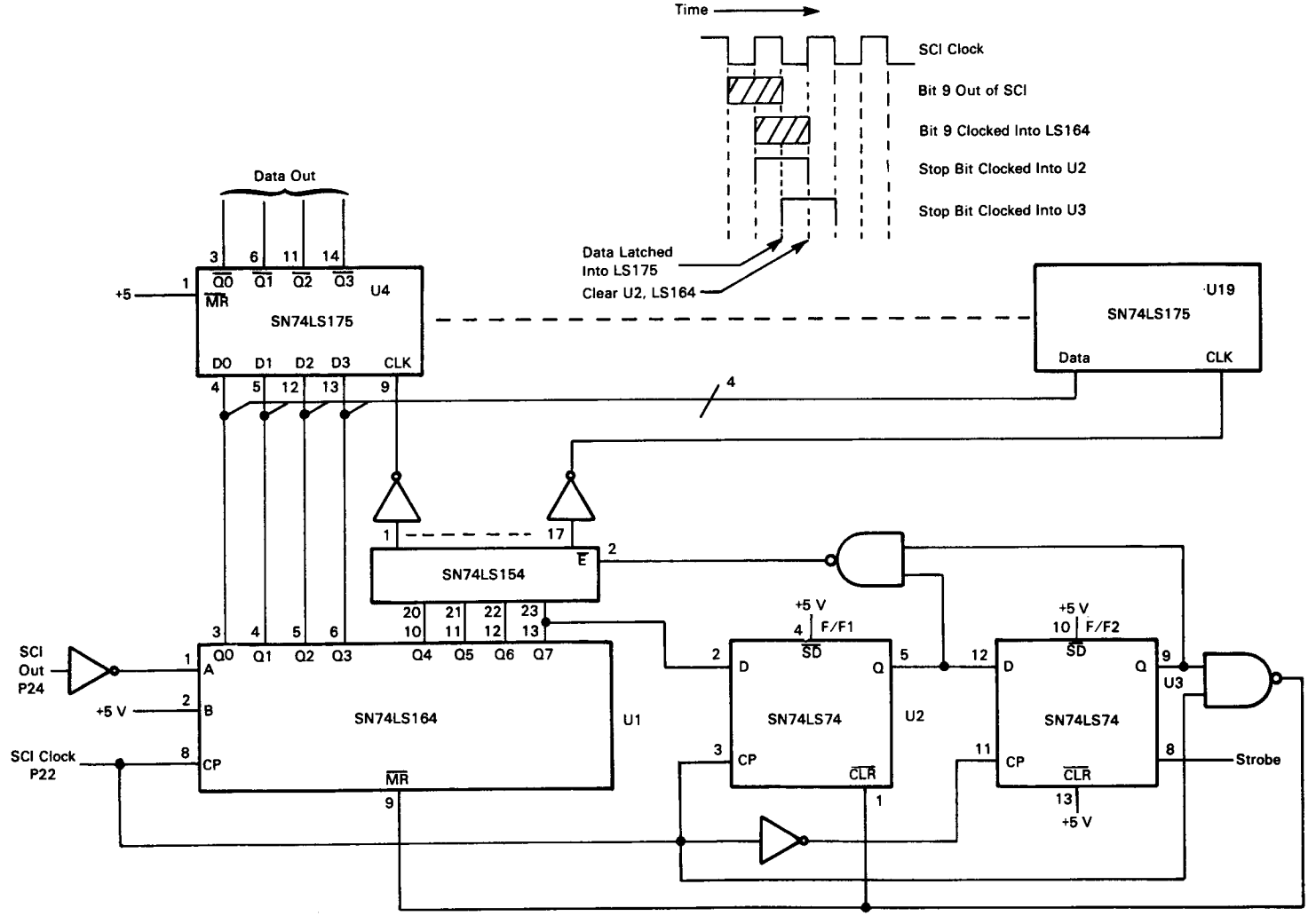
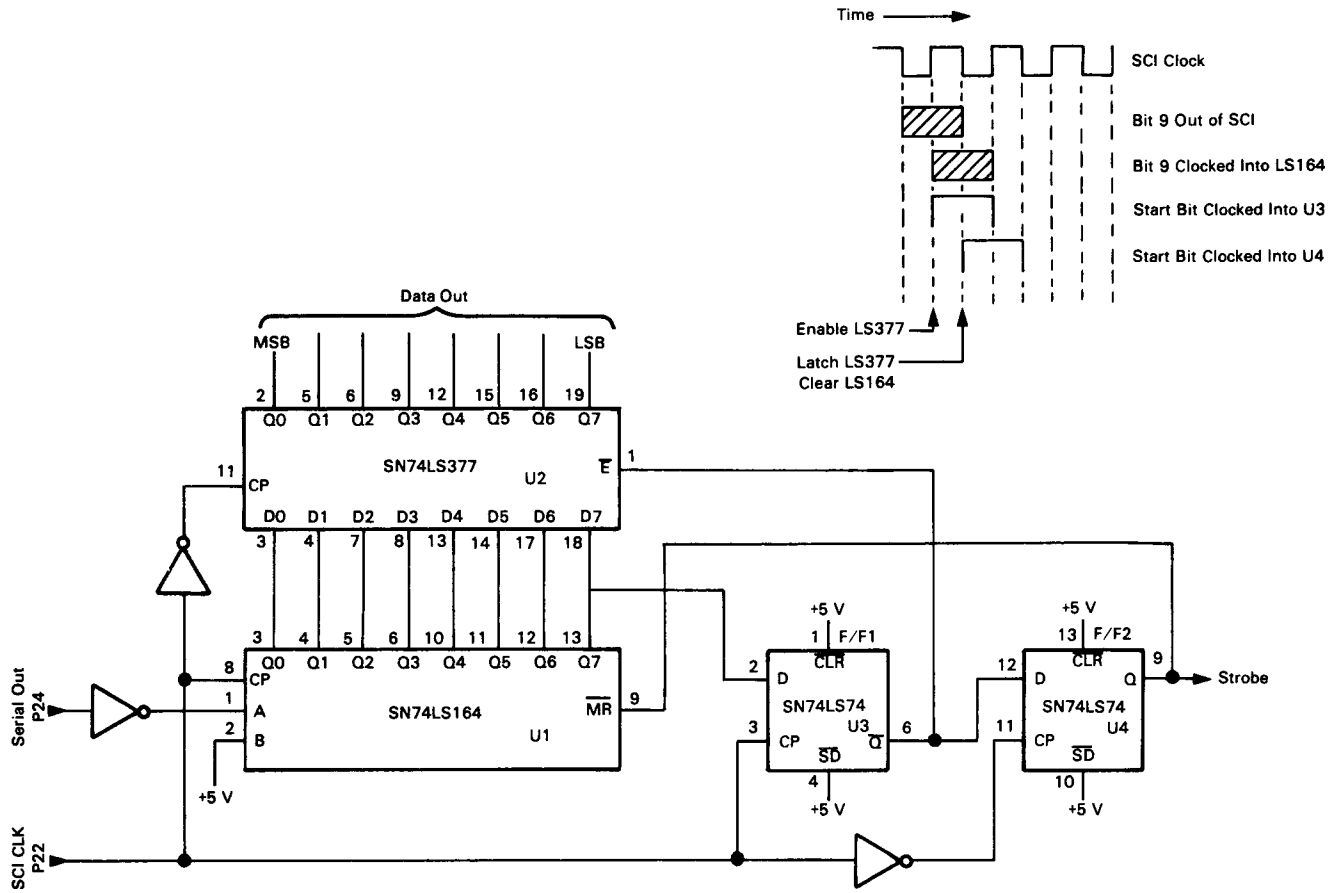


FIGURE 2 — Latched SCI Output Expansion



Note: Data Out is Inverted

FIGURE 3 — SCI Latched Port Expansion

Once again, the SCI bit stream is inverted and an idle line clocks zeros (lows) into the LS164 and LS74's. In this idle state the SN74LS377 octal "D" F/F is disabled with $\overline{E}$ high so no new data can be latched in, and the $\overline{MR}$ pin of the LS164 is held high, enabling clocking of serial input data.

When SCI data is transmitted the start bit is inverted and clocked through the LS164 as a one (high). When the start bit is clocked into the first F/F (U3), the LS377 is enabled. One-half SCI clock time later, the eight data bits in the LS164 are latched into the LS377. At the same time the start bit is clocked into the second F/F (U4) and its Q output, with appropriate propagation delay, goes low, pulling LS164 $\overline{MR}$ low, thus resetting it to all zeros. At this time the system is ready for a new SCI data byte. If the SCI line goes idle (no new SCI data bytes), the LS377 output remains unchanged.

The output of the LS377 is inverted. Non-inverted outputs can be effected by simply complementing data for MC6801/03 SCI transmission, using the appropriate "complement" op code.

SCI PORT INPUT EXPANSION

Figure 4 illustrates a parallel-to-serial interface, designed to input keyboard ASCII characters and clock the data serially into the MC6801/03 SCI port.

The SN74LS165 "serial in" line is tied high so that during an idle period (no keyboard data) 1's are clocked through the LS165 and F/F U4 into the SCI. The SCI thus sees an idle line. F/F U1 and F/F U2 are cleared at this time.

When a key is punched the keyboard strobe clocks a high into F/F U1. This high is clocked into F/F U2 on the falling edge of the SCI clock. When the SCI clock next goes high, F/FU1 and F/FU4 are cleared and LS165 (U3) $\overline{P/L}$ is driven low, latching the keyboard data. The output of F/F U4, a low, is the start bit. U2 is driven low on the next high-to-low SCI clock transition.

Data is now clocked into the SCI by the SCI clock. Ones (highs) are clocked into the SCI after the eight data bits are clocked in, indicating an idle line. At this time the interface is ready for more data.

Care must be taken to insure that "repeat" characters are not sent by the keyboard while characters are being clocked into the SCI.

MC6801 PORT 3 OUTPUT EXPANSION WITH HANDSHAKING

Port 3 of the MC6801 operated in the single chip mode can be easily expanded using SN74LS377 octal D flip-flops. Figure 5 illustrates one method of expanding port 3 to two 8-bit output ports with handshaking.

The "D" inputs of each LS377 are tied to port 3. Port 4 bit 0 (P40) is used to select one of the LS377s and deselect the other by controlling the respective $\overline{E}$ inputs.

When data is written to port 3, the port 3 strobe (OS3) clocks both LS377's. Only the selected LS377, however, will latch in the data. Nand gates are used to generate the appropriate strobe, OS3A or OS3B.

Further expansion is possible using two or more port 4 outputs for LS377 selection. Software initialization must include setting bit 4 in the Port 3 Control/Status register ($0F), so that the OS3 strobe is generated by a write to port 3.

MC6801 PORT 3 INPUT EXPANSION WITH HANDSHAKING

Input expansion of port 3 is illustrated in Figure 6 with the MC6801 operated in the single chip mode.

Initially, F/F U3 and U4 are set. When data is strobed into one of the LS374's, one of the LS74 flip-flops is also strobed, clocking its Q output low. When either LS374 is strobed, the $\overline{IS3}$ pin of the MC6801 is driven low, setting the IS3 flag in the Port 3 Control/Status Register. Setting the IS3 IRQ1 Enable bit in the Port 3 Control/Status Register enables the IS3 flag to generate an IRQ1 interrupt, vectoring the MPU to a routine for servicing port 3.

When data is strobed into port A, F/F U4 is clocked and its Q output goes low, enabling the output of U1 and making the output of U2 high impedance. When data is strobed into port B the Q output of F/FU4 remains high, enabling the output of U2 and making the output of U1 a high impedance. The Q output of F/FU4 is also tied to port 4 bit 0, programmed as an I/O input.

The MC6801 software responds to the IS3 flag by polling port 4 bit 0 to determine which port has data. The software then reads port 3 data, thus generating an OS3 strobe which sets F/F U3 and U4. The system is now ready for new data.

Software initilization must include initializing the Port 3 Control/Status Register ($0F). The IS3 interrupt enable bit (bit 6) may be set if desired. The Output Strobe Select bit (bit 4), cleared during reset, must remain cleared so that the OS3 strobe is generated by an MPU read of port 3. The latch enable bit (bit 3), also cleared during reset, must remain cleared so the port 3 latches remain transparent. Port 3 latching is external in this circuit.

Initialization should also include a read of port 3 to set F/F U3 and U4.

Measures must be taken to insure that data is not strobed into one port while data in another port is being processed. One approach is to inhibit peripheral writes to the port while the output of U5 is low, indicating that port 3 servicing is in progress. Further arbitration logic must be included if the possibility exists of data being strobed into both ports simultaneously.

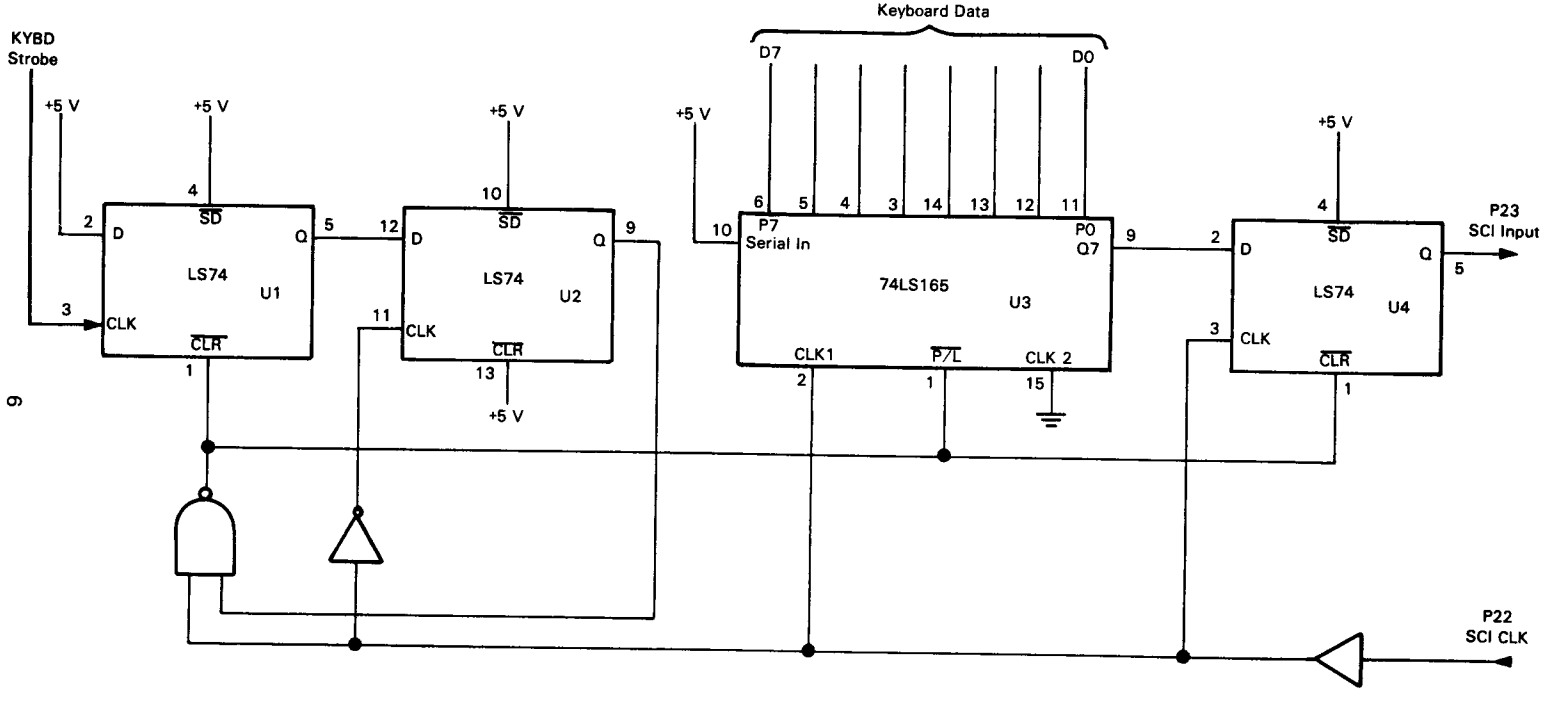


FIGURE 4 — SCI Keyboard Interface

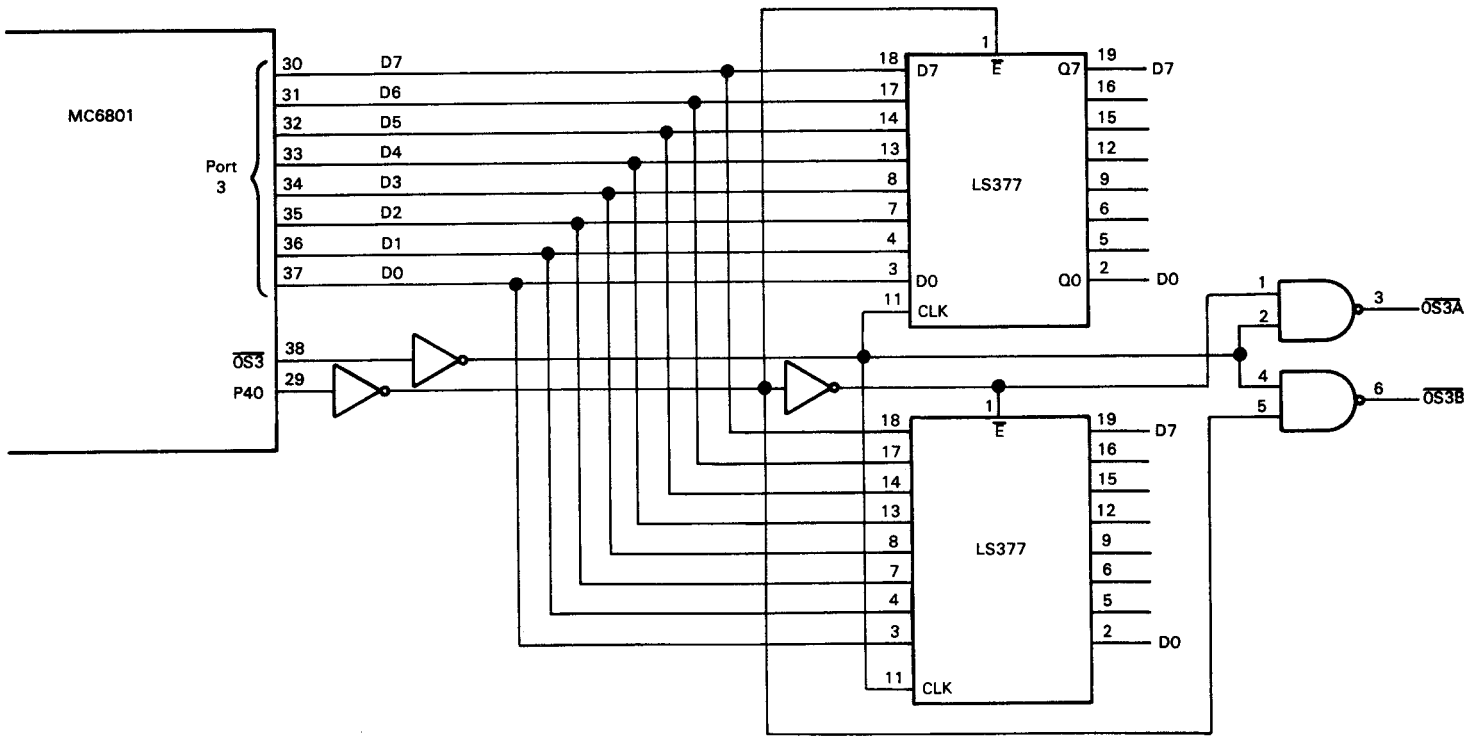


FIGURE 5 — MC6801 Port 3 Expansion (Output)

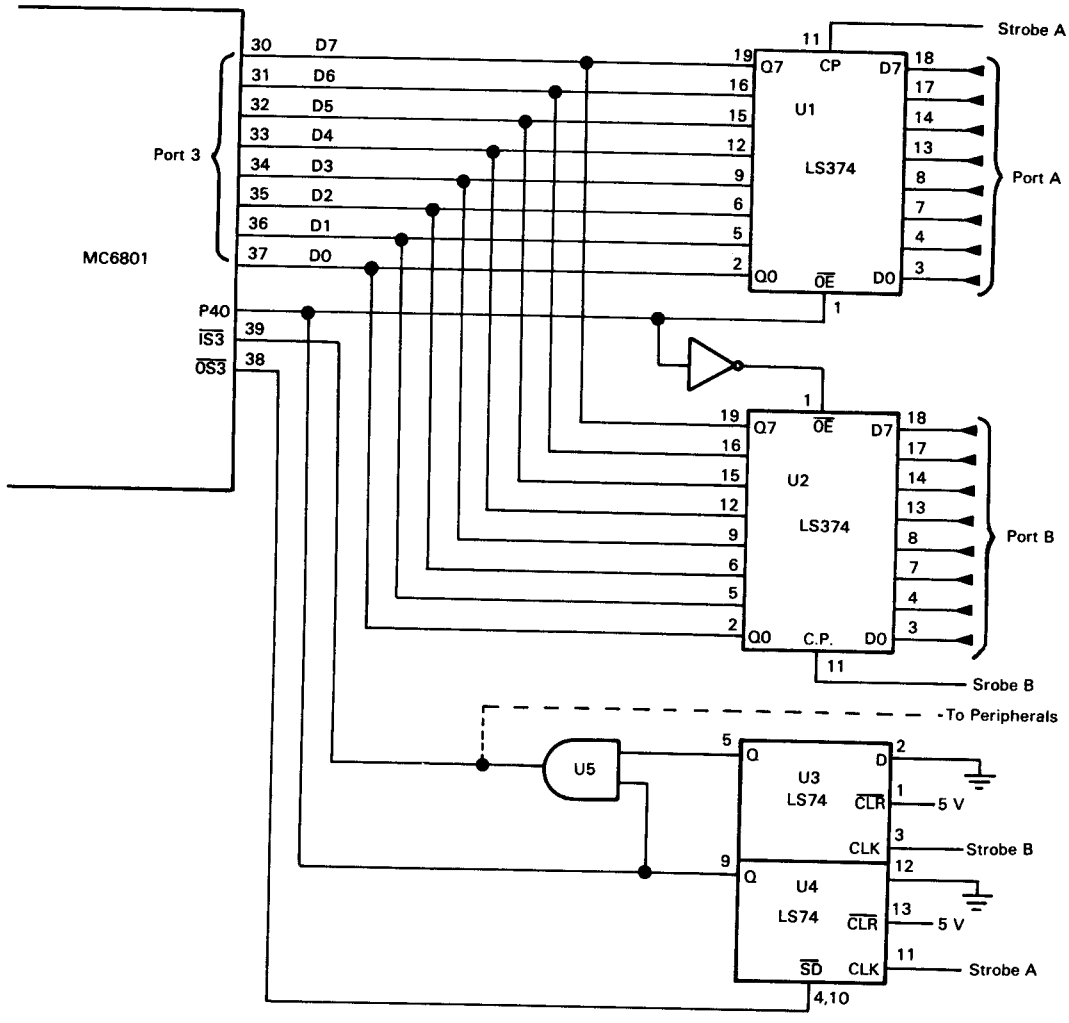


FIGURE 6 — MC6801 Port 3 Expansion (Input)