DP8459 Evaluation Board

National Semiconductor
Application Note 502
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I. INTRODUCTION

This literature describes the hardware and function of a printed circuit board for the evaluation of National Semiconductor's DP8459—All Code PLL Data Synchronizer. The purpose of the board is to assist the user of the chip in becoming familiar with the device features and in understanding its operation. The board is configured (socketed) for the 28-pin PLCC package (DP8459V) device. It contains the necessary connections and circuitry which greatly simplify the set-up of a test apparatus and facilitates the task of device evaluation.

II. CIRCUIT BOARD DESCRIPTION

Please refer to the schematic and layout captions in *Figures 1* to *4*. The circuit board layout follows the general recommendations discussed in Section 5 of the DP8459 data sheet. The entire circuit on the board can be described by the four subsections in the following text.

1. RESET FUNCTION: D1, Q1, Q2, and ½ of U1 (2-input NAND gates) form a single-shot circuit which generates a reset pulse during power-on. This signal clears the shift register, counters, and D-type flip-flops on board. Subsequently, it allows the selected STROBE circuitry control word (bits #0 to #4) and the test bit #5 to be loaded into the PLL's internal control register. The board also provides a manual reset function, which consists of switch SW-1 (SPDT momentary or toggle switch) and the remaining half of U1. It provides a reset signal while the chip is powered on.

2. LOAD AND SHIFT FUNCTION: U2 (2-input NAND gates), U3 (D-type flip-flops connected in toggle mode), U4 (8-bit parallel-in serial-out Shift Register), and U5 (divide-by-6 counter) constitute a 6-bit word programmable data generator. It issues a set of MICROWIRE™ equivalent outputs to program the control register in the PLL. U5 pin #8 is the Control Register Enable (CRE) signal. A logic LOW level allows data to be strobed into the registers. A logic HIGH level latches the register data and issues the information to the appropriate circuitry in the chip. U4 pin #9 to the Control Register Data (CRD) input shifts out a selectable 6-bit word. U3 pin #8 is input to the Control Register Clock (CRC) whose negative edge clocks the CRD pattern into the register.

3. REFERENCE FREQUENCY CLOCK: U6 (CMOS Inverter HC04) and a crystal form a stable reference oscillator which is required by the PLL for proper operation. This signal is applied to the RFC input of the DUT.

4. DIP SWITCHES: Three sets of toggle DIP switches are used to manually program the PLL input pins for the different modes of operation and for the various ranges of data rates and window strobe features.

(i) SW2—Switches #1 to #6 select the 32 combinations or steps of Early/Late window strobe position which is useful for the purpose of window skew compensation or recovery routines of marginally readable data. For normal device operation (non-test mode), the test bit (switch #6) must be set logic LOW.

The control register bit and toggle switch correspondence is shown below. Whenever the reset function is activated, the current SW2 setting is loaded into the control register. For detailed window step vs. strobe bit, refer to *Figure 4* in the data sheet.

SW2: Switches	#1	#2	#3	#4	#5	#6
Control Register Bit:	0	1	2	3	4	Test

(ii) SW3—The top three switches are used to select the VCO frequency range via the Range Select pins RS0, RS1, and RS2. The fourth switch is not used. The relative VCO frequency versus the 3 bit code is tabulated below:

Switch			VCO Range
#3 RS2	#2 RS1	#1 RSO	
1	1	X	0.50 MHz–1.25 MHz
1	0	1	1.25 MHz–2.5 MHz
1	0	0	2.5 MHz–5.0 MHz
0	1	1	5.0 MHz–10.0 MHz
0	1	0	10.0 MHz–20.0 MHz
0	0	X	20.0 MHz–48.0 MHz

Important—If the desired VCO frequency is located at the boundary of 2 ranges (overlapping), select the range which places that frequency at the higher end of the spectrum, (e.g. Fvco = 20.0 MHz, choose RS code = 010). This will optimize the performance of the chip.

(iii) SW4—The functions of the 8 switches are detailed as follows:

Switches #1 to #3 control the Frequency Lock Control (FLC). At most one and only one of the 3 switches should be engaged or closed.

Switch #1 closed—FLC connects to PDT

Switch #2 closed—FLC connects to RG

Switch #3 closed—FLC connects to GND

Switches #4 and #5 program the Sync Pattern Select Pins SP0, SP1 for the internal divider modulus to detect either the 1T, 2T, 3T, or 4T preamble pattern. (T = VC0 period; e.g. 3T = 100100...preamble).

Switch		Sync Matching Divider Modulus M
#5 SP1	#4 SP0	
0	0	1
0	1	2
1	0	3
1	1	4

Switches #6 to #8 control the High Gain Disable (HGD) pin. Again, only one of these 3 switches should be closed at any time.

Switch #6 closed—HGD connects to GND

Switch #7 closed—HGD connects to RG

Switch #8 closed—HGD connects to PDT

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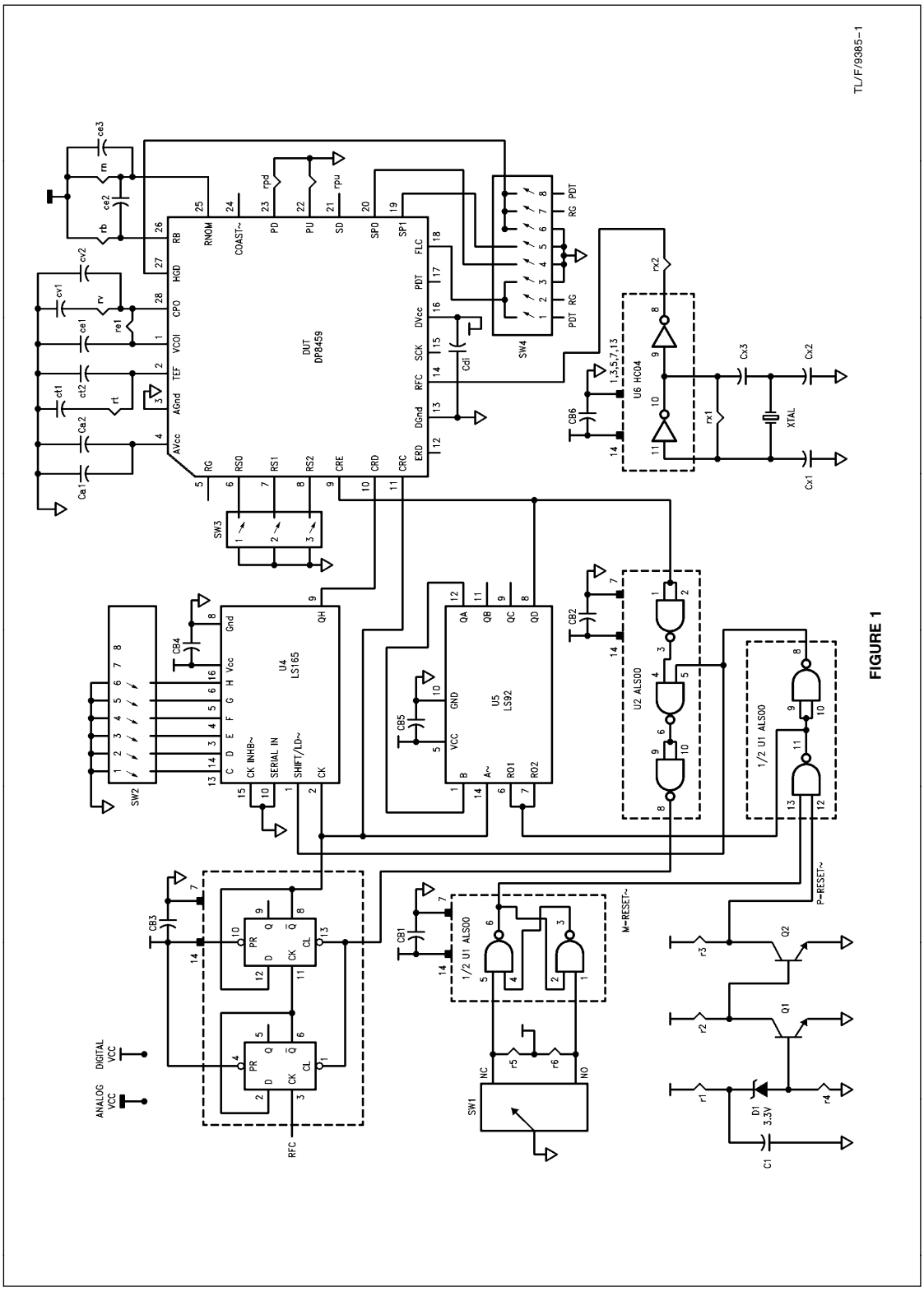
TL/F/9385–1
DUT
DP8459
U4
LS165
U5
LS92
U6 HC04
U2 ALS00
1/2 U1 ALS00
SW1
SW2
SW3
SW4
XTAL
D1
3.3V
ANALOG VCC
DIGITAL VCC
RFC
M–RESET~
P–RESET~

FIGURE 1

III. TEST HARDWARE

1. EXTERNAL COMPONENTS: All integrated circuits are socket mounted to make it easy for the purpose of interchange or replacement. Passive components for the loop filters, charge pump resistors, and the crystal oscillator sections are also provided with sockets to facilitate alteration of components for different data rates.

2. POWER SUPPLY: Three separate supply terminals are provided on board. One ties to the Analog V_{CC} and a second ties to the Digital V_{CC} of the PLL chip. A third post makes connection to the rest of the digital support circuitry. Normally two +5V supplies are used, one to supply the V_{CC} pins of the PLL device under test, another to power the support circuitry. It should be noted that in order to take advantage of the power on reset function, the power of the PLL chip must be turned on first, then apply power to the support circuitry.

3. ENCODED READ DATA (ERD) AND READ GATE (RG): A word pattern generator is a convenient signal source to provide the desired TTL logic level signals to these inputs.

4. LOOP FILTER COMPONENTS: Normally components "Re1" should be replaced by a short-circuited connection and "Ce1" should be open-circuited for a second order loop filter implementation. These optional components are intended for higher order filter realization.

IV. DP8459 EVALUATION BOARD PARTS LIST: (10 Mbit/s 2, 7 code operation)

DUT = DP8459 (PLCC package)
U1 = 74ALS00
U2 = 74ALS00
U3 = 74ALS74
U4 = 74LS165
U5 = 74LS92
U6 = 74HC04

D1 = Zener Diode (Vz = 3.3V)
Q1 = 2N2369 (NPN)
Q2 = 2N2369 (NPN)

Xtal = 20 MHz

SW1 = SPDT Momentary Switch
SW2 = 16-Pin DIP Toggle Switch
SW3 = 8-Pin DIP Toggle Switch
SW4 = 16-Pin DIP Toggle Switch

Bypass Capacitors:
Cb1 = 0.1 μF
Cb2 = 0.1 μF
Cb3 = 0.1 μF
Cb4 = 0.1 μF
Cb5 = 0.1 μF
Cb6 = 0.1 μF
Ca1 = 0.1 μF
Ca2 = 1000 pF
Cdi = 0.1 μF

Loop Filters:
Ct1 = 0.05 μF
Ct2 = NC*
Rt = 68Ω
Cv1 = 0.022 μF
Cv2 = 510 pF
Rv = 150Ω

Crystal Oscillator:
Cx1 = 22 pF
Cx2 = 100 pF
Cx3 = 56 pF
Rx1 = 1 MΩ
Rx2 = 100Ω

Other External Components:
Ce1 = NC*
Re1 = Short Circuit It
Rn = 2.4 kΩ
Rb = 2.4 kΩ
Ce2 = NC*
Ce3 = 1000 pF
Rpu = 510Ω
Rpd = 510Ω

Reset Circuitry:
R1 = 2 kΩ
R2 = 10 kΩ
R3 = 10 kΩ
R4 = 10 kΩ
R5 = 1 kΩ
R6 = 1 kΩ
C1 = 10 μF

*NC means no component required there (leave nodes open).

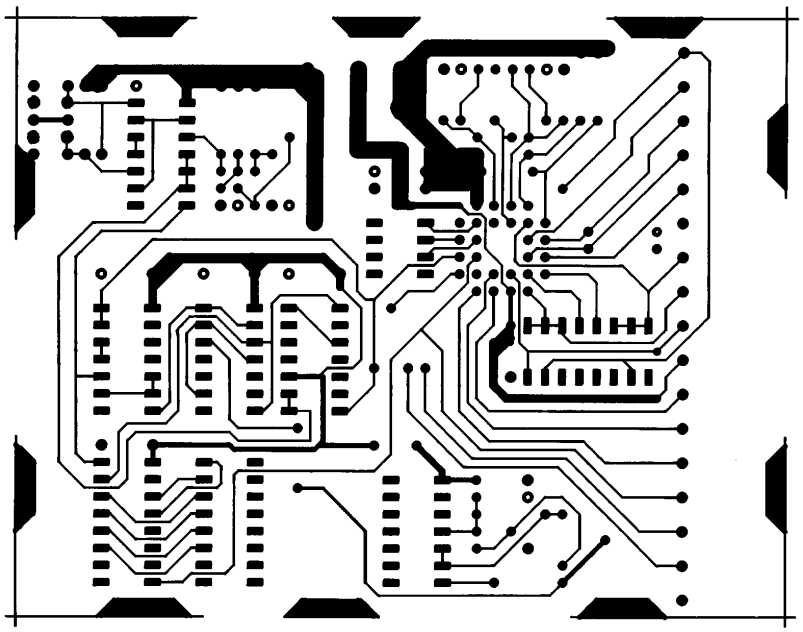

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FIGURE 2. Trace Side (Bottom View)

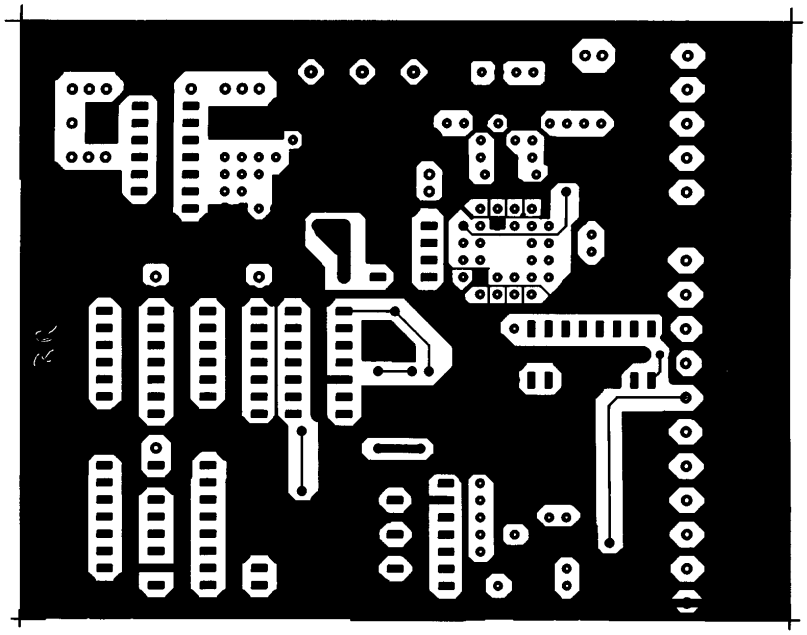

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FIGURE 3. Component Side with Ground Plane

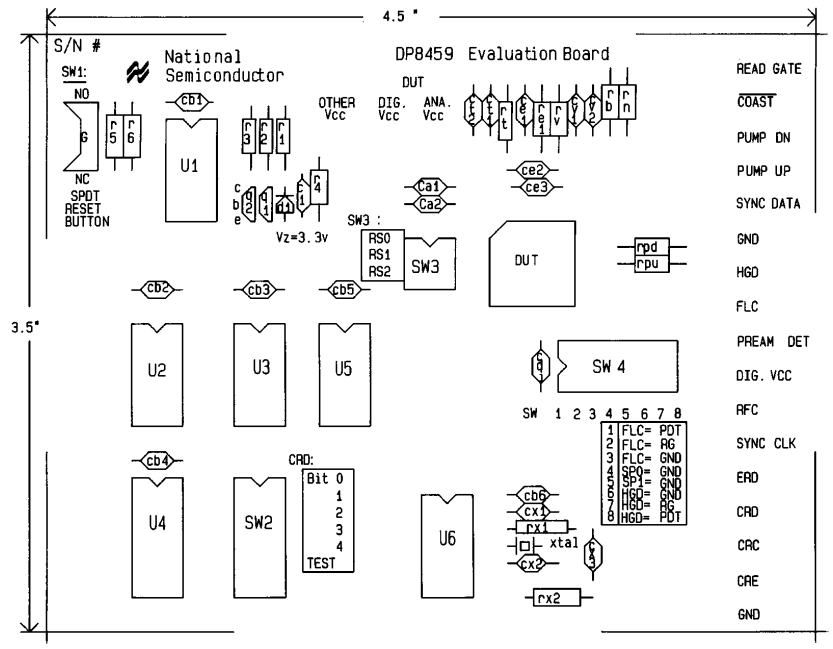

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FIGURE 4. Component Location (Top View)

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