DP8459 Window Strobe Function

National Semiconductor
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INTRODUCTION

This note explains in detail the Strobe Function incorporated on the DP8459 ALL-Code Data Synchronizer. It is recommended that the reader reviews the data sheet prior to reading this note. The Strobe Function within the DP8459 chip is considerably more intricate and versatile than any existing Strobe Function on commercially available data synchronizers, thus, this application note is intended to point out the significance of this device feature and to convey important information on the proper use of it. It is also the intent of this writing to offer an explanation on the concept of Strobing and associated terminology for customers who may not be familiar with the subject. Further, the ease with which the Strobe Function can be employed to optimize system performance and to realize cost effective manufacturing of products is discussed.

DESCRIPTION

The Strobe Function implemented in the DP8459 chip provides a powerful and convenient means for the synchronization window to be shifted either Early or Late with respect to its nominal position. By definition the Strobe step, t_S is the digitally programmable time displacement of the (DP8459) synchronization window from its nominal position and is expressed as:

$$t_S = M \times (1.8\% \times t_{VCO})$$

where ''M'' is the value of the Strobe control word, having a range from -15 to $+15$. The fine resolution of the individual strobe step (LSB) in conjunction with the thirty-one steps of movement provided by the DP8459 is unprecedented among commercially available devices, which have at most a few fixed strobe positions if any at all. The strobe control word, ''M'', is set by five of the six binary bits within the Control Register as shown in *Figure 1*. Bit #4 is the sign bit which determines Early or Late strobe movement. The last bit (#5) in the control word is the test bit, which when set to high is used for factory testing. This bit is always the first bit serially loaded into the shift register. The following truth table (refers to Table I) maps ''t_S'' to the corresponding Strobe word representations.

TABLE I. Window Strobe Truth Table

Strobe Bit 4	3	2	1	0	Strobe Word M	Window Strobe t_S (Typical)
0	1	1	1	1	−15	$-0.270 \times \tau_{VCO}$
0	1	1	1	0	−14	$-0.252 \times \tau_{VCO}$
0	1	1	0	1	−13	$-0.234 \times \tau_{VCO}$
0	1	1	0	0	−12	$-0.216 \times \tau_{VCO}$
0	1	0	1	1	−11	$-0.198 \times \tau_{VCO}$
0	1	0	1	0	−10	$-0.180 \times \tau_{VCO}$
0	1	0	0	1	−9	$-0.162 \times \tau_{VCO}$
0	1	0	0	0	−8	$-0.144 \times \tau_{VCO}$
0	0	1	1	1	−7	$-0.126 \times \tau_{VCO}$
0	0	1	1	0	−6	$-0.108 \times \tau_{VCO}$
0	0	1	0	1	−5	$-0.090 \times \tau_{VCO}$
0	0	1	0	0	−4	$-0.072 \times \tau_{VCO}$
0	0	0	1	1	−3	$-0.054 \times \tau_{VCO}$
0	0	0	1	0	−2	$-0.036 \times \tau_{VCO}$
0	0	0	0	1	−1	$-0.018 \times \tau_{VCO}$
0	0	0	0	0	0	0
1	0	0	0	0	0	0
1	0	0	0	1	1	$0.018 \times \tau_{VCO}$
1	0	0	1	0	2	$0.036 \times \tau_{VCO}$
1	0	0	1	1	3	$0.054 \times \tau_{VCO}$
1	0	1	0	0	4	$0.072 \times \tau_{VCO}$
1	0	1	0	1	5	$0.090 \times \tau_{VCO}$
1	0	1	1	0	6	$0.108 \times \tau_{VCO}$
1	0	1	1	1	7	$0.126 \times \tau_{VCO}$
1	1	0	0	0	8	$0.144 \times \tau_{VCO}$
1	1	0	0	1	9	$0.162 \times \tau_{VCO}$
1	1	0	1	0	10	$0.180 \times \tau_{VCO}$
1	1	0	1	1	11	$0.198 \times \tau_{VCO}$
1	1	1	0	0	12	$0.216 \times \tau_{VCO}$
1	1	1	0	1	13	$0.234 \times \tau_{VCO}$
1	1	1	1	0	14	$0.252 \times \tau_{VCO}$
1	1	1	1	1	15	$0.270 \times \tau_{VCO}$

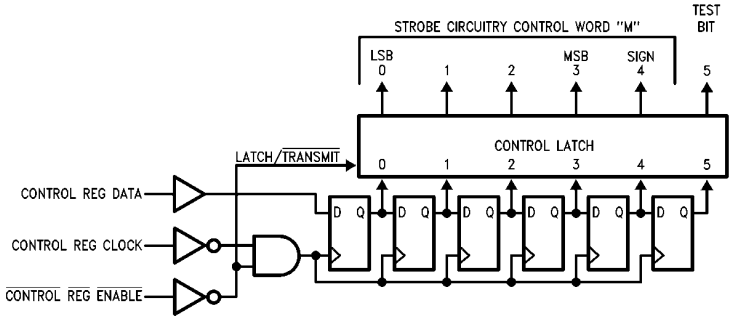

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FIGURE 1. Strobe Control Register Diagram

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The Strobe Function is also referred to as Window Strobe, because strobing is used to adjust the relative position of the synchronization window. To better illustrate the relationship of strobe to the synchronization window, please refer to *Figure 2a*. This diagram depicts the concept of synchronization window. The synchronization window is defined as a continuously repeating time cell, which has a nominal time span equal to the period of the VCO. Ideally, an Encoded Read Data pulse will be captured and correctly interpreted regardless of its position within the window boundaries. However, the ideal window width cannot be realized in practice, due to noise and device non-idealities such as VCO jitter. Thus, a small fraction of the usuable window is truncated, leaving a correspondingly narrower available window width. If device mismatch and other asymmetric phenomena are also present, another window eroding phenomenon called window shift results. This phenomenon causes the average data window center to shift with respect to the expected mean bit position. Referring to *Figure 2b*, note that the static window width in this case appears congruent to that in *Figure 2a*. However, early shifted data bits in *Figure 2b* actually have a greater probability of falling outside the window since it is shifted late. The Strobe function is a simple to use, yet powerful feature which, as will be explained later, allows the user to offset, within ½ LSB, the undesirable window shift and improve system performance.

Synchronization Window Diagram

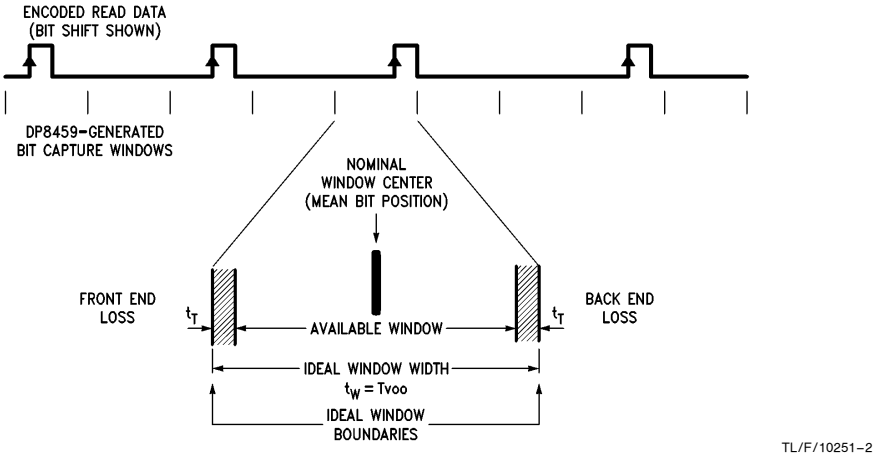

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FIGURE 2a. Synchronization Window

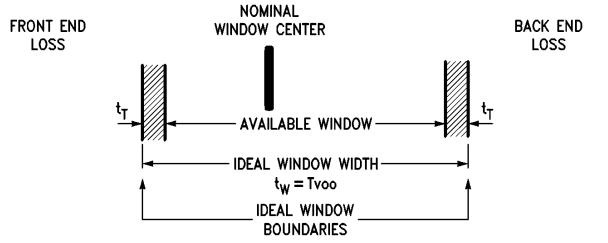

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FIGURE 2b. Window Shifted Late

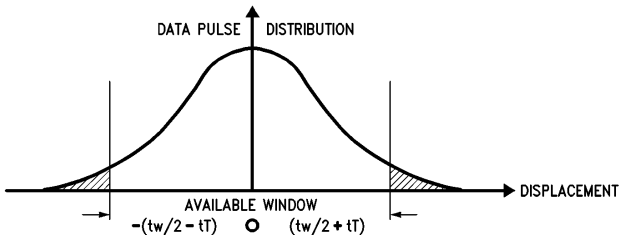

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FIGURE 2c. Bitshirt vs Probability of Its Occurrence

BYPASSING STROBE FEATURE

To fully harness the Strobe feature as in an intelligent interface environment, the MICROWIRE™ bus may be interfaced to a processor or controller function to program the internal control register during initialization or between read operations. The information stored in the control register, bits #0 through #4, defines the amount and sense of window displacement. (Important, bit #5 must be set to "0" for normal operation, since a "1" at this location will place the chip into a test mode used during production testing.) A typical system diagram with the MICROWIRE bus is shown in *Figure 3*.

If the customer does not wish to use the Strobe feature (strobe word may be fixed at the nominal setting of all bits equal to 0), the MICROWIRE bus can be bypassed. By appropriate hardwiring of the control register inputs, as depicted in *Figure 4*, the control register content is always set to the nominal strobe upon Read Gate assertion. Please note that the window truncation is not specified at the "Nominal" Strobe setting. Therefore, optimum window performance may not be realized at this setting. This and similar device configurations are usually employed when the prime interest is to construct a simple setup for general device evaluation purposes. Of course it can also be used in lower data rate systems and, particularly, in tape and floppy drives where the window margin requirement is generally less stringent.

Although the technique just described can serve as a convenient means to set the control register content, it is very important to note that it requires the user to correctly sequence the Read Gate. For example the chip must be powered up in the non-read mode, this is with Read Gate low. Since Read Gate is tied to the "CRE" pin, a logic low enables the shift register portion of the control register to serially enter data while the control latch is held in its previous state. Concurrently, the E.R.D. pulses must be present which serve as clock pulses to shift the all "zeroes" data. Finally, the Read Gate must then be switched to the high state, thus inhibiting data entry into the shift register and allowing the new data just entered into the shift register to be transferred to the latch. Whether loading the control registers with the method as shown in *Figure 4* (this diagram represents a typical system setup where the RG also controls the HDG and CRE pins) or employing the same scheme via external circuitry, if the Read Gate is tied to CRE, the synchronizer chip must be powered up with Read Gate low. After the control data has been loaded, Read Gate must be set high. (The need to pulse the Read Gate was not mentioned in the March 1988 datasheet).

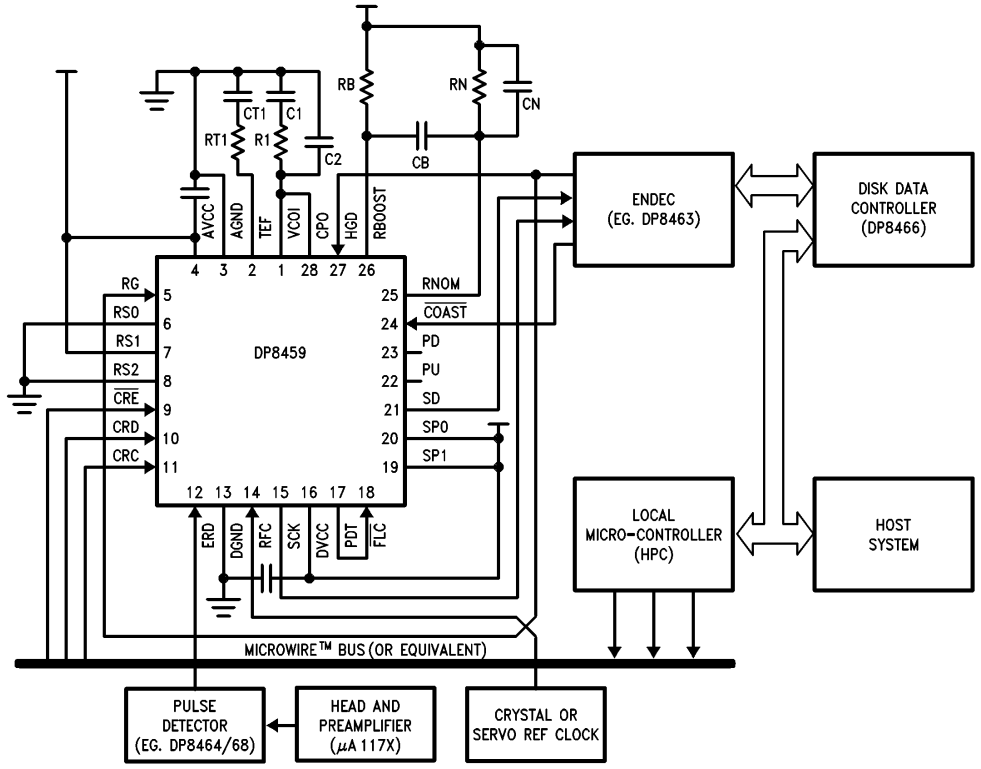

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FIGURE 3. Typical System with the MICROWIRE Bus

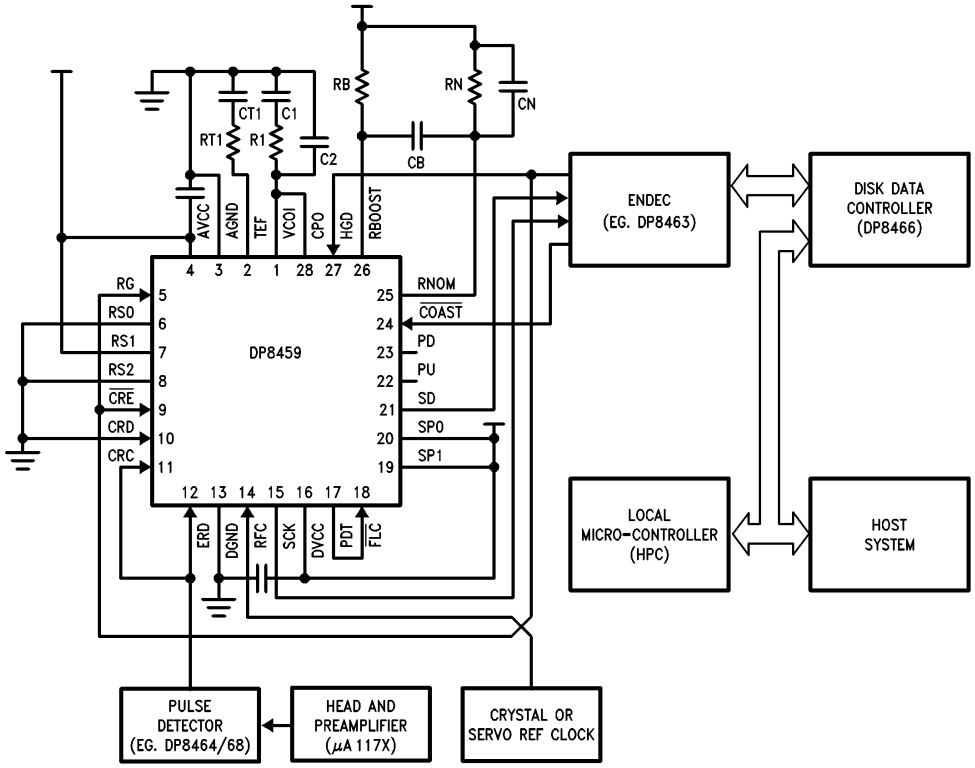

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FIGURE 4. Typical System without the MICROWIRE Bus

WINDOW TRUNCATION SPECIFICATION

The Strobe function is also used to qualify the window truncation specification. For example, the DP8459 half-window loss, "t_T", represents the sum of static window truncations from all relevant circuits and mechanisms in the data synchronizer, e.g. window shift, VCO jitter, etc. At 10 Mb/s, "t_T" is specified as 3.0 ns (6% of VCO period) maximum with M $= -2$. If the strobe is not used, i.e. M $= 0$, then "t_T" maximum would typically be 4.8 ns. This, however, is not tested and therefore not guaranteed.

The static window truncation consists of two separate major contributors to window loss, namely "T_S" (which is due to window shift) and "T_N" (which is truncation due to noise and other relevant mechanisms). The window strobe feature can be used to minimize "T_S" to ½ LSB of the strobe step. At 10 Mb/s "T_S" can be minimized to typically 0.45 ns. The remaining loss is due to "T_N".

The DP8459 window specifications are valid over the entire operating temperature and power supply ranges per datasheet. Thus the window specification "T_T" is actually comprised of "T_N", "T_S", temperature guardbanding, and measurement system guardbanding. The "t_T" parameter is tested at 4.75V V_{CC} and 5.25V V_{CC}. The device is checked at 10 Mb/s and 20 Mb/s data rates for window specification compliance as part of the final test in manufacturing. It should be noted that the data sheet recommended strobe position settings are determined by statistical averaging of many units during device characterization. In high performance drive system applications, users can take advantage of this Strobe feature to individually "tune" the synchronizer for optimal detection window symmetry.

STROBE FUNCTION

There are several reasons why one wishes to alter the inherent average window position generated by the phase-locked oscillator within the synchronizer. First, the average data window position may not be perfectly centered about the expected mean data bit position. Second, deliberately skewing the window position can serve to recover malshifted data bits. Third, shifting the window can introduce excessive error rate for testing and calibration purposes.

There could be a substantial amount of random displacement (jitter) of individual bits dependent on the design of the read/write head, media, signal processing electronics, and the result of bit interaction. This is exemplified in *Figure 2c*, which shows that the data bit displacement (also known as bitshift) versus its probability of occurrence is a Gaussian distribution. In bitshift theory, total bitshift refers to the movement of the magnetic transitions with respect to the position where they are recorded. There are three dominant factors which contribute to the loss of window margin, i.e. the difference between the farthest shifted bit and the actual window boundary. The intersymbol interference, which is a function of recording components and code used, the pulse detector imperfection, which is primarily caused by

equalization and differentiation errors, and the phase locked loop accuracy, which involves its inherent window skew and jitter. The first two contribute to bitshift while the last one reduces the effective window width. Fortunately, the fraction of window loss due to the PLL window skew can be substantially nullified, and excessive bitshifts may be compensated during read mode via the strobe function in high performance data synchronizers such as the DP8459.

The first three LSBs of the Strobe Control Word produce strobe steps that have shown to track quite well with respect to the predicted values. For example, at 10 Mb/s data rate, typical characterization data indicates less than one nanosecond deviation between the measured strobe readings and the corresponding calculated strobe values. The data is taken with the Strobe Control Word range from M = 0 to M = ±6 and with the chip operating at 4.75V V_{CC} and 5.25V V_{CC}. It is recommended that this strobe range (M = 0 to M = ±6) be used for applications requiring relatively accurate strobe step control, such as for window alignment, data recovery, and window margin test. The higher strobe ranges are not as accurate due to the cumulative error when more bits of the control word are turned on. Thus for $|M| \geq 7$, this range is perhaps more suitable for inducing excessive soft errors in system analysis and experimentation purposes. System designers can thus perform real time system optimization studies to identify and to correct anomalies within the read channel chain. For example, after creating a significant amount of soft errors, any component within the read channel may be changed or modified to determine if error reduction can be achieved.

DESIGN CONSIDERATIONS

It is important to note that changing the strobe setting requires a finite response time of the control circuitry. In addition to the time required to load the 5-bit Strobe Control Word to the internal register the user must account for the settling time associated with any change of the strobe. This is a function of the Timing Extractor Filter (TEF) components and the data rate at which the data synchronizer is being operated. It is highly recommended that any change to the strobe setting be done with the Read Gate deasserted and with sufficient time allowed for settling prior to the initiation of another read sequence.

The Time Extractor Filter is used in a second PLL, the reference phase-locked loop, within the chip. This loop stably locks to a crystal reference oscillator (or a servo derived) frequency reference and it is responsible for producing a delay time of exactly one-half of the VCO period. Via this delay, the synchronizer data window is accurately centered about the mean bit position such that optimal capturing of the data becomes possible in the presence of jittery data pulses. Furthermore, strobing, which modifies the one-half VCO period delay, is achieved by programming a small amount of change in current (sourcing or sinking) to the current controlled oscillator of the reference phase-locked loop.

The VCO circuit of the reference PLL is constructed identical to that of the primary PLL. To prevent VCO frequency-control-voltage runaway in the primary loop, a comparator circuit is connected between the two loops to sense when the primary oscillator current crosses thresholds, which are placed 50% above and below the reference current. (Please refer to the simplified block diagram in *Figure 5*.) If

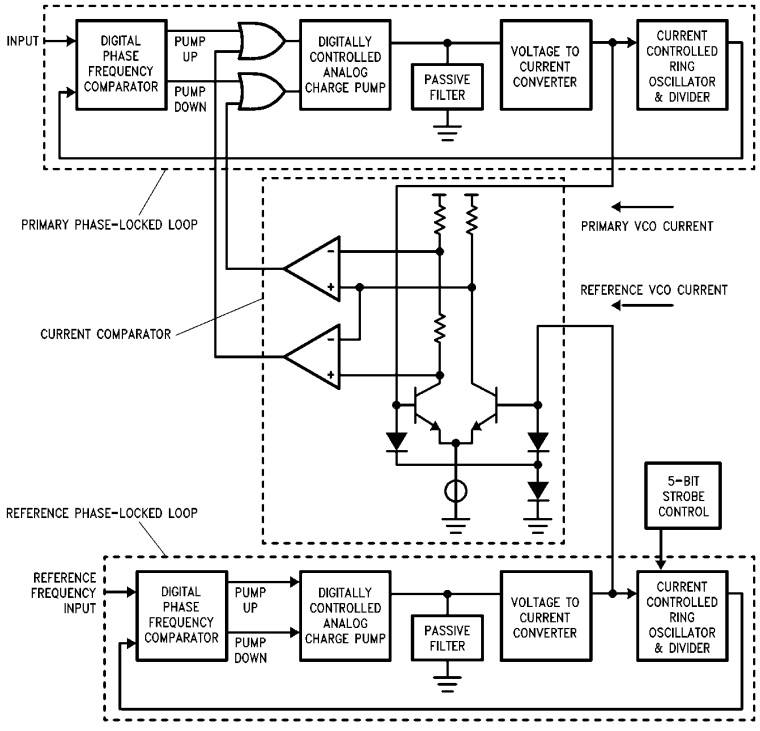

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FIGURE 5. Reference and Primary PLLs within the DP8459

either one of the preset threshold is crossed, the comparator directs a correction signal to the primary PLL and limits further excursion of its VCO control voltage.

Since the reference PLL is part of the feedback loop that regulates the primary PLL, the Time Extractor Filter components also affect the synchronizer performance, but not the strobe step amount. In the (March 1988) DP8459 datasheet, *Figure 10*, presents a table of the estimated settling times due to a phase step for different (TEF) loop component values operating at various data rates. The calculated numbers in that table reflect the idealized settling time of the reference PLL block only. Assumptions made in the calculation, as empirical data was not available at the time of the publication, were no initial frequency offset, the values of the loop gain and the loop's natural frequency were approximately equal, and the effect of any parasitic conditions were neglected. Current lab data shows the TEF settling time from a maximum strobe movement (a step from M = −15 to M = +15) is nearly 15 times longer than the figures projected in the datasheet. [i.e. at RFC = 10 MHz, T_{SETTLE} ≅ 290 μs (measured) instead of 19.6 μs as predicted; and at RFC = 20 MHz, T_{SETTLE} measured is approximately 140 μs versus 9.6 μs as calculated.] In practice it is expected that customers would normally use the strobe range of |M| ≤ 6 for reasons as mentioned in the previous section. Typical lab data for a strobe movement from M = −6 to M = +6 are also included here for reference: with RFC = 10 MHz, T_{SETTLE} ≅ 130 μs and at RFC = 20 MHz, T_{SETTLE} ≅ 54 μs.

Complete settling of the synchronized outputs at the primary loop may require slightly longer time. Although this settling time can be substantially reduced by either raising the bandwidth of the TEF or increasing the damping of the filter via RT1, this usually degrades the static window margin (by up to a few percent of the ideal window width). Since the window margin is an important parameter, it should not be compromised with the settling time. In a multi-data rate system it is recommended to employ the TEF components associated with the lowest data rate. In general the TEF settling time is not a critical parameter except perhaps for test time considerations when multiple strobing is involved (i.e. in margin testing in the production line). Other than the highest performance and the fastest systems, the latency time due to such system factors as soft-sectoring, command instruction delays, error correction/retrys, etc. in typical hard disk storage drives may be much longer than the TEF settling time. Therefore changing strobe settings from sector to sector is not practical in many hard disk environments. It is advisable that even for systems that are not limited by their latency time between read executions to allow a minimum of one revolution time (16.7 ms) between strobing. It should be mentioned also that the customer who wants to change the TEF settling time must observe stability criteria as in any PLL system.

APPLICATIONS

Individual "Trimming" of the PLL

For mass storage systems operating at low data rates (e.g. 5 Mb/s or less), two or three nanoseconds of window loss due to skew may be an acceptable specification. But, at higher data rates, storage systems can not tolerate such figures. As mentioned in the previous section, a portion of the window loss is ascribed to window skew. Although most of this loss may be recovered, undertaking the trimming of the synchronizer block is often an unpleasant manufacturing issue; presently this involves a technician in the assembly line adjusting a potentiometer while monitoring an oscilloscope. In high performance drives it is always desirable to regain as much margin as practical in production. The ability to perform in-system window deskewing is an extremely attractive attribute because it can attain the potential window margin available by optimizing each drive individually. It should be noted that this is superior to having the PLL chip statically adjusted prior to system integration. Of course such an in-system trimming procedure usually tags on a relatively high premium, such as added cost of time, labor, and material. Other than discrete designs, monolithic PLL devices generally afford limited or no adjustment to nullify window skew. The DP8459 synchronizer's Strobe feature presents a viable solution to perform window adjustment easily and inexpensively. The digitally controlled strobing within the chip allows "trimming" of the detection window without the need to "tweak" any external components. As mentioned, its 5-bit resolution strobe function makes it possible to deskew the inherent window offset with subnanosecond precision at 10 Mb/s and higher data rates.

Window Centering Algorithm

Truncation due to inherent window shift can be mostly nullified via the window strobing technique. Hence, an intelligent drive system can greatly benefit from the DP8459 Strobe feature because a window centering algorithm can be installed with no extra hardware or adjustment required. Moreover, the task of window deskewing can be readily automated with the DP8459 via the MICROWIRE bus. For example, some of the industrial interface standards such as the Rev-2 "ESDI" interface standard already supports a 4-step Early/Late strobe option in the command level, independent of the strobe step size to be implemented. The following describes a strobing alogorithm that can be employed for window centering.

A typical window centering routine should establish some higher than nominal error rate thresholds by strobing the data window in the early direction, then repeating the same process in the late direction. The early and late strobe settings which yield the equivalent error distribution are then stored. From the strobe excursion information, the window center skew can thus be determined and the appropriate strobe word is set to correct the window skew. To implement an effective routine one should employ a periodic test pattern such that the average decode window is made more stable. The system error rate can be deliberately made more responsive if some constant (time independent) source of window degradation functions such as maximum bit crowding or reduced signal to noise ratio is introduced during testing, i.e. performing the test at the inner recording cylinders of the Winchester type disk drive. Such a routine could execute during system power-up and produce optimal centering of the window. The system would function like having a built-in tester to perform window auto-calibration at power up or at any scheduled maintenance interval.

Data Recovery

Another valuable application of the DP8459 Strobe function is to service error-bound data recovery. Infrequently, the need arises to rescue vital, but marginally recorded, data

information from a removable data cartridge, and in particular from a (magnetically) damaged or defective storage module. Usually, such an operation requires repetitively reading through one block of data at a time and exhaustively shifting through some range of window strobe steps in an attempt to correctly retrieve the data of interest. However, employing the DP8459 in conjunction with a suitable data retrieval algorithm, could offer any mass storage system a powerful tool for speedy recovery of error-bound data. The DP8459 device is capable of delivering typically a 1.8% window shift resolution, furthermore, its thirty-one steps of strobe setting is programmable via the MICROWIRE bus. Such features make it possible to incorporate sophisticated utility programs such as one for data recovery.

Window Margin Test

The technique of Strobing employed in window margin testing is not a new practice. Shifting the detection window is one of two acceptable means to ''marginalize'' the window (modify the VCO generated data window) for checking the merit of the read channel. Although it has been gaining popularity in the test equipment sector, the theory behind it may be unfamiliar to some drive users and manufacturers alike. Window margin testing is an extension of the window centering process as discussed above. Please refer to Appendix A for a discussion of window shifting and window narrowing techniques in error-rate analysis.

Window strobing can be a very time-saving method to analyze the drive system's error rate characteristics. Unlike conventional testing, it does not consume hours to transfer data and to perform data integrity comparison. Hence, the DP8459 Strobe Function is very convenient for this purpose. For example, in a manufacturing environment, a new data storage drive system will be thoroughly characterized for its error rate profile with independent test techniques. Then it will be followed by a series of window shift induced error rate tests. The accelerated error rate profile thus generated is next compared to those produced from other test methods. Error distribution, statistical correlation, and acceptable thresholds are thus established. In production then, the correlated error rate figures and their corresponding Strobe settings are stored permanently in the memory of the drive/system during final checkout. These statistics are subsequently utilized as criteria for performance acceptance or rejection such as in QA and incoming inspections. Furthermore, systems in the field can be routinely interrogated for their current window margin status.. This, for example, can take the form of an embedded system maintenance routine to reduce the potential hazard of an unexpected system crash predicament. An effective window margin diagnostic test routine should employ the most bitshift sensitive test pattern and operate at the maximum bit crowding region of the media.

SUMMARY

The Window Strobe feature of National's latest PLL data synchronizer chip, the DP8459, has been presented along with the background information necessary for its utilization. The versatility and power embedded in this digitally controlled Strobe function is unparalleled. Although the prime intent of strobing is to deskew the inherent window asymmetry thus improving the device window margin, it also lends itself to a host of important system applications. They include in-system calibration of window centering which also allows adjustment of the individual drives to maximize their performance margin; system window margin analysis in design optimization and system maintenance; and data recovery on damaged media without the need of dedicated test equipment. The DP8459 strobe feature provides an economic and reliable solution to enhance the value and performance of disk drive designs, at the same time making the products more cost effective to manufacture.

Acknowledgement

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1. ''Effects of Bitshift Distribution on Error Rate in Magnetic Recording'', E. R. Katz and T. G. Campbell, *IEEE Transactions on Magnetics* Vol. MAG-15, No. 3, May 1979.
2. ''Phase Margin Analysis'', M. Monett, Memory Technology Inc., 1980.

Appendix A

The purpose of this appendix is to present some basic information on a few commonly used tools and methodologies in window margin analysis. It will derive a mathematical expression describing the relationship between window shifting versus error rate probability. It will be shown that this expression is equivalent to that which relates to the window narrowing method, which is a well publicized technique to analyze the detection window margin.

There are two prevalent methods in the industry to qualify the window margin of disk drives, the margin that remains when the worst case jitter on the Encoded Read Data bits is subtracted from the non-ideal window (shifted and/or truncated). One method is to ascertain the average pulse distribution from the encoded data stream output. It usually involves a precision time-interval acquisition apparatus which measures the average pulse separation read from a particular track that has been preconditioned with a worst case data pattern. Another method is to measure the accelerated soft error rate induced by modifying the data window derived from an accurate (discrete designed) PLL circuit. Most disk drive testers employ either one of these methods for window margin test. It should be pointed out that testers used in research and development are usually built with the variable window width design, because they lend more sophisticated testing and render additional useful information such as system signal to noise ratio, media defects, and resolution of the head/disk components. It is also interesting to note that because an external PLL system is required, such a tester is generally not capable of checking the data synchronizer block in a disk data storage system.

Since a PLL system with programmable detection window width is expensive and difficult to build, nearly all commercial disk drive testers for manufacturing and end user applications do not employ such technique. Instead, they employ other methods such as measuring the average pulse distribution or the average synchronization window width. Although strobing is also incorporated in some drive testers, they contain but only a few strobe steps. Therefore, in window margin analysis their result can not be compared to the more extensive data gathered from the variable window width method. This trend, however, is changing as engineers are turning to more sophisticated strobing in both disk drive and drive tester designs. If a window shifting technique can mimic window narrowing in error rate response, it can be applied to window margin analysis also. The following discussion presents an accepted model used in the industry to describe error rate probability versus window width and shows that an equivalent expression also holds for the case of a shifted window.

As mentioned in the Strobe Function section, a Gaussian distribution describes error rates due to bit shift. Two such distributions are needed to define the error probability. One distribution is associated with the positive bitshifts and one is associated with negative bitshifts. This is due to the fact that for adjacent bits, one bit is pushed in the Early direction and one is pushed in the Late direction. The residual bitshift is denoted as offset or ''To''. The width of each of the distributions is defined as ''Tne'' which describes the broadening of the distributions due to the random noise of the environment (please refer to *Figure 6*). Hence, the appropriate Gaussian function, defined as N, for the two distributions can be written as:

$$N = \frac{No(K)}{2}\left[\exp\left(-\frac{(t-To^2}{2\,(Tne)^2}\right) + \exp\left(-\frac{(t+To)^2}{2(Tne)^2}\right)\right] \quad (1)$$

where ''No'' is the number of bits read in a revolution of the disc, ''K'' is the normalizing constant to normalize each of the resulting error constants to unity when the distributions are integrated, and ''t'' is the time associated with the bitshift distribution. The equation for the error rate, which is simply the area of the tails of the bitshift distribution beyond the available window width, can be written as:

$$\text{Error Rate (Window-Narrowed)} = \frac{K(No)}{2}\left\{\left[\int_t^{\infty} \exp\left(-\frac{(t-To)^2}{2(Tne)^2}\right)\right] dt \quad (2)$$

$$+ \left[\int_{-\infty}^{t} \exp\left(-\frac{(t+To)^2}{2(Tne)^2}\right)\right] dt\Bigg\}$$

$$= No/2\left\{\text{erfc}\left[\frac{t-To}{Tne}\right] + \text{erfc}\left[\frac{t+To}{Tne}\right]\right\} \quad (3)$$

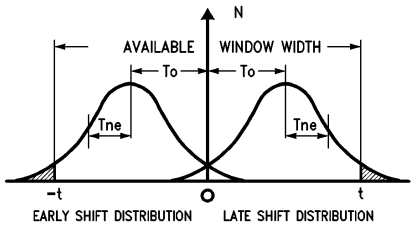

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FIGURE 6. Error Probability from Early/Late Shift Distributions

where ''erfc'' is the complementary error function and ''t'' is the half-window width at which the error rate is observed. An error rate versus window width curve takes the form represented in *Figure 7*. This is obtainable for the case where the data window is modified by narrowing the window while keeping it centered about the phase-locked oscillator expected window. This technique is typical of engineering drive testers employing an external PLL system for window margin analysis.

Consider if the window is shifted, instead of being narrowed, the limits on the second integration of equation (2) are changed and the corresponding ''erfc'' term becomes:

Error Rate
(Shifted Window)

$$= \frac{K(No)}{2}\left\{\int_{t}^{\infty}\left[\exp\left(-\frac{(t'-To)^2}{2(Tne)^2}\right)dt'\right]\right. \quad (4)$$

$$\left.+\int_{-\infty}^{t-T_{\omega}}\left[\exp\left(-\frac{(t'+To)^2}{2(Tne)^2}\right)dt'\right]\right\}$$

$$= No/2\left\{\text{efrc}\left[\frac{t-To}{Tne}\right]+\text{erfc}\left[\frac{Tw-t+To}{Tne}\right]\right\} \quad (5)$$

This corresponds to the bit error distribution evaluated with the average window having nominal width of ''Tw'', and ''t'' being the time position of the window's right-side boundary. In theory, the techniques with window narrowing and that of window shifting are equivalent. Empirical results from these two approaches should correlate if the incremental change in window displacement or window size employed is the same in both cases. Typical error rate versus the amount of shifted window with respect to the mean bit distribution should be similar to the profile depicted in *Figure 7*. A means to implement the shifted window scheme via the DP8459 Strobe function for margin testing is discussed in the text. Unlike the variable PLL-window technique, this method presents a bootstrap test methodology wherein the PLL synchronizer in the system is included in the window margin test.

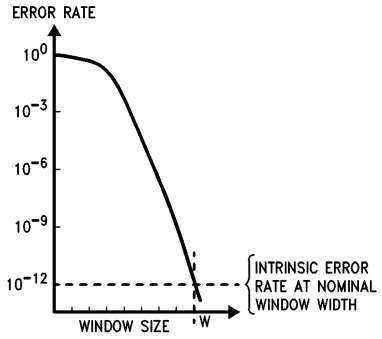

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FIGURE 7. Error Rate Distribution vs Window Width

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