2001
1K (128 x 8) Non-Volatile Random Access Memory

- **5 Volt Only Operation**
- **Fast Static RAM Read Access Time**
  2001-2, 180 ns Max.
  2001, 300 ns Max.
- **Single Line STORE & RECALL**
- **10 ms Self-Timed STORE Cycle**
- **Automatic Recall on Power Up**
- **Write Protect Circuit to Preserve Data On Power-Up and Power-Down**
- **Multiplexed Address and Data Bus**
- **Lower Power Standby Mode**
- **10-Year Data Retention for each STORE**
- **Minimum 10,000 Non-Volatile STORE Cycle Endurance**
- **Unlimited Endurance for Read, Write and RECALL Cycles**
- **HMOS*-E FLOTOX Cell Design**
- **Available in 18-Lead Cerdip and Plastic Packages**
  (See Packaging Spec, Order #231369)

The Intel 2001 Non-Volatile Random Access Memory (NVRAM) is a 1K device organized 128 x 8. It provides the real-time read/write functions of a static RAM together with the reliable non-volatile storage capability of an E²PROM array to preserve its memory contents when power is removed. The multiplexed address and data bus allows the 2001 to interface directly to the iAPX 88 and iAPX 188 microprocessors and MCS®-51 microcomputer to provide a maximum level of system integration.

Internally, the 2001 NVRAM consists of a high speed static RAM array backed up, bit-for-bit, by an E²PROM array for non-volatile storage. The transfer of memory data between the static RAM and the E²PROM array occurs in parallel for fast storage and recall as well as minimal system support.

Two functions are provided to transfer data between the volatile RAM and its non-volatile E²PROM counterpart. The STORE function transfers RAM data into the E²PROM while the RECALL function fetches E²PROM data and places it in the RAM array. Both functions are controlled by a single $\overline{NE}$ signal which can easily be activated with traditional circuitry in memory mapped space, through an I/O port, or from the output of a power-fail detector.

The RAM operating characteristics of the 2001 NVRAM provides high speed microprocessor performance with unlimited endurance. In the non-volatile storage mode, data retention is specified at over 10 years for each STORE operation. Over 10,000 STORE operations can be performed reliably.

The 2001 NVRAM is furnished in an 18-pin, 300 mil package with its address and data lines multiplexed for direct interface to specific microcontrollers and microprocessors.

*HMOS is a patented process of Intel Corporation.

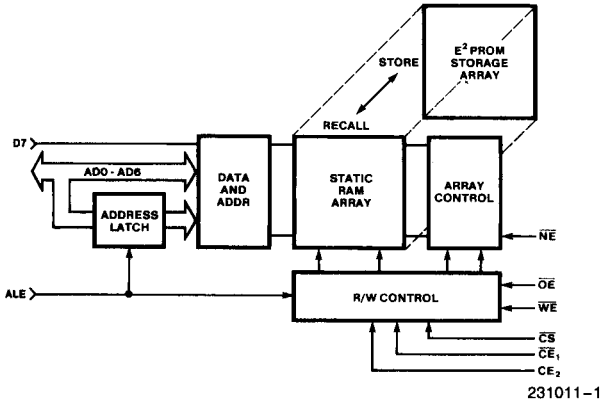


Figure 1. 2001 Functional Diagram

2001 Pin Names

AD0-AD6	Multiplexed Address/Data Lines
D7	Data Bit 7
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
$\overline{CE}_1$	Chip Enable 1
CE_2	Chip Enable 2
$\overline{NE}$	Non-Volatile Enable (Store/Recall Control)
ALE	Address Latch Enable
NC	No Internal Connection

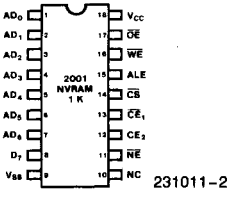


Figure 2. 2001 Pin Configuration

October 1985
Order Number: 231011-003

DEVICE OPERATION

The design of the 2001 NVRAM allows it to be connected directly to the multiplexed address/data bus of the iAPX 88 and iAPX 188 microprocessors, and the MCS-51 microcontroller. The 7 address lines and lower 7 data bits for the 2001 are multiplexed on pins AD0–AD6. The falling edge of ALE (Address Latch Enable) strobes the seven address bits of AD0–AD6 and the states of $\overline{CE}_1$ and CE_2 into the 2001's on-chip latches. The rising edge of $\overline{WE}$ writes the data from the address/data bus into the RAM array location specified by the latched address. An ALE pulse is required for STORE and RECALL initiation cycles as well as read and write cycles. The 2001's operational modes are given in Table 1.

Table 1. 2001 Operational Modes V_{CC} = 5V

Mode Pin	$\overline{CE}_1$	CE_2	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{NE}$	Data
Standby	V_{IH}	X	X	X	X	X	Hi-Z
	X	V_{IL}	X	X	X	X	Hi-Z
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data In
Automatic RECALL at V_{CC} Power Up	X	X	X	X	X	X	Hi-Z
Normal RECALL	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Hi-Z
STORE	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Hi-Z

NOTES:
1. X = Don't Care.
2. The $\overline{CE}_1$ and CE_2 inputs are latched by the falling edge of ALE for Read and Write cycles. For STORE and RECALL initiation cycles, ALE may be either pulsed as in Write and Read cycles (see Write and Read cycles timing diagrams) or ALE can be held at V_{IH} for the active duration of $\overline{CS}$. In the latter case $\overline{CE}_1$ and CE_2 should also be held active for as long as $\overline{CS} = V_{IL}$.

Reading or writing to the 2001's RAM array allows immediate random access to any of the 128 bytes in that array. To do a read or write cycle, a V_{IL} level is put on the $\overline{CS}$ pin and a V_{IH} level on the $\overline{NE}$ pin. A read cycle is performed by putting a V_{IL} level on $\overline{OE}$ with $\overline{WE}$ held high, and a write cycle is performed by applying a V_{IL} level to $\overline{WE}$ with $\overline{OE}$ held high.

The timing for a RECALL or a STORE initiation cycle is the same as for a read or write cycle, respectively, except that a V_{IL} level is applied to the $\overline{NE}$ input.

RECALL OPERATION

A RECALL operation is initiated by bringing $\overline{OE}$ low while $\overline{NE} = V_{IL}$. This causes the data from the NVRAM's internal non-volatile storage array to be transferred to the static RAM array, from which it can be externally accessed. The RECALL function can be activated by the CPU at any time, as often as desired without affecting the integrity of the data in the non-volatile storage array. The RECALL function occurs automatically when V_{CC} is applied.

STORE

A STORE operation is started by bringing $\overline{WE}$ low with $\overline{NE} = V_{IL}$. This causes the data in the static RAM array to be transferred to the non-volatile storage array. The STORE function is typically used to save data at system power-down and is initiated when a POWER DOWN signal is received by the system from the power supply or a power supply monitoring circuit. Since the STORE cycle takes 10 ms for reliable storage, the NVRAM's V_{CC} supply must be maintained at no less than V_{CC} Min for at least 10 ms. (V_{CCMIN} = 4.75V for parts with 5% V_{CC} tolerance.)

TWO-LINE CONTROL

The 2001 Non-Volatile RAM features 2-line control. By requiring a Chip Select ($\overline{CS} = V_{IL}$) whenever a device function is to be activated (determined by $\overline{OE}$, $\overline{WE}$, and $\overline{NE}$), data bus contention is eliminated, system noise is reduced, and system design is simplified.

MULTIPLE CHIP SELECTS ALLOWS MEMORY DECODING

The 2001 has three device enabling control inputs, $\overline{CS}$, $\overline{CE}_1$, and CE_2. Having multiple device enable lines allows memory decoding to be done by connecting the enable lines to system addresses. In the MCS-51 microcontroller example in Figure 3, by connecting $\overline{CS}$, $\overline{CE}_1$, and CE_2 to addresses A13, A14, and A15, respectively, the 2001 would be memory-mapped at location 8000H.

STANDBY MODE

Power for the internal circuitry of the 2001 NVRAM is controlled by the $\overline{CE}_1$ and CE_2 inputs. When either input is inactive ($\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$), the NVRAM is in the Standby mode and consumes 65% less power. In this mode the address/data pins are in a high impedance state.

STORE AND RECALL CONSIDERATIONS

Data retention for data that has been written into the 2001's non-volatile array by a STORE operation is greater than 10 years. The STORE endurance is a minimum of 10^4 cycles, that is, at least 10,000 STORE operations can be reliably performed.

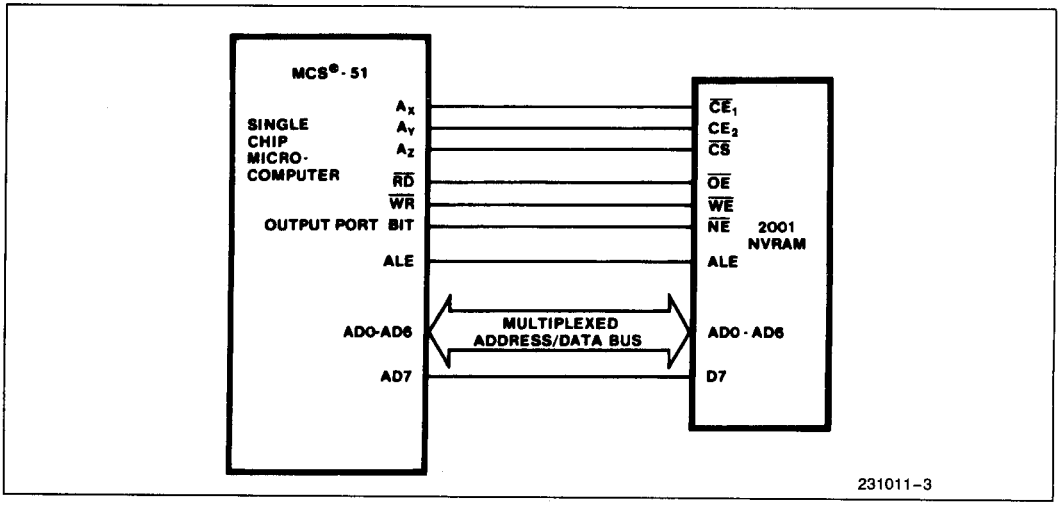


Figure 3. Using the 2001 NVRAM with an MCS®-51 Single Chip Microcomputer

NOTE:
A_X, A_Y, and A_Z are any three of the MCS®-51 address pins A8–A15. By connecting $\overline{CE}_1$, CE_2, and $\overline{CS}$ to specific address lines, the 2001 can be mapped to a particular range in memory, eliminating the need for an external memory decoder.

ON-CHIP DATA PROTECTION DURING SYSTEM POWER UP/DOWN

The 2001 NVRAM has an on-chip STORE lockout circuit which prevents spurious STOREs from occurring when system power is being applied or taken away. This on-chip circuit frees the designer from having to design in an external data protection circuit.

Spurious STOREs can be caused by unstable system control signals generated by system components when V_{CC} is rising or falling during system power up or power down. Although a STORE operation is normally initiated in an NVRAM when system power-down is detected, a second spurious STORE caused by unpredictable system components due to falling power could cause incorrect data to be transferred to the non-volatile storage array.

The on-chip STORE lockout circuit prevents a STORE operation from being initiated when V_{CC} is below 4V (V_{LKO}). Since systems tend to stabilize when V_{CC} is above 3.5V, this value provides suitable margin. For more information about power up/down data protection, see Application Note AP-165.

SYSTEM IMPLEMENTATION

The multiplexed address/data bus of the 2001 allows the device to be directly connected to the address/data bus of microprocessors such as the iAPX 88 and the iAPX 188, and to microcomputers such as the MCS-51. Figure 3 shows an example of a 2001 connected to an MCS-51 microcomputer. The $\overline{NE}$ signal is generated by one of the MCS-51's I/O output port bits. The three enable signals on the 2001, $\overline{CE}_1$, CE_2, and $\overline{CS}$ are connected directly to specific address bits that map the device into a particular address range, thus eliminating the need for a memory decoder.

Figure 4 shows the 2001 in an iAPX 88 minimum mode system. As in the MCS-51 system in Figure 3, no additional system components are needed for the 2001. The 2001's address/data bus connects directly to AD0–AD6 of the iAPX 88, and system address line A8 is used to drive the $\overline{NE}$ input. As shown in the memory map for this example in Figure 4, Store/Recall access is done at addresses 40000H-40007FH, and a write or a read cycle at address 40100H will start a WRITE or a READ operation, respectively.

The 2001 NVRAM is typically used in a system to save critical data when the system powers down. This is done by connecting a POWER DOWN signal to an interrupt input on the CPU such that an interrupt subroutine is called when system power starts to fall. The interrupt subroutine writes all critical system data to the NVRAM's RAM array, then initiates a STORE operation. The STORE operation transfers the on-chip RAM array data to the device's non-volatile storage array. (See Figure 5.)

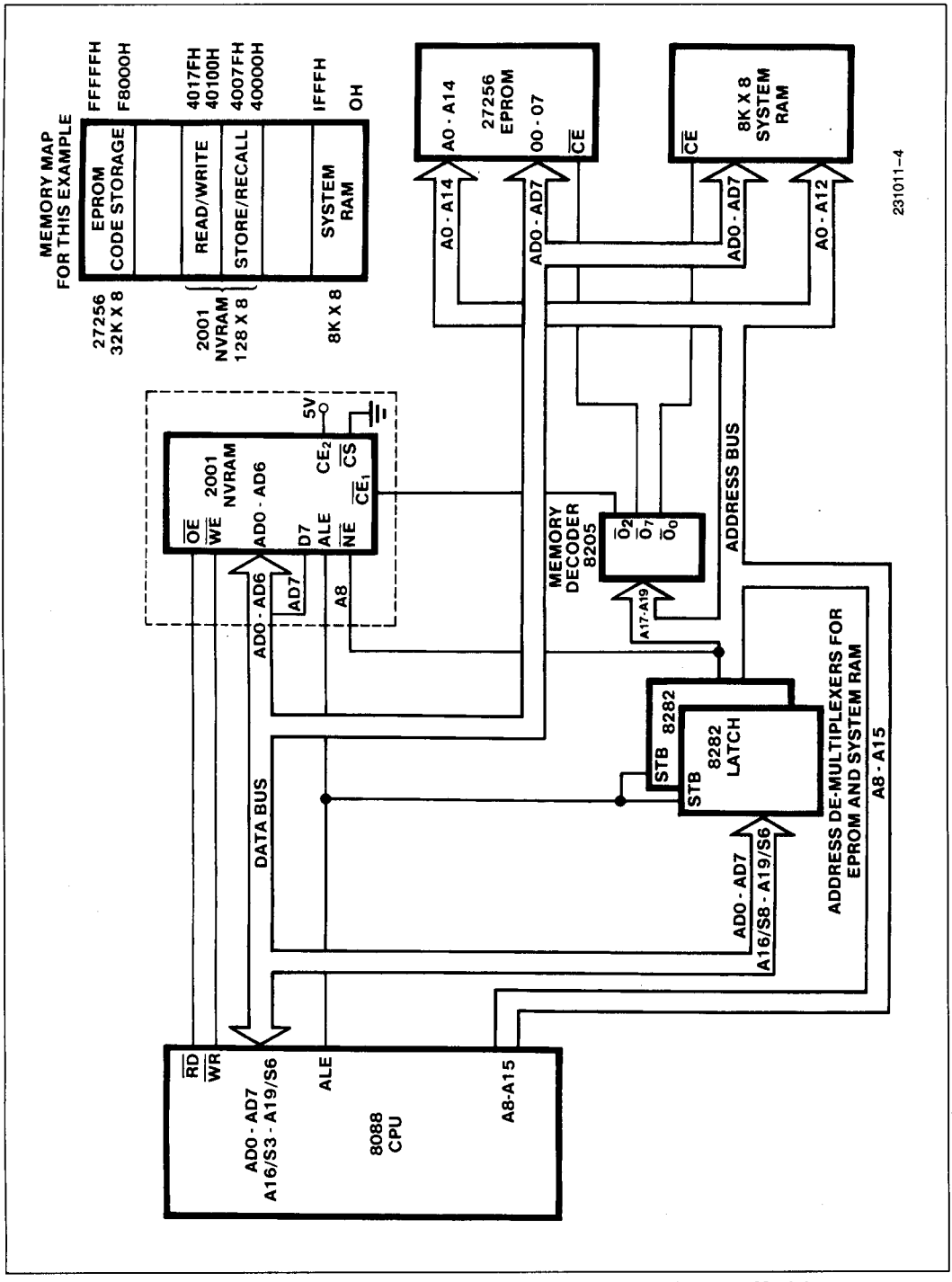


Figure 4. Adding the 2001 NVRAM to an iAPX 88 System (Minimum Mode)

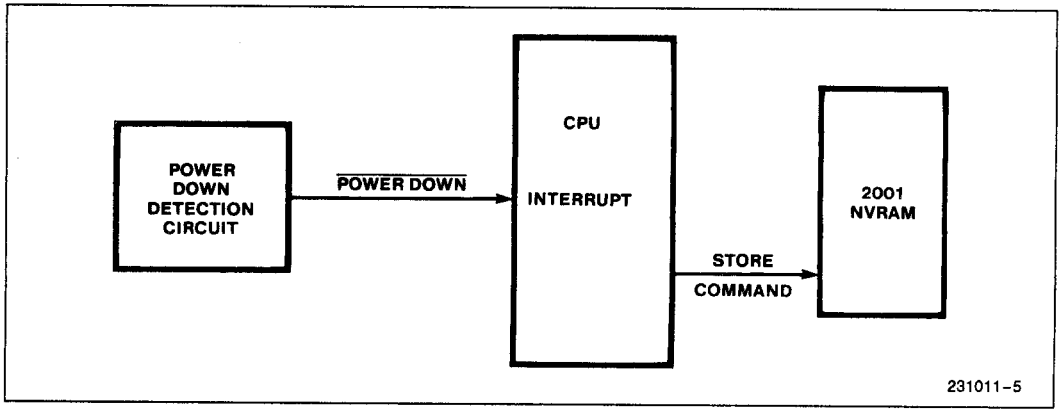


Figure 5. Basic NVRAM System Implementation

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
All Input or Output Voltages with Respect to Ground ..... +6V to −0.3V

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

Operating Conditions: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	2001-2		2001		Units	Conditions
		Min	Max	Min	Max		
I_{LI}	Input leakage current		10		10	μA	V_{CC} = Max, V_{IN} = GND to V_{CC}
I_{LO}	Output leakage current		10		10	μA	V_{CC} = Max, V_{OUT} = GND to V_{CC}
I_{CC1}	V_{CC} current (Standby)		35		30	mA	V_{CC} = Max, $\overline{CE} = V_{IH}$ or $CE_2 = V_{IL}$
I_{CC2}	V_{CC} current (Active)		100		85	mA	V_{CC} = Max, Mode = Read or Write
I_{CC3}	V_{CC} current (STORE)		100		85	mA	V_{CC} = Max, Mode = STORE
I_{CC4}	V_{CC} current (RECALL)		100		85	mA	V_{CC} = Max, Mode = RECALL
V_{IL}	Input low voltage	−0.1(1)	0.8	−0.1(1)	0.8	V	
V_{IH}	Input high voltage	2.0	$V_{CC}+1$	2.0	$V_{CC}+1$	V	
V_{OL}	Output low voltage		0.4		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output high voltage	2.4		2.4		V	I_{OH} = −400 μA
V_{RCL}	V_{CC} level at which automatic RECALL begins during V_{CC} Power-Up	4.0		4.0		V	
V_{LKO}	V_{CC} level for STORE lockout	4.0	4.65	4.0	4.65	V	

NOTE:
1. −1.0V spikes less than 20 ns in duration are allowed.

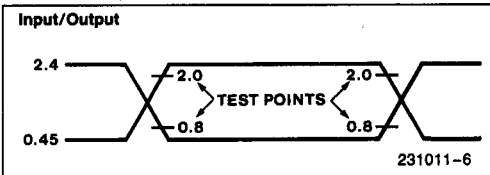
CAPACITANCE ($T_A = 25°C$, f = 1 MHz)

Symbol	Parameter	Typ.(1)	Max	Units	Test Conditions
C_{IN}	Input Capacitance	5	10	pF	$V_{IN} = OV$
C_{OUT}	Output Capacitance		10	pF	$\overline{OE} = \overline{CE_1} = \overline{CS} = V_{IH}$, $CE_2 = V_{IL}$

A.C. TEST CONDITIONS

Output Load . . . . . 1 TTL gate + C_L = 100 pF
Input Rise and Fall Times
(10% to 90%) . . . . . 20 ns
Input Pulse Levels . . . . . 0.45V to 2.4V
Input Timing Reference Level . . . . . 0.8V and 2.0V
Output Timing Reference Level . . . . . 0.8V and 2.0V

A.C. Testing Input, Output Waveform



A.C. Testing inputs are driven at 2.4V for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8V for a Logic 0.

A.C. CHARACTERISTICS

Read Cycle

Symbol	Parameter	2001-2		2001		Units
		Min	Max	Min	Max	
t_{LD}	ALE to Valid Data Out (Access Time)		180		300	ns
t_{OE}	$\overline{OE}$ Access Time		120		170	ns
t_{RP}	$\overline{OE}$ Pulse Width	150		250		ns
t_{OH}	Output Held from Addresses, $\overline{CS}$, or $\overline{OE}$ (whichever changes first)	0		0		ns
t_{DF}(1)	$\overline{OE}$ High to Output Not Driven	0	60	0	95	ns
t_{OLZ}	$\overline{OE}$ Low to Output Driven	10		10		ns

Write Cycle

Symbol	Parameter	2001-2		2001		Units
		Min	Max	Min	Max	
t_{WP}	Write Pulse Width	150		250		ns
t_{DS}	Data Valid to End of Write	150		150		ns
t_{DH}	Data Valid After End of Write	15		20		ns

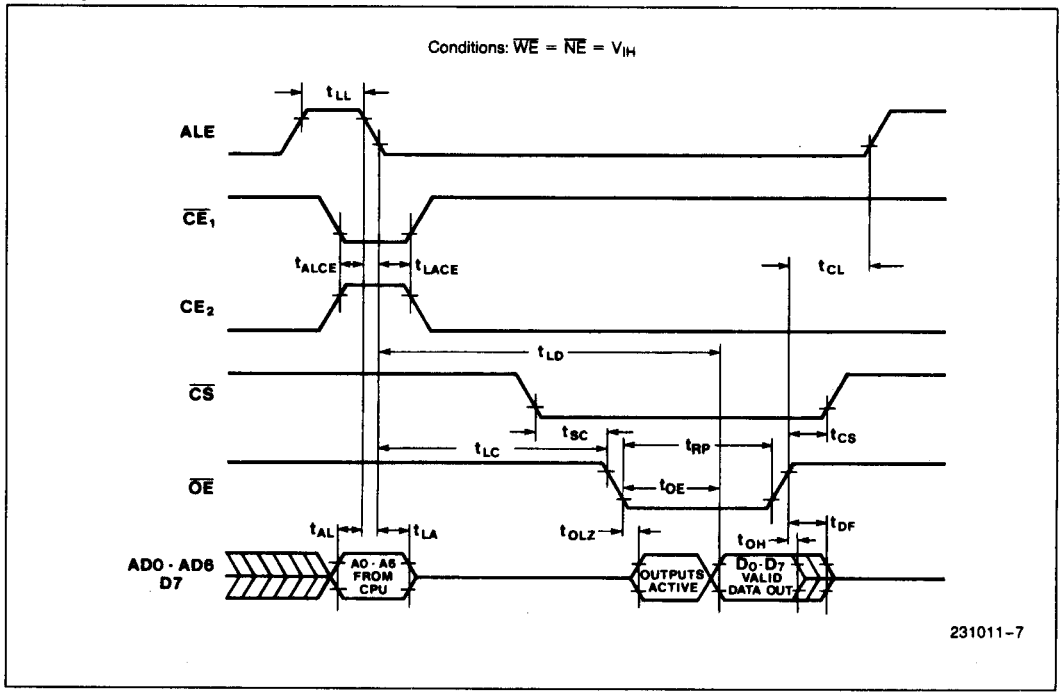
NOTE:
1. This parameter only sampled and not 100% tested.

Timing For ALE, $\overline{CE}_1$, CE_2, and $\overline{CS}$

Symbol	Parameter	2001-2		2001		Units
		Min	Max	Min	Max	
t_{LL}	ALE Width	60		100		ns
t_{ALCE}	$\overline{CE}$ Setup to ALE	5		30		ns
t_{LACE}	$\overline{CE}$ Hold After ALE	40		45		ns
t_{AL}	Address Setup to ALE	20		50		ns
t_{LA}	Address Hold After ALE	30		45		ns
t_{SC}	$\overline{CS}$ Setup to Read/Write Command	20		50		ns
t_{CS}	$\overline{CS}$ Hold After Read/Write Command	10		10		ns
t_{LC}	ALE to Read/Write Command	35		80		ns
t_{CL}	Read/Write Command to ALE	0		0		ns

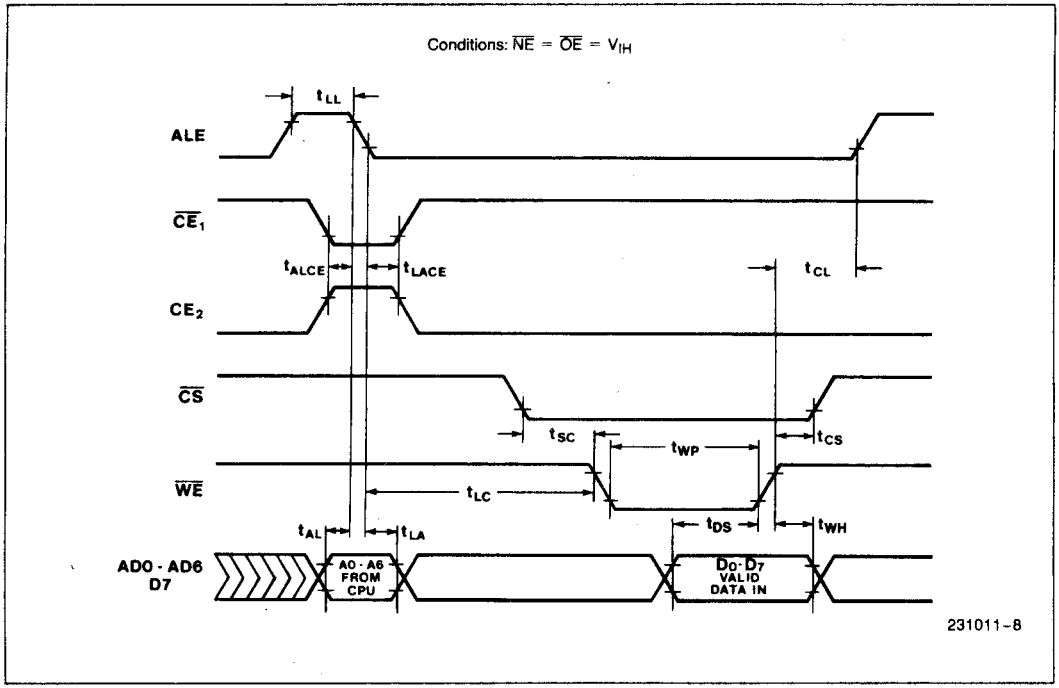
WAVEFORMS

Read Cycle



WAVEFORMS (Continued)

Write Cycle



STORE Operation(1,2)

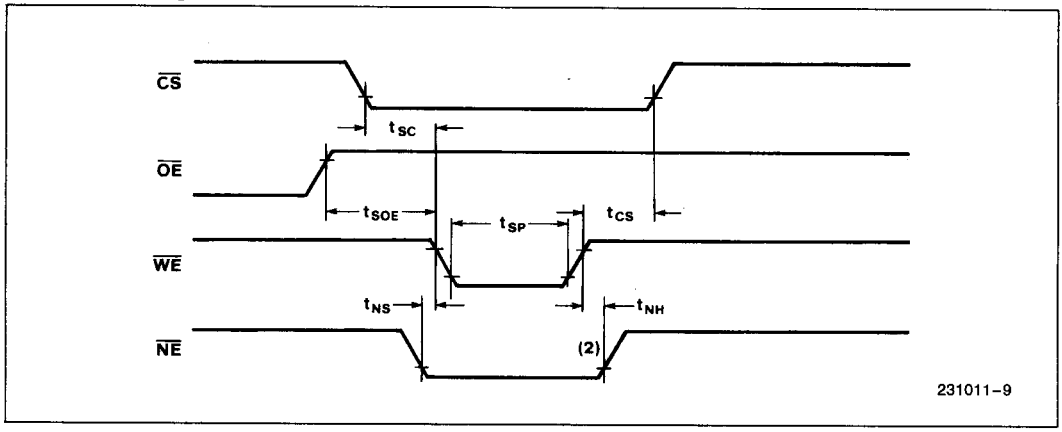
Symbol	Parameter	2001-2		2001		Units
		Min	Max	Min	Max	
t_{SC}	$\overline{CS}$ Setup Time to STORE Command	20		50		ns
t_{CS}	$\overline{CS}$ Hold Time after STORE Command	10		10		ns
t_{NS}	$\overline{NE}$ Setup Time to STORE Command	0		0		ns
t_{NH}	$\overline{NE}$ Hold Time after STORE Command	0		0		ns
t_{SOE}	$\overline{OE}$ Disable to STORE Initiation Cycle Pulse	90		90		ns
t_{SP}	STORE Initiation Cycle Pulse Width	150		250		ns
t_{STR}(3)	STORE Operation Time		10		10	ms
t_{VMIN}	V_{CC} Above V_{CCMIN} after STORE Operation is Initiated	10		10		ms

NOTES:
1. During a STORE Initiation Cycle, address/data inputs are ignored.
2. For a STORE Initiation Cycle, $\overline{WE}$ must not go low before $\overline{NE}$. Otherwise, a RAM write cycle will result.
3. t_{STR} begins on the falling edge of $\overline{WE}$.

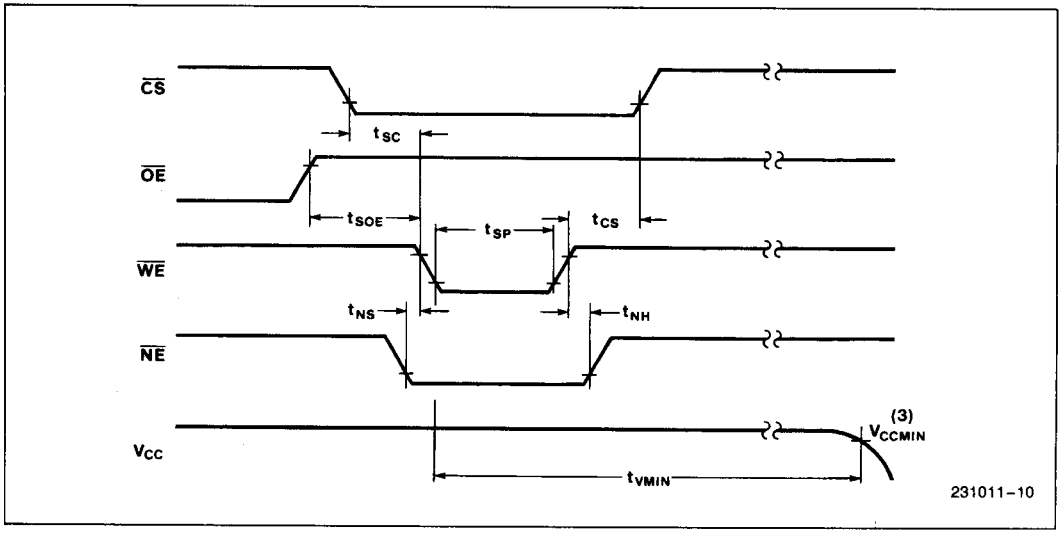
WAVEFORMS

STORE Initiation Cycle (1) (See Mode Table Note 2 for ALE, $\overline{CE}_1$, and CE_2 timing)

Normal Operating Conditions



System Power Down

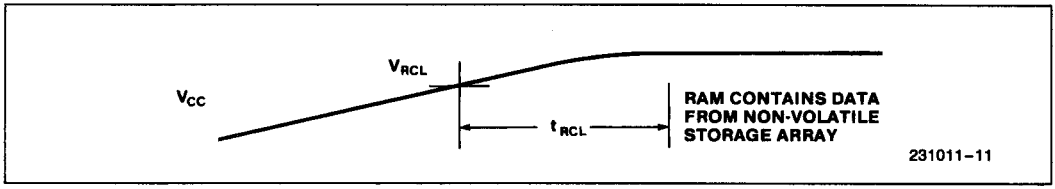


NOTES:
1. Once a STORE Operation has begun, all inputs are ignored and the output: are in a high impedance state.
2. After either a STORE or a RECALL operation, or after the device has been powered up, a lockout feature on the $\overline{NE}$ input inhibits subsequent STORE or RECALL initiation cycles until $\overline{NE}$ is brought back high. The $\overline{NE}$ input should therefore be brought back high after each STORE or RECALL operation if another STORE or RECALL is to be performed before the system is powered down.
3. V_{CCMIN} = 4.75V for 5% V_{CC} specs.

RECALL Operation (1)

Symbol	Parameter	2001-2		2001		Units
		Min	Max	Min	Max	
t_{SC}	$\overline{CS}$ Setup Time to RECALL Command	20		50		ns
t_{CS}	$\overline{CS}$ Hold Time after RECALL Command	10		10		ns
t_{RS}	$\overline{NE}$ Setup Time to RECALL Command	0		0		ns
t_{RH}	$\overline{NE}$ Hold Time after RECALL Command	0		0		ns
t_{RWE}	$\overline{WE}$ Disable to RECALL Initiation Cycle Pulse	90		90		ns
t_{RP}	RECALL Initiation Cycle Pulse Width	150		250		ns
t_{RCL}	RECALL Operation Time		5		5	μs

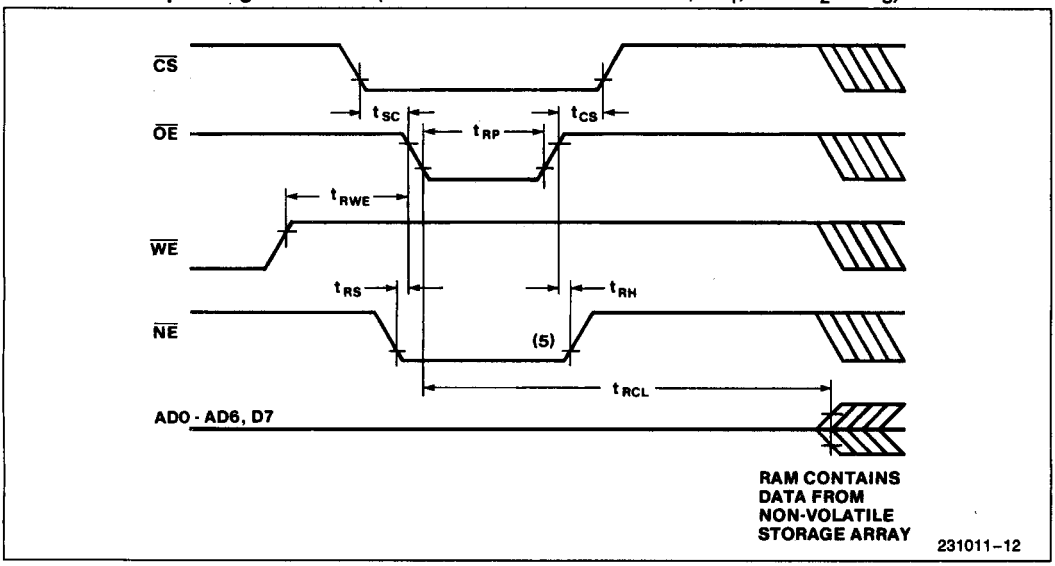
Automatic RECALL During System Power Up(2)



WAVEFORM

Recall Initiation Cycle (4)

Under Normal Operating Conditions (See Mode Table Note 2 for ALE, $\overline{CE}_1$, and CE_2 timing)



NOTES:
1. During a RECALL Initiation Cycle, the address and data inputs are ignored.
2. During Automatic Power-Up RECALL, all control signal inputs are ignored.
3. V_{CCMIN} = 4.75V for 5% V_{CC} specification.
4. Once a RECALL Operation has begun all inputs are ignored and the outputs are in a high impedance state.
5. After either a STORE or a RECALL operation, or after the device has been powered up, a lockout feature on the $\overline{NE}$ input inhibits subsequent STORE or RECALL initiation cycles until $\overline{NE}$ is brought back high. The $\overline{NE}$ input should therefore be brought back high after each STORE or RECALL operation if another STORE or RECALL is to be performed before the system is powered down.

EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS NVRAM family is a series of non-volatile random access memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of NVRAM, allowing the choice of appropriate memory size to match system applications. EXPRESS NVRAM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS NVRAM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel NVRAMs, the EXPRESS NVRAM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS NVRAM PRODUCT FAMILY

Product Definitions

Type	Operating Temperature	Burn-in 125° (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	None
L	−40°C to +85°C	168 ±8

PACKAGING OPTIONS

2001 Versions

Packaging Options		
Speed Versions	**Cerdip**	**Plastic**
−2	Comm, T, Q, L	Comm
−STD	Comm, T, Q, L	Comm

Comm = Commercial (0°−70°C) devices