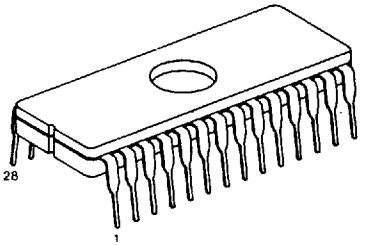
256 K (32 K x 8) CMOS UV ERASABLE PROM

DESCRIPTION

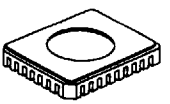
The 27C256 is a high speed 262, 144 bit ultraviolet erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

The 27C256 is packaged in 28 pin Window Ceramic Freat Seal package (Cerdip). The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

All inputs/outputs are fully TTL compatible.



Q suffix
28 pins CERDIP
Dual in line glass sealed package



EQ suffix
32 pins LCCC
(Leadless Ceramic Chip Carrier with window)

MAIN FEATURES

- Organized 8 K x 8 : JEDEC Standard Pinouts :
  - 28 Pin Dual in Line Package,
  - 32 Pin Chip Carrier (Leadless Ceramic).
- Very fast access time : 150, 200 and 250 ns.
- Compatible to high speed microprocessors zero wait state.
- Low «CMOS» consumption :
  - active current : 100 mA max,
  - standby current : 1 mA max.
- Programming voltage : 12.5 V.
- Electronic signature for automated programming.
- Programming times in the 3 seconds range (PRESTO II algorithm).
- Military temperature range : $T_C = -55, +125°C$.
- Power supply : 5 V_{DC} ± 10 %.
- Also available in OTP version on request (One Time Programmable).

SCREENING / QUALITY

This product is manufactured in full compliance with :

- CECC 90000 (class B, quality assessment level Y).
- TMS STANDARD.
- MIL-STD-883C (to be introduced).

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SUMMARY

A · GENERAL DESCRIPTION

INTRODUCTION

The following characteristics shall apply over the full operating temperature range V_{CC} = 5 V ± 10 %.

The 27C256 series are 262, 144-bit, ultraviolet-light, erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The 27C256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (Q suffix) and LCCC (EQ suffix) rated for operation from − 55°C to + 125°C for T_C.

Since these EPROMs operate from a single 5 V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming but all programming signals are TTL level.

There are seven modes of operation for the 27C256. Read mode requires a single 5 V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

The 27C256 has a standby mode that reduces the maximum power dissipation. But in this case the read access of the memory is not possible.

Maximum operating power dissipation : 250 mW at 5 V at $T_C \geqslant 25°C$ / 500 mW at 5 V at $T_C < 25°C$.

Maximum standby power dissipation : 5 mW at 5 V.

This memory has static operation : no clocks no refresh.

Max access / Min cycle time :
27C256-15 : 150 ns
27C256-20 : 200 ns
27C256-25 : 250 ns

This memory is fully compatible with TTL families S, LS, AS, ALS.

1 · DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

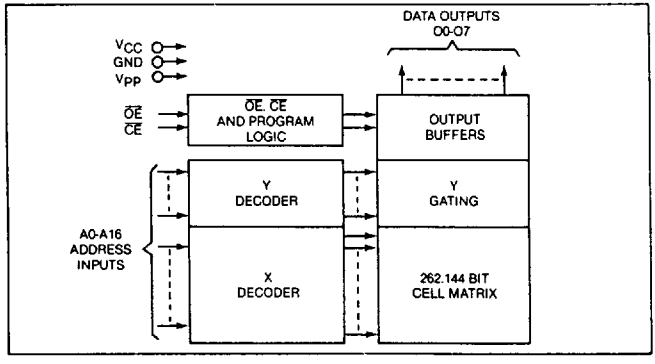
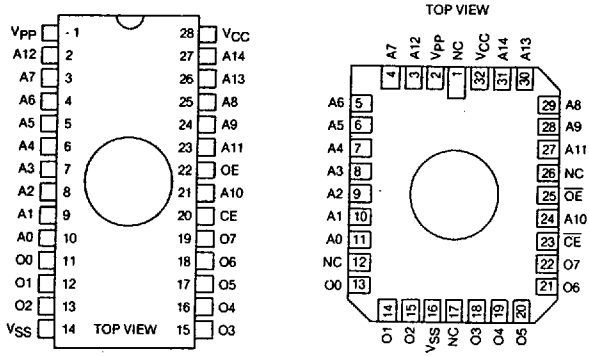


FIGURE 1 - 27C256 BLOCK DIAGRAM.

2 - PIN ASSIGNEMENTS



• Pin 1 indicator on top of package.

FIGURE 2 - PIN CONFIGURATION.

3 - TERMINAL DESIGNATIONS

The function and relevant symbols of each terminal of the device are given in the Figure 3 below.

A0-A14	Address Input
CE	Chip Enable Input
OE	Output Enable
O0-O7	Data Input / Output
NC	Non Connected

FIGURE 3 - PIN FUNCTION.

4 - OPERATING MODES

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	OUTPUTS
Read	L	L	X	V_{CC}	D_{OUT}
Output disable	L	H	X	V_{CC}	High Z
Standby	H	X	X	V_{CC}	High Z
Program	L	H	X	V_{PP}	D_{IN}
Program verify	H	L	X	V_{PP}	D_{OUT}
Program inhibit	H	H	X	V_{PP}	High Z
Electronic signature	L	L	V_H	CC	CODE

Notes : X = Don't care ; V_H = 12 V ±0.5 V ; H = High ; L = Low.

B · DETAILED SPECIFICATIONS

1 · SCOPE

This drawing describes the specific requirements for the CMOS UV erasable PROM memories 27C256 150 ns, 200 ns and 250 ns access time with MIL-STD-883 class B rev C or CECC 90000.

2 · APPLICABLE DOCUMENTS

2.1 · MIL-STD-883 (non applicable)

1) MIL-STD-883 : test methods and procedures for electronics
2) MIL-M-38510 : general specifications for microcircuits

2.2 · CECC 90000

1) CECC 90000
2) Specification 90113-001 UTEC 86-252-001

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be is shown in figure 3.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-M-38510.

3.2.3 · Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-M-38510 appendix C (when defined) :

- Cerdip 28
- 32 LCCC with window.

The precise case outlines are described into MIL-M-38510.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings (Table 1)

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

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Table 1 - Absolute maximum ratings
Unless otherwise stated all voltages are referenced to the reference terminal as defined in Figure 3 of this specification.
Limiting conditions (ratings) are not for inspection purposes.
All voltages are referenced to GND.

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		−0.6	7	V
V_{PP}	Programming supply voltage		−0.6	14	V
V_I	Input voltage	(Except A9)	−0.6	6.5	V
		(A9)	−0.6	13.5	V
V_O	Output voltage		−0.6	V_{CC} + 1	V
V_{OZ}	Off-state voltage		−0.6	V_{CC} + 1	V
I_O	Output current			5	mA
I_I	Input current			15	mA
P_D max.	Max. power dissipation			550	mW
T_{case}	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−65		°C

Note : Stresses above those listed under «Absolute maximum ratings» may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.3.2 - Recommanded conditions of use and guaranteed characteristics

a) Guaranteed characteristics (Tables 4 and 5)

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined is this specification in guaranteed only under the conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommanded operating ranges specified below.

b) Recommended conditions of use (Table 2)

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also above).

These conditions shall not be for inspection purposes.

Some recommanded values may, however, be taken in other parts of this specification as detail conditions for an applicable test.

Table 2 - Recommended conditions of use
All voltages are referenced to a reference terminal (V_{SS}, GND, etc...)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	4.5	5.5	V
V_{IL}	Low level input voltage	−0.1	0.8	V
V_{IH}	High level input voltage	2	V_{CC} + 0.5	V
T_{case}	Operating temperature	−55	+125	°C

3.4 · Thermal characteristics

Table 3

Package	Symbol	Parameter	Value	Unit
CERDIP DIL 28		**Thermal resistance · Ceramic**		
	$\theta_{J\text{-}A}$	Junction-to-Ambient	55	°C/W
	$\theta_{J\text{-}C}$	Junction-to-Case	10	°C/W
LCCC 32		**Thermal resistance · Ceramic**		
	$\theta_{J\text{-}A}$	Junction-to-Ambient	60	°C/W
	$\theta_{J\text{-}C}$	Junction-to-Case	15	°C/W

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output

Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in «Thermal Resistance Measurement Method for EF 68xx Microcomponent Devices», and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or CECC 90000 devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883 (non applicable)

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

4.2 · CECC

Is in accordance with CECC 90000. Group A and B inspection are performed on each production lot as specified in CECC 90113-001. Group C inspection is performed on a periodic basis in accordance with CECC 90113-001.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurements conditions are given below :

- Table 4 : Static electrical characteristics.
- Table 5 : Dynamic electrical characteristics.

For static characteristics (Table 4), test methods refer to IEC 748-2 method number, where existing.

5.2 · Static characteristics

$V_{CC} = 5.0\,V_{dc} \pm 10\%$; GND = $0\,V_{dc}$; $T_C = -55 / +125°C$

All voltages are referenced to GND.

Table 4

Symbol	Parameter	Test Conditions	Min	Max	Unit
I_{LI}	Input leakage current	$V_{IN} = 5.5\,V$		10	µA
I_{LO}	Output leakage current	$V_{OUT} = 5.5\,V$		10	µA
I_{CC1}	V_{CC} active current $\overline{CE} = \overline{OE} = V_{IL}$ to f = 8 MHz	V_{CC} max I_{OUT} = 0 mA (open output) · T < 25°C · T ⩾ 25°C		 100 50	 mA mA
I_{CC2}	V_{CC} standby current	CE = V_{IH} , V_{CC} max		1	mA
I_{PP1}	V_{PP} read current	$V_{PP} = V_{CC}$		0.1	mA
V_{IL}	Input low voltage	V_{CC}		0.8	V
V_{IH}	Input high voltage	V_{CC}	2		V
V_{OL}	Output low voltage (see Note)	$I_{OL} = 2.1\,mA$		0.45	V
V_{OH}	Ouput high voltage (see Note)	$I_{OH} = -400\,\mu A$	2.4		V
Note : For measurement of this characteristic it may be necessary to programme the device.					

5.3 · Dynamic characteristics

$V_{CC} = 5.0\,V_{dc} \pm 10\%$; GND = $0\,V_{dc}$; $T_C = -55 / +125°C$

Table 5

Symbol	Parameter	$V_{CC} \pm 10\ \%$	27C256-15		27C256-20		27C256-25		Unit
		Test conditions	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address access time	$\overline{CE} = \overline{OE} = V_{IL}$ (see Note 1)		150		200		250	ns
t_{CE}	Chip enable access time	$\overline{OE} = V_{IL}$ (see Note 1)		150		200		250	ns
t_{OE}	Output enable access time	$\overline{CE} = V_{IL}$ (see Note 1)		50		60		70	ns
t_{DF}	Output disable float time	(see Note 2)	0	40	0	50	0	60	ns
t_{OH}	Output hold time	$\overline{CE} = \overline{OE} = V_{IL}$ (see Note 1)	0		0		0		ns

Note 1 : Loading circuit (see Figure 4) input pulse levels : 0 V to 3 V.
Note 2 : t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whatever occurs first.

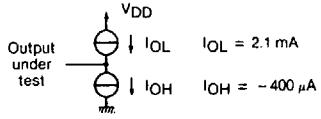

FIGURE 4 - AC LOADING CIRCUIT.

5.4 - AC test conditions specific to the device

Input rise and fall times ..... ≤ 20 ns
Input pulse levels ..... 0 V to 3 V
Timing measurement reference level inputs, outputs ..... 0.8 V and 2 V

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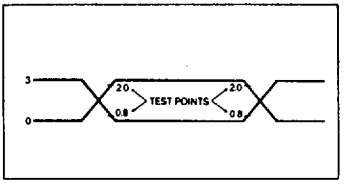


FIGURE 5 - AC TESTING INPUT / OUPUT WAVEFORM.

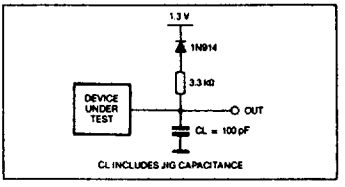
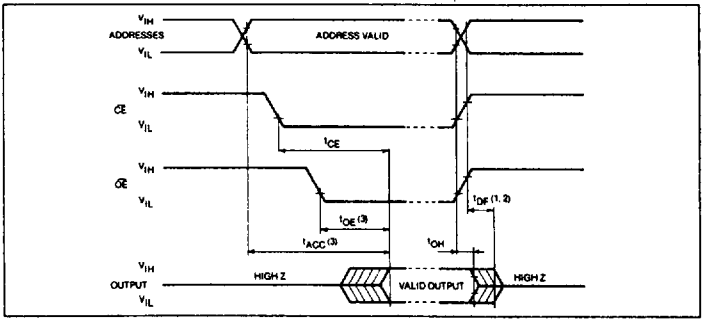


FIGURE 6 - AC TESTING LOAD CIRCUIT.



Note 1 : This parameter is only sampled and not 100 % tested.
Note 2 : t_{DF} is specified form $\overline{OE}$ or $\overline{CE}$ whichever occurs first.
Note 3 : $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.

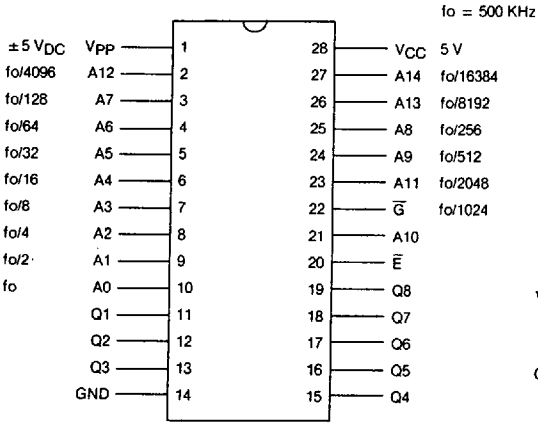
FIGURE 7 - AC WAVEFORMS.

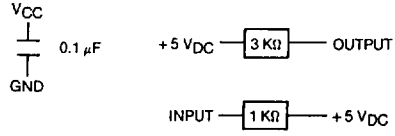
5.5 · Capacitance

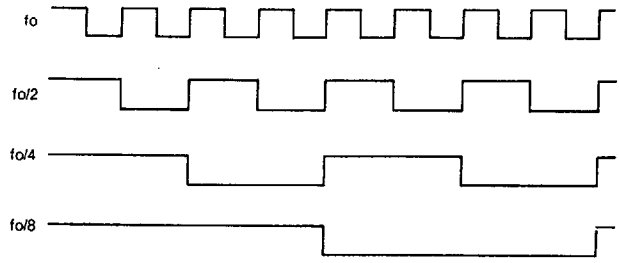
Table 6 · T_{amb} = +25°C, f = 1 MHz (see note)

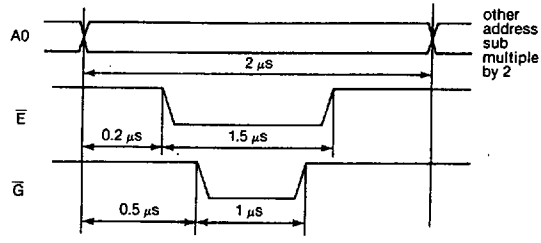
Symbol	Parameter	Test Conditions	Min	Typ. (Note)	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		4	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		8	12	pF
Note : Capacitance is guaranteed by periodic testing, T_{amb} = +25°C, f = 1 MHz.						

5.6 · Burn-in conditions for DIL package









6 - FUNCTIONAL DESCRIPTION

6.1 - Function description

The 27C256 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 262, 144 bits organized as 32, 768 words of 8 bits length.

When the outputs of two or more 27C256's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the 27C256, a low-level signal is applied to the E and G pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

Active I_{CC} current can be reduced by applying a high TTL signal to the E pin. In this mode all outputs are in the high-impedance state.

6.2 - Function table

Table 7

Functions (pins)	Mode						
	Read	Output disable	Standby	Programming	Verify	Program inhibit	Signature mode
$\overline{CE}$ (20)	0	0	1	0	1	1	0
$\overline{OE}$ (22)	0	1	X	1	0	1	0
A9 (24)	X	X	X	X	X	X	V_H*
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11-13, 15-19)	Q	HI-Z	HI-Z	D	Q	HI-Z	Code

* V_H = 12 V ±0.5 V.

6.3 - Device operation

The modes of operations of the 27C256 are listed in the Operating Modes. A single 5 V power supply is required in the read mode. All inputs are TTL levels except for 12 V on A9 for Electronic Signature.

Read mode

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after delay at t_{OE} from the falling edge of $\overline{OE}$, assuming that CE has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby mode

The 27C256 has a standby mode which reduces the maximum active current from 50 mA to 1 mA. The 27C256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two line output control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows :

a) the lowest possible memory power dissipation,

b) complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{CE}$ should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

System considerations

The power switching characteristics of CMOS-E4 EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{CE}$. The magnitude of this transient current peaks

is dependent on the ouput capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitors should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array.

The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

7 - PROGRAMMING MODES

Caution : exceeding 14 V on V_{PP} pin will permanently damage the 27C256.

When delivered, and after each erasure, all bits of the 27C256 are in the «1» state. Data is introduced by selectively programming «0s» into the desired bit locations. Although only «0s» will be programmed, both «1s» and «0s» can be present in the data word. The only way to change a «0» to a «1» is by ultraviolet light erasure. The 27C256 is in the programming mode when the V_{PP} input is at 12.75 V and $\overline{CE}$ is at TTL-low.

The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25 V ± 0.25 V.

7.1 · Very fast and reliable programming algorithm = PRESTO II

PRESTO II programming algorithm, available for the 27C256, is an enhancement of the PRESTO algorithm used for the 27C1024.

During programming and verify operation a MARGIN MODE™ Circuit is automatically activated. It provides adequate margin on threshold voltage of programmed cells, thus writing margin is independent from V_{CC} in verify mode and over program pulse is not necessary, reducing programming time down to a theoretical value of 3 seconds.

Program inhibit

Programming of multiple 27C256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel 27C256 may be common. A TTL low-level pulse applied to a 27C256's $\overline{CE}$ input, with V_{PP} at 12.75 V, will program that 27C256. A high level $\overline{CE}$ input inhibits the other 27C256s from being programmed. V_{CC} is specified to be 6.25 V ± 0.25 V.

Program verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH}, V_{PP} at 12.75 V and V_{CC} at 6.25 V ± 0.25 V.

7.2 · Electronic signature

The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C256. To activate this mode, the programming equipment must force 11.5 V to 12.5 V on address line A9 of the 27C256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the TMS 27C256, these two identifier bytes are given here below, and can be read-out on outputs Q1 to Q8.

Table 8 - Electronic signature mode

Identifier \ Pins	A0	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Hex
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20
Device code	V_{IH}	1	0	0	0	1	1	0	1	8D

Notes : A9 = 12 V ±0.5 V ; $\overline{CE}$, $\overline{OE}$ = V_{IL} ; A1-A8, A10-A14 = V_{IL}.

7.3 · Erasure operation

The erasure characteristic of the 27C256 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstrom A. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 A range. Data shows that constant exposure to room level fluorescent lighting could erase a typical 27C256 in about 3 years, while it would take approximately 1 week to cause erasure when expose to direct sunlight. If the 27C256 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the 27C256 window to prevent unintentional erasure. The recommended erasure procedure for the 27C256 is exposure to short wave ultraviolet light which has wavelength 2537 A. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 uW/cm² power rating. The 27C256 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

7.4 · Programming operation

Table 9 - DC and operating characteristic
T_A = 25°C ±5°C, V_{CC} (1) = 6.25 V ±0.25 V, V_{PP} (1) = 12.75 V ±0.25 V

Symbol	Parameter	Test Conditions (see Note 1)	Min	Max	Unit
I_{LI}	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10	µA
V_{IL}	Input low level (all inputs)		−0.1	0.8	V
V_{IH}	Input high level		2.0	V_{CC} +0.5	V
V_{OL}	Output low voltage during verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output high voltage during verify	I_{OH} = −400 µA	2.4		V
I_{CC2}	V_{CC} supply current			50	mA
I_{PP2}	V_{PP} supply current (program)	CE = V_{IL}		50	mA
V_{ID}	A9 electronic signature voltage		11.5	12.5	V

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10 - AC characteristics

Symbol	Parameter	Test Conditions (see Note 1)	Min	Max	Unit
t_{AS}	Address setup time		2		µs
t_{OES}	OE setup time		2		µs
t_{DS}	Data setup time		2		µs
t_{AH}	Address hold time		0		µs
t_{DH}	Data hold time		2		µs
t_{DFP} (see Note 2)	Output enable output float delay		0	130	ns
t_{VPS}	V_{PP} setup time		2		µs
t_{VCS}	V_{CC} setup time		2		µs
t_{PW}	Initial program pulse width		95	105	µs
t_{OE}	Data valid from OE			100	ns

Note 1 : V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
Note 2 : This parameter is only sampled and not 100 % tested.
Output Float is defined as the point where data is no longer driven (see timing diagram).

7

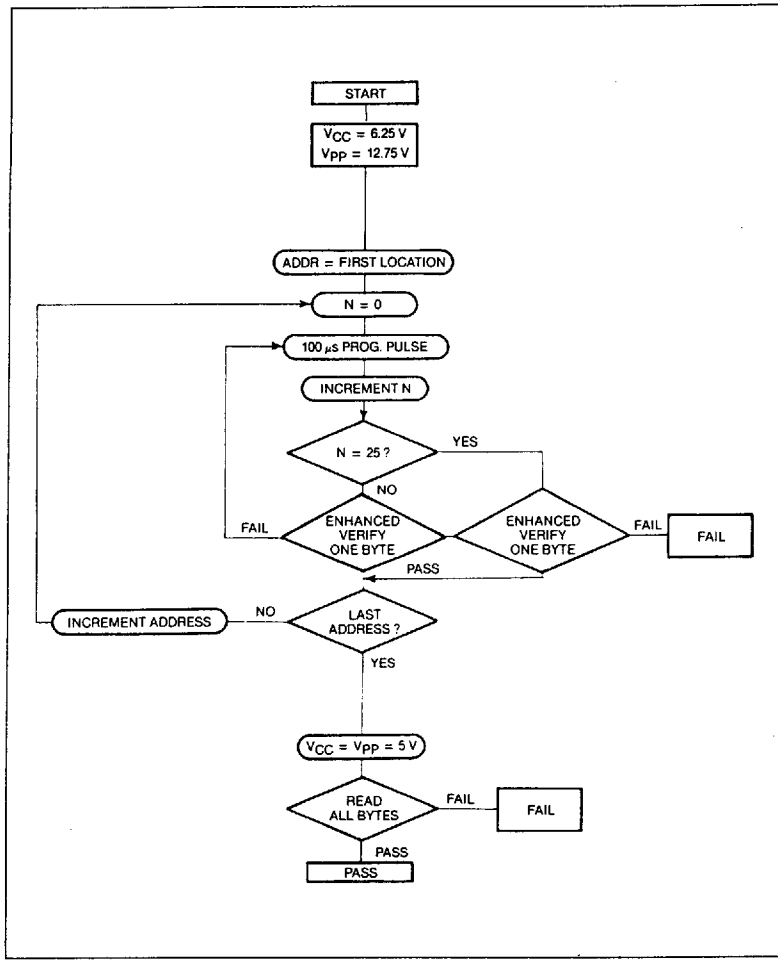
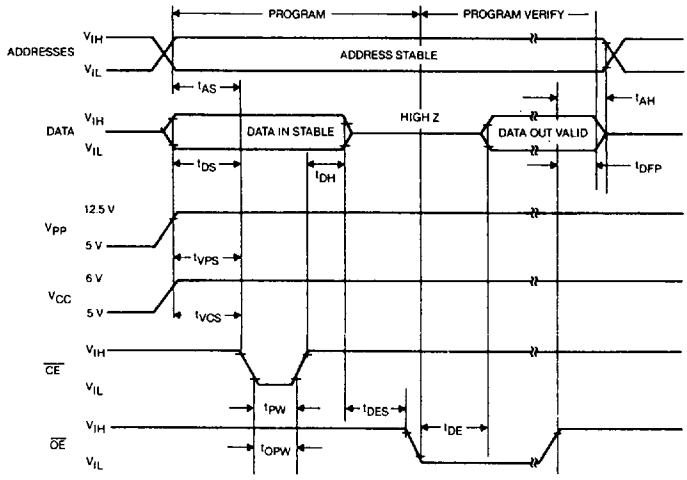


FIGURE 8 - PRESTO II PROGRAMMING ALGORITHM FLOWCHART.



Note 1 : The input timing reference level is 0.8 V for a V_{IL} and 2 V for a V_{IH}.

Note 2 : t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

Note 3 : When programming the 27C256, a 0.1 µF capacitor is required across V_{PP} and GND to suppress spurious voltage transients which can damage the device.

FIGURE 9 - PROGRAMMING WAVEFORMS

8 - PREPARATION FOR DELIVERY

8.1 - Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

8.2 - Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at extreme temperature for the entire temperature range.

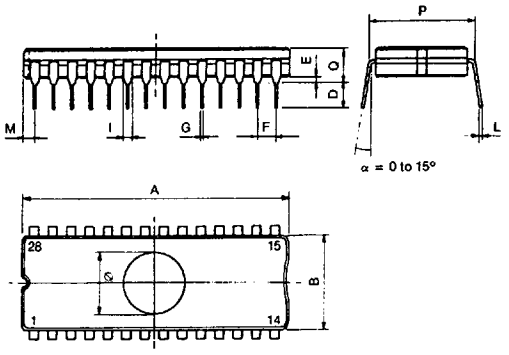
9 - HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.
b) Ground test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 percent, if practical.

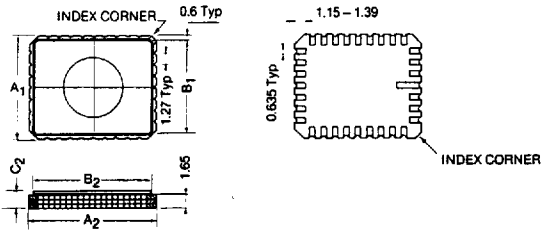
10 · PACKAGE MECHANICAL DATA

10.1 · 28 pins - DIL Cerdip with window



Symbol	Millimeters		
	Min	Typ	Max
A			37.85
B	12.7		15.49
D	3.81		
E	0.38		1.52
F	2.29		2.79
G	0.35		0.58
I	0.96		1.65
L	0.20		0.38
M			2.54
P	14.98		15.75
Q			5.89
∅		7.11	

10.2 · 32 pins - Leadless Ceramic Chip Carrier with window



Symbol	Millimeters	
	Min	Max
A_1	11.3	11.63
A_2	13.72	14.22
B_1		11.63
B_2		14.17
C_2	1.78	2.92

11 - ORDERING INFORMATION

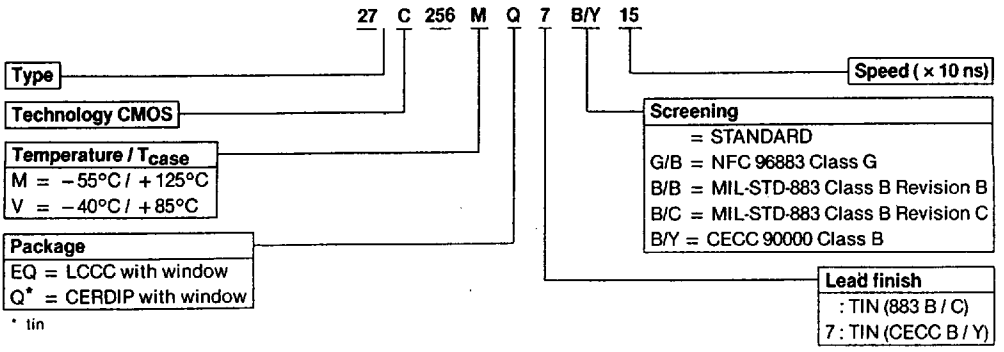
11.1 - HI-REL product

TMS part-number (1)	Norms	Package	Temperature range T_C (°C)	T_{ACC} (µs)	Drawing number
27C256MQG/B15	NFC 96883 - Class G	Cerdip 28	– 55 / + 125	150	TMS data sheet
27C256MQG/B20	NFC 96883 - Class G	Cerdip 28	– 55 / + 125	200	TMS data sheet
27C256MQG/B25	NFC 96883 - Class G	Cerdip 28	– 55 / + 125	250	TMS data sheet
27C256MEQG/B15	NFC 96883 - Class G	LCCC 32	– 55 / + 125	150	TMS data sheet
27C256MEQG/B20	NFC 96883 - Class G	LCCC 32	– 55 / + 125	200	TMS data sheet
27C256MEQG/B25	NFC 96883 - Class G	LCCC 32	– 55 / + 125	250	TMS data sheet
27C256MQ7B/Y15	CECC 90000	Cerdip 28	– 55 / + 125	150	CECC 90113-001
27C256MQ7B/Y20	CECC 90000	Cerdip 28	– 55 / + 125	200	CECC 90113-001
27C256MQ7B/Y25	CECC 90000	Cerdip 28	– 55 / + 125	250	CECC 90113-001
27C256MEQ7B/Y15	CECC 90000	LCCC 32	– 55 / + 125	150	CECC 90113-001
27C256MEQ7B/Y20	CECC 90000	LCCC 32	– 55 / + 125	200	CECC 90113-001
27C256MEQ7B/Y25	CECC 90000	LCCC 32	– 55 / + 125	250	CECC 90113-001
27C256MQB/C15	MIL-STD-883 C	Cerdip 28	– 55 / + 125	150	TMS data sheet
27C256MQB/C20	MIL-STD-883 C	Cerdip 28	– 55 / + 125	200	TMS data sheet
27C256MQB/C25	MIL-STD-883 C	Cerdip 28	– 55 / + 125	250	TMS data sheet
27C256MEQ1B/C15	MIL-STD-883 C	LCCC 32	– 55 / + 125	150	TMS data sheet
27C256MEQ1B/C20	MIL-STD-883 C	LCCC 32	– 55 / + 125	200	TMS data sheet
27C256MEQ1B/C25	MIL-STD-883 C	LCCC 32	– 55 / + 125	250	TMS data sheet
(1) THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.					

7

11.2 - Standard product

TMS part-number (1)	Norms	Package	Temperature range T_C (°C)	T_{ACC} (µs)	Drawing number
27C256MQ15	TMS Standard	Cerdip 28	– 55 / + 125	150	
27C256MQ20	TMS Standard	Cerdip 28	– 55 / + 125	200	
27C256MQ25	TMS Standard	Cerdip 28	– 55 / + 125	250	
27C256MEQ15	TMS Standard	LCCC 32	– 55 / + 125	150	
27C256MEQ20	TMS Standard	LCCC 32	– 55 / + 125	200	
27C256MEQ25	TMS Standard	LCCC 32	– 55 / + 125	250	
(1) THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.					


27 C 256 M Q 7 B/Y 15
Type
Technology CMOS
Temperature / Tcase
M = −55°C / +125°C
V = −40°C / +85°C
Package
EQ = LCCC with window
Q* = CERDIP with window
* tin
Screening
= STANDARD
G/B = NFC 96883 Class G
B/B = MIL-STD-883 Class B Revision B
B/C = MIL-STD-883 Class B Revision C
B/Y = CECC 90000 Class B
Lead finish
: TIN (883 B / C)
7 : TIN (CECC B / Y)
Speed (x 10 ns)