

High Performance

32x8 Ti-W PROM

53/63S080 53/63S081

Features/Benefits

- 9ns typical access time
- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage generic programming
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current

Applications

- Programmable logic element
- Address decoder
- Priority encoder
- Random logic replacement

Description

The 53/63S080 and 53/63S081 features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

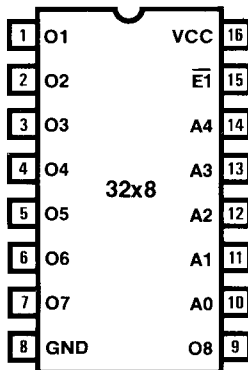
The 53/63S080 and 53/63S081 are programmed with the same programming algorithm as all other Monolithic Memories' generic Ti-W PROMs. For details refer to Monolithic Memories' LSI Data Book.

Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	-55°C to +125°C
1/4 K	32x8	O.C.	16	N, J	63S080	53S080
		T.S.			63S081	53S081

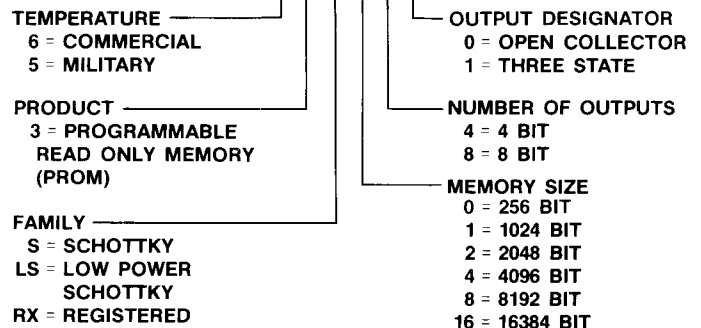
Pin Configuration

53/63S080
53/63S081



Part Numbering System

63S081



Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Off-state output voltage	5.5V
Storage temperature	-65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT		
		MIN	TYP	MAX	MIN	TYP	MAX			
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V		
T_A	Operating free-air temperature	55			125			0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage			0.8			V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18\text{mA}$	-1.5			V
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$	-0.25			mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$	40			mA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$ $V_{IL} = 0.8\text{V}$ $V_{IH} = 2\text{V}$	$I_{OL} = 16\text{mA}$	MIL	0.5		V
				COM	0.45		
V_{OH}	High-level output voltage*	$V_{CC} = \text{MIN}$ $V_{IL} = 0.8\text{V}$ $V_{IH} = 2\text{V}$	MIL $I_{OH} = -2\text{mA}$	2.4		V	
			COM $I_{OH} = -3.2\text{mA}$				
I_{OZL}	Off-state output current *	$V_{CC} = \text{MAX}$	$V_O = 0.4\text{V}$	-40		μA	
I_{OZH}			$V_O = 2.4\text{V}$	40		μA	
I_{CEX}	Open collector output current	$V_{CC} = \text{MAX}$	$V_O = 2.4\text{V}$	40		μA	
			$V_O = 5.5\text{V}$	100			
I_{OS}	Output short-circuit current**	$V_{CC} = 5\text{V}$	$V_O = 0\text{V}$	-20	-90	mA	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$	All inputs grounded. All outputs open.	90	125	mA	

* Three-state only

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†Typicals at 5.0V V_{CC} and 25°C TAA

Switching Characteristics

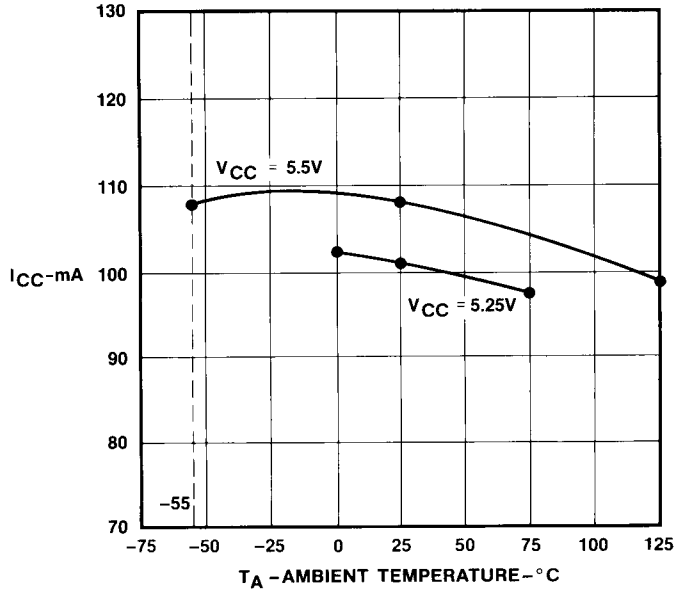
Over Commercial Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS AND RECOVERY TIME		CONDITIONS (See standard test load)	
	TYP†	MAX	TYP†	MAX	R1(Ω)	R2(Ω)
63S080/1	9	25	9	20	300	600
53S080/1	9	35	9	30		

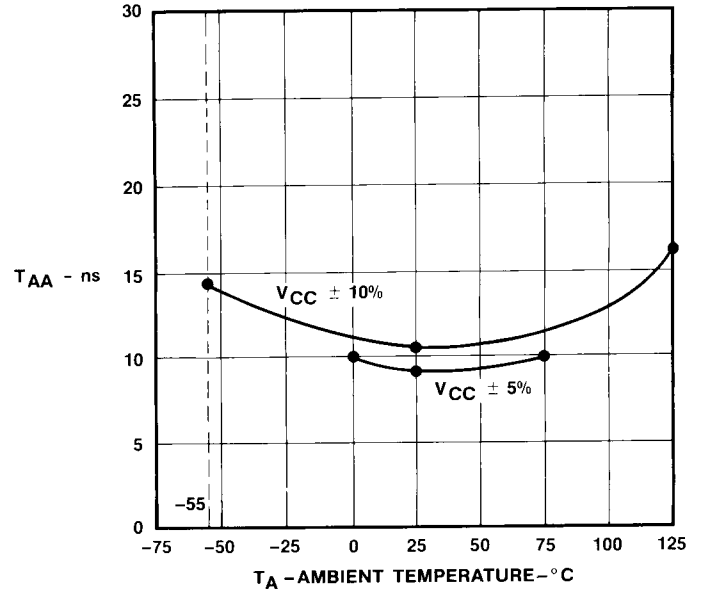
†Typicals at 5.0 V_{CC} and 25°C TA.

53/63S081

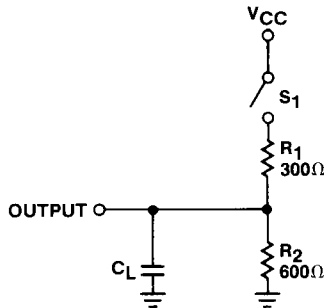
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature



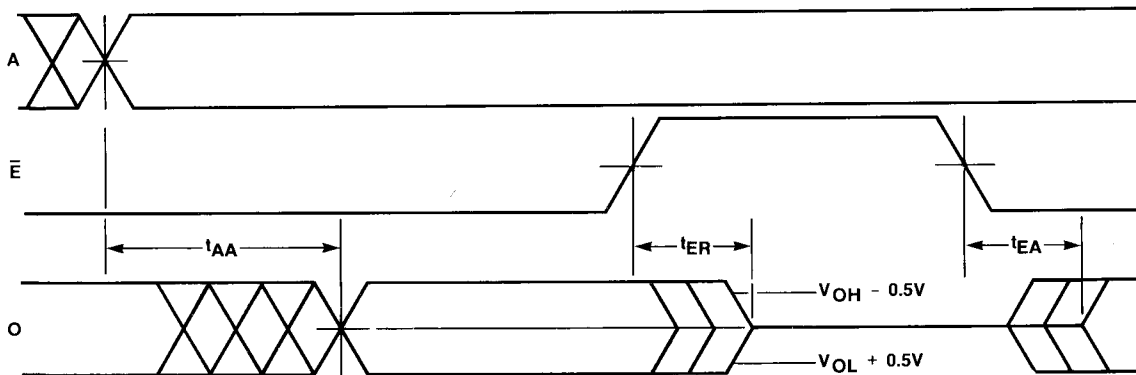
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 5ns from 1.0V to 2.0V.

3. Input access measured at the 1.5V level.

4. t_{AA} is tested with switch S_1 closed, $C_L = 30pF$ and measured at 1.5V output level.

5. For open collector devices, TEA and TER are measured at the 1.5V output level with S_1 closed and $C_L = 30pF$.

6. For three-state devices, TEA is measured at the 1.5V output level with $C_L = 30pF$. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

TER is tested with $C_L = 5 pF$. S_1 is open for "1" to high impedance test, measured at $V_{OH} - 0.5$ output level; S_1 is closed for "0" to high impedance test measured at $V_{OL} + 0.5V$ output level.

Monolithic Memories

Americas

Monolithic Memories

1165 East Arques Avenue
Sunnyvale, CA 94086
Phone (408) 739-3535
Telex (910) 339-9229

France

Monolithic Memories France S.A.R.L.

Silic 463
F 94613 Rungis Cedex
France
Phone 1-6874500
Telex 202146
Fax 1-6876825

Japan

Monolithic Memories Japan KK

4-5-15, Sendagaya
Shibuya-Ku
Tokyo 151
Japan
Phone 3-4039061
Telex 781-26364
Fax 3-4040570

England

Monolithic Memories, Ltd.

Lynwood House
1 Camp Road
Farnborough, Hampshire
United Kingdom GU146EN
Phone (0252) 517431
Telex 858051 MONO UKG
Fax (0252) 43724

Germany

Monolithic Memories, GmbH

Mauerkircherstr 4
D 8000 Munich 80
West Germany
Phone 89-984961
Telex 524385
Fax 89-983162

Monolithic Memories reserves the right to make changes in order to improve circuitry and supply the best product possible.

Monolithic Memories cannot assume responsibility for the use of any circuitry described other than circuitry entirely embodied in their product. No other circuit patent licenses are implied.