Interfacing the 6800 Microprocessor to National CMOS MM74C910 Memory

National Semiconductor
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INTRODUCTION

The applications of solid state non-volatile memory are numerous. One such application involves an Area Navigation System used on aircraft. Waypoint information can be conveniently stored upon engine shutdown and becomes readily available at power-up. This is especially useful for cross-country flying so that the same waypoint data does not have to be entered into the Area Navigation System at each aircraft takeoff.

6800 AND MM74C910 INTERFACE

A 6800 is utilized in the Area Navigation System for processing and computations. Figure 1 shows a block diagram of the system which includes 2k x 8 ROM and 64 x 4 RAM.

Non-volatile memory for waypoint storage is obtained by usage of the MM74C910. This device is a 64-word by 4-bit RAM consisting of six address lines, four data input lines, four data output lines, a Write Enable ($\overline{WE}$) and a Memory Enable ($\overline{ME}$). Typical supply current for the device is 0.05 μA.

Interface of the 6800 and MM74C910 is accomplished via the DS8T28 Bus Transceiver. However, additional hardware and software are required to extend the data time on the bus to read and write 4-bit data. (Two MM74C910 CMOS RAMs organized by 8-bit words would simplify software.)

Figure 2 shows the clock circuit hardware required to extend the data time during Write. Clock phase 2 is extended from 500 ns to 550 ns by increasing the time constant of the Monostable generator. The output is passed through one NAND and two INVERTER circuits to the Data Bus Enable input of the microprocessor. A data extension of approximately three gate delays is thereby accomplished, allowing Data Input Hold Time t_{HD} (min) of 30 ns to be met before $\overline{WE}$ from the 6800 goes high. When the MM74C910 is not being accessed the Data Bus Enable input of the 6800 is high and the clock 1 and clock 2 monostable generators are a symmetrical 500 ns.

CONCLUSION

National CMOS RAMs are competitive in solid-state non-volatile memory applications. Projections for battery life of 10 years have been made using lithium batteries with average current drains of 10 μA.

One other approach using MOS technology for Electrically Alterable ROMs can be competitive in larger systems, although the Read Cycle of approximately 20 ms and the Write Cycle of approximately 60 ms are prohibitively long compared to those of CMOS RAMs.

*Refer to Introduction.

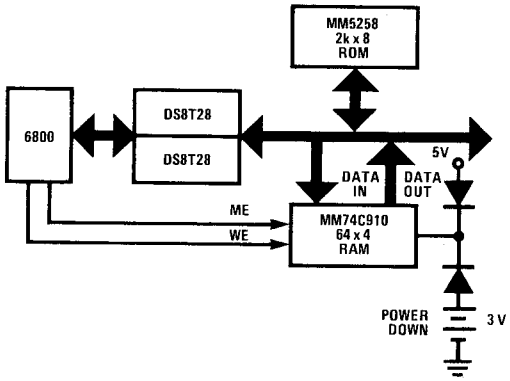

Figure 1.

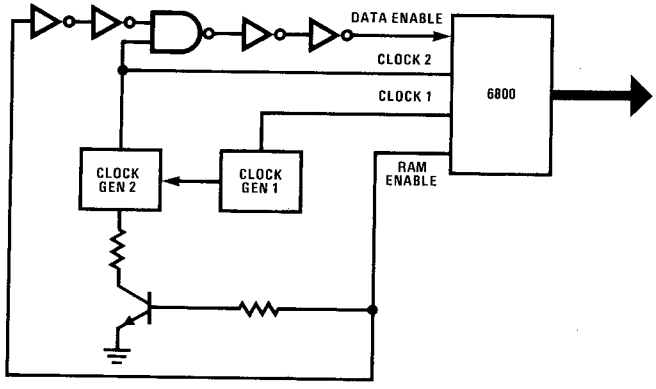

Figure 2.