CHAPTER 5
HARDWARE APPLICATIONS

5.1 INTRODUCTION

When the initial microprocessors appeared in the marketplace, the actual on-chip circuitry was extremely limited. This required the use of a large number of devices just to support the actual processor. However, as technology progressed much of the support hardware was included on-chip with the processor. The M6805 HMOS/M146805 CMOS Family now includes standard on-chip features such as: an oscillator, ROM, RAM, timer, and a wide variety of I/O devices. Combining these standard features with other features such as analog-to-digital conversion, phase-lock-loop, etc. onto a single chip simplifies system design efforts while reducing production costs.

This chapter contains discussions and examples of applications which describe how some of these on-chip hardware features may be used and enhanced. The first paragraphs provide discussions of some of the features, whereas, the latter paragraphs describe application examples which perform real tasks.

The evaluation ROM devices for each member of the M6805 HMOS/M146805 CMOS Family contain evaluation examples which can be used to better understand the device. Many of the evaluation examples have been used to perform real tasks, and many of these are described in various Motorola application notes.

One paragraph of this chapter is dedicated to CMOS design considerations. This discussion highlights the somewhat different design considerations required when designing a system using CMOS.

5.2 I/O EXPANSION

The M6805 HMOS/M146805 CMOS Family devices may require interfacing with other peripherals. Several representative descriptions are provided in this paragraph, all of which are in general terms except for the MC146805E2 MPU.

5.2.1 MC146805E2 Microprocessor Unit (MPU)

The MC146805E2 MPU is the only member of the M6805 HMOS/M146805 CMOS Family that has no on-chip ROM; however, it does use a multiplexed address/data bus to interface with external memory or peripherals. Multiplexed bus memory peripheral interfacing techniques are discussed below. In addition, the MC146805E2 can also be interfaced with non-multiplexed bus memory peripherals, and this technique is also discussed

below. In some applications it is necessary to interface the MC146805E2 with peripherals which require longer access times ("slow memory"). A discussion of this technique is also included as part of this paragraph.

5.2.1.1 INTERFACING MULTIPLEXED BUS MEMORY WITH PERIPHERALS. A multiplexed bus device is characterized by an address latch and an output enable signal. The address latch captures the lower eight bits of the address from the multiplexed bus, and the output enable signal is used to determine when data can be safely transferred. The circuit in Figure 5-1 illustrates a typical multiplexed bus interface. This figure provides a detailed representation of the minimum circuit required to use the CBUG05 debug monitor which is contained in the MCM65516 2K × 8 CMOS ROM. A complete description of the CBUG05 can be found in Motorola Application Note AN-823.

The circuit shown in Figure 5-1 consists entirely of CMOS devices. The system could be expanded easily by adding CMOS RAM, ROM, EPROM, or peripherals such as MC146818 real time clock or the MC146823 CMOS peripheral interface.

The MCM65516 ROM uses the AS signal from the MC146805E2 to latch the multiplexed address and the DS signal to transfer data. The data transfer direction is controlled by the R/$\overline{W}$ signal. Since the MCM65516 ROM is a read-only device, R/$\overline{W}$ is used together with A11 and A12 to provide the chip select and enable lines to ensure that an inadvertant write does not cause a bus conflict. The chip enable and select lines on the MCM65516 are mask programmable as either active high or active low; therefore, no external address decoding is necessary in this example. A second example is discussed below which uses an MC146823 CMOS peripheral interface to emulate the C and D ports of the MC146805G2.

5.2.1.2 INTERFACING NON-MULTIPLEXED BUS MEMORY WITH PERIPHERALS. Since the majority of existing memory and peripheral devices use a non-multiplexed bus, an interface with the MC146805E2 can be relatively simple. The main difference between multiplexed and non-multiplexed memory and peripheral devices is the absence of an address latch in non-multiplexed bus devices. The non-multiplexed bus devices require that all address lines be valid for the entire cycle. In order to provide this valid address to a non-multiplexed memory or peripheral device, the MC146805E2 multiplexed bus can be demultiplexed merely by adding an external address latch. This is illustrated in Figure 5-2 which uses an MC74HC373 to demultiplex the bus for the non-multiplexed MCM27C16 EPROMs. The multiplexed address lines (B0-B7 of the MC146805E2) are latched in the MC74HC373 by the falling edge of address strobe (AS). They remain latched until AS goes high. The emulator shown in Figure 5-2 is further discussed in the Emulating The MC146805G2 MCU paragraph.

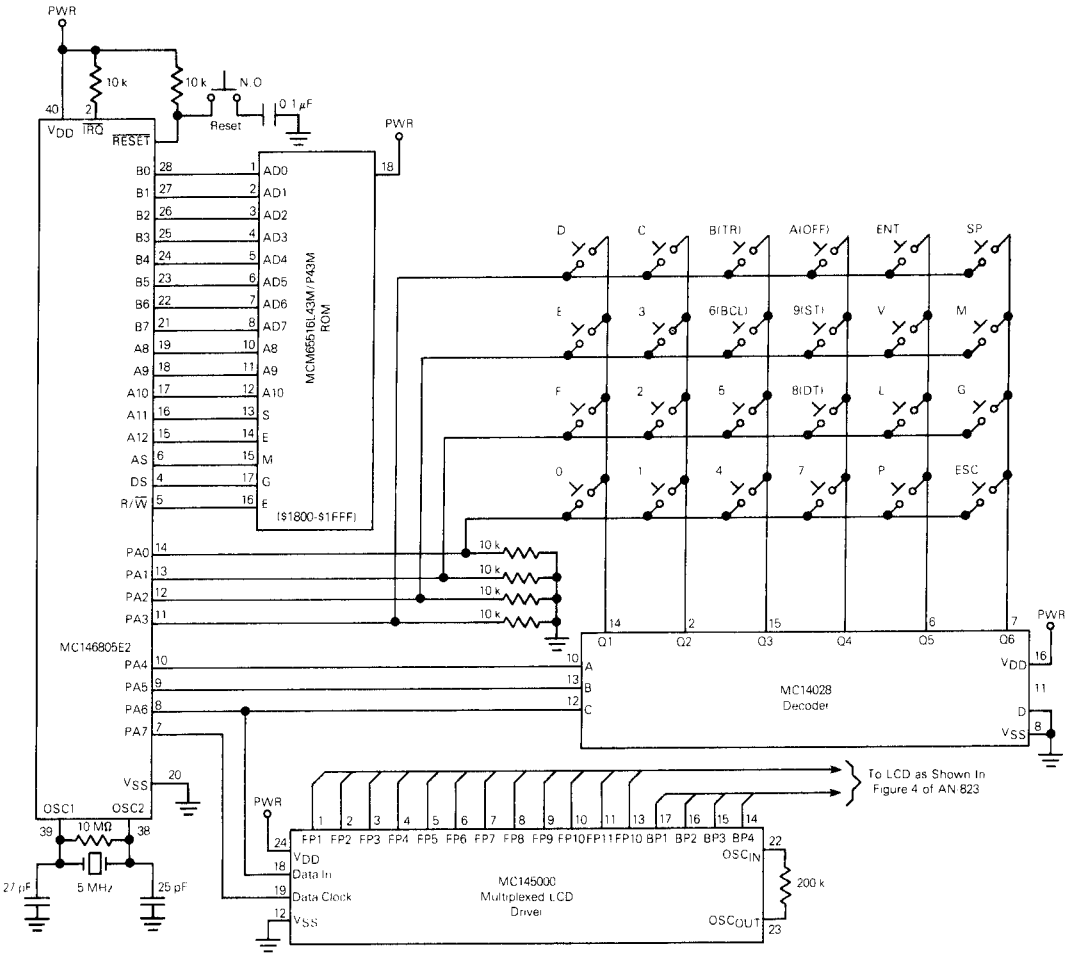
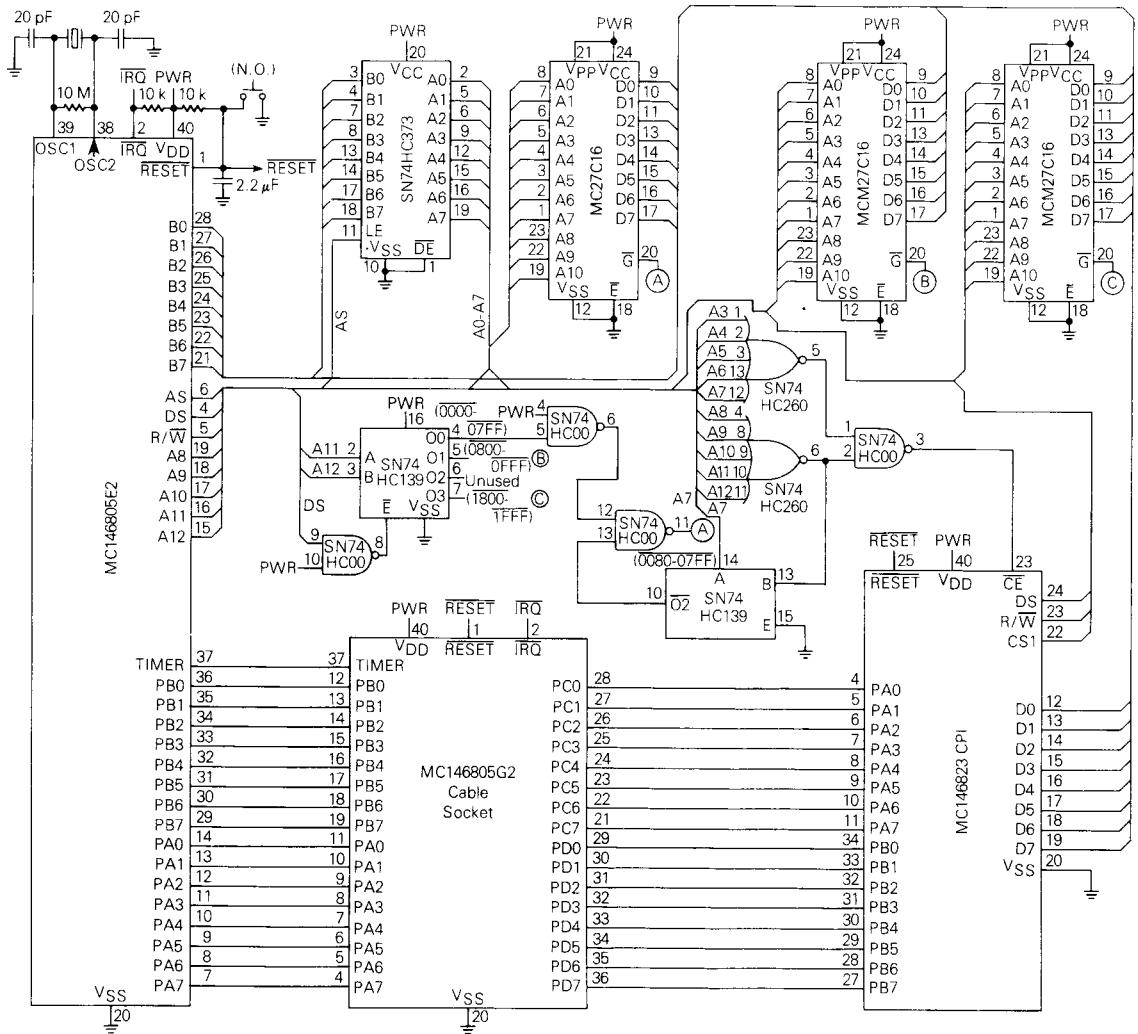


Figure 5-1. CBUG05 Debug Monitor Minimum CMOS Only System, Schematic Diagram



5-2. MC146805G2 Emulator Schematic Diagram

5.2.1.3 INTERFACING WITH SLOW MEMORY AND PERIPHERAL DEVICES. At times, it is desirable to use memory or peripheral devices which require both chip enable and output enable. In these devices, the access time is calculated from when chip enable is valid, whereas, output enable simply opens the gates to the external bus.

The emulator circuit of Figure 5-2 shows an interface with an MC146805E2 and an MCM27C16; however, slow, single-supply SC682716 EPROMs could be used. Note that the chip enable ($\overline{E}$) of the MCM27C16 EPROM is continuously held low. This allows the address to be gated by using the MC146805E2 DS signal to generate the output enable ($\overline{G}$). The DS signal is actually used in decoder SN74HC139 to generate three $\overline{G}$ inputs, one for each EPROM. In this type of interface, the output enable time is the limiting factor and it is typically much shorter than the access time. On most devices power consumption increases when this type of interface is used.

5.2.1.4 EMULATING THE MC146805G2 MCU. The circuit shown in Figure 5-2 illustrates the use of each of the three interfacing techniques to allow the MC146805E2 MCU to provide real-time emulation for the MC146805G2 Microcomputer (MCU). In the circuit of Figure 5-2 all devices are CMOS; however, the actual MC146805G2 power consumption will be approximately 20% of that consumed by the emulator. More information concerning MC146805G2 emulation, as well as other MCUs, is contained in Motorola Application Note AN-853.

5.2.2 Single-Chip Microcomputer (MCUs)

The increased circuit density of single-chip MCUs greatly reduces the need for additional hardware external to the MCU itself. By combining as much I/O as needed on a single integrated circuit device, the cost is lowered and reliability increased. Since the probability of system failure increases with each added system component, system reliability increases as a result of more system components being designed into a single-chip MCU.

The single-chip MCUs which are part of the M6805 HMOS/M146805 CMOS Family continue to grow in order to fill the diversity of I/O needs in the controller market; however, some applications may require I/O functions that are not yet included, or are unsuitable for inclusion, as part of the single-chip MCU. Whatever the reason, the MCU must provide a means for using external devices in a system.

All M6805 HMOS/M146805 CMOS MCUs contain programmable bidirectional I/O lines; however, the actual number of these I/O lines may vary between specific MCUs. In all cases an external interface may be simulated by properly manipulating these lines. The MC145000 LCD driver interface described in Chapter 3 is an example of such an interface.

More complicated interfaces may be simulated as shown in Figure 5-3. This example combines the MC146818 real-time clock with an M6805 HMOS/M146805 CMOS Family MCU. Eleven I/O lines are used in this interface to provide the multiplexed bus required by the MC146818. If an interface requiring more lines were used, a peripheral interface adapter (PIA), latch, or input buffer could be added to increase the effective number of I/O lines.

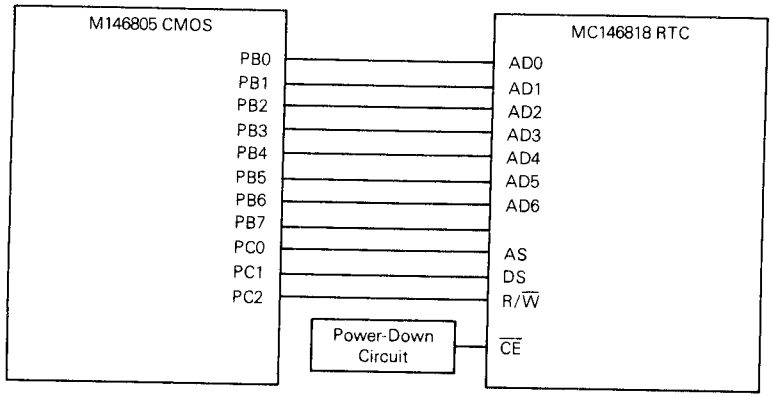


Figure 5-3. MCU Interface With Multiplexed Bus Peripheral

All MCU interfaces require some amount of software overhead. The software requirement for the MC146818 interface is illustrated in Figure 5-4. The MC146818 multiplexed bus requires that signals and transitions occur in specific order. The software of Figure 5-4 guarantees that these timing requirements are met.

```
*       INITIALIZATION OF I/O LINES
PORTB   EQU     1
PORTC   EQU     2
DDRB    EQU     5
DDRC    EQU     6
AS      EQU     0
DS      EQU     1
RW      EQU     0
ADDR    RMB     1           ADDRESS OF BYTE TO BE ACCESSED
INIT    CLR     PORTC       CLEAR PORT C OUTPUT DATA LATCH
        CLR     PORTB       CLEAR PORT B OUTPUT DATA LATCH
        LDA     #$FF        CONFIGURE PB0-PB7 AS OUTPUT
        STA     DDRB
        LDA     #7          CONFIGURE PC0-PC2 AS OUTPUTS
        STA     DDRC
        RTS                 RETURN
*        READ MC146818
READ    BSET    RW,PORTC    FORCE R/W AND AS HIGH
        BSET    AS, PORTC
        LDA     ADDR        PRESENT MUXED ADDRESS
        STA     PORTB
        BCLR    AS,PORTC    FORCE AS LOW TO LATCH MUXED ADDRESS
        CLR     DDRB        CONFIGURE PORT B AS INPUTS
        BSET    DS,PORTC    READ DS HIGH
        LDA     PORTB       READ DATA
        STA     DATA        STORE DATA IN RAM FOR LATER USE
        BRA     INIT        REINITIALIZE LINES AND RETURN
*        WRITE MC146818
WRITE   BSET    AS,PORTC    FORCE AS HIGH
        LDA     ADDR        PRESENT MUXED ADDRESS
        STA     PORTB
        BCLR    AS,PORTC    FORCE AS LOW TO LATCH MUXED ADDRESS
        LDA     DATA        PRESENT WRITE DATA
        STA     PORTB
        BSET    DS,PORTC    TOGGLE DS TO LATCH DATA INTO MC146818
        BCLR    DS,PORTC
        BRA     INIT        REINITIALIZE LINES AND RETURNS
```

Figure 5-4. MCU to MC146818 Interface Software

5.3 PERIODIC WAKE-UP FROM WAIT MODE

The timer may be used to generate a signal which causes a member of the M146805 CMOS Family to exit from the WAIT mode. The WAIT instruction (like the STOP instruction) places the MPU or MCU into a low-power mode which may be exited by using either a reset or an external interrupt; however, unlike the STOP mode, the WAIT mode does not disable the timer. In the WAIT mode, the timer interrupt can also cause the processor to exit the WAIT mode and begin execution of the program pointed to by the timer wait interrupt vector. This feature of using the timer interrupt to periodically "wake-up" the processor, is extremely useful in systems that require the lowest possible power consumption and at the same time require infrequent processor control. In these systems, the processor is "put to sleep" and periodically "awakened" by the timer interrupt.

The example shown in Figure 5-5 is similar to the keyscan example described in Chapter 3. The main difference between the examples is that the keyscan routine uses the external interrupt to exit the STOP mode; whereas, the example of Figure 5-5 uses the internal bus frequency (clock) to exit the WAIT mode. Power comsumption using the WAIT mode is slightly higher than the STOP mode. This is because the timer is active and consumes power during the WAIT mode. Also, in the example of Figure 5-5, the data at ports A and B are compared (using the SUB instruction) and the difference is outputted at port C every 298 internal clock cycles. No external hardware, except as necessary to guard against possible CMOS latch-up, is necessary.

```
PORTA   EQU   0
PORTB   EQU   1
PORTC   EQU   2
DDRC    EQU   6
TDR     EQU   8
TCR     EQU   9
RESET   CLR   PORTC   INITIALIZE PORT C OUTPUT DATA LATCH
        LDA   #$FF    CONFIGURE PORT C AS OUTPUT PINS
        STA   DDRC
        LDA   #$20    DISABLE TIMER
        STA   TCR
PAUSE   LDA   #$F9    LOAD TIMER DATA REGISTER
        STA   TDR
        LDA   #$00    ENABLE TIMER INTERRUPT AND FOR INTERNAL INPUT
        STA   TCR
        WAIT          ENTER LOW POWER WAIT MODE
        BRA   PAUSE   RETURN HERE AFTER INTERRUPT IS SERVICED

TWIRQ   BCLR  7,TCR   CLEAR TIMER INTERRUPT
        LDA   PORTA   READ PORT A REGISTER INPUT DATA
        SUB   PORTB   FIND DIFFERENCE
        STA   PORTC   OUTPUT DIFFERENCE TO PORT C
        RTI           RETURN FROM INTERRUPT
```

Figure 5-5. Timer Wait Mode Exit Software

5.4 INTERRUPTS

The $\overline{IRQ}$ or $\overline{INT}$ pins on the M6805 HMOS/M146805 CMOS Family may be used in many different interrupt-type applications. An interrupt is used either as a request by a peripheral for MPU/MCU service or as a flag to the MPU/MCU which indicates the occurrence of some event. The following paragraphs provide descriptions in which the interrupt line is used as a flag for the processor.

5.4.1 Exiting From STOP Mode

The STOP instruction is used in the M146805 CMOS Family to enter a low-power operating mode. In most MPU/MCU applications, there are intervals in which no processing, except to wait for an event to occur, is required. The example described in Chapter 3 of the 4 × 4 keypad interface is a typical example. One of the features of this keypad interface is that the processor enters the low-power STOP mode and remains there until a valid keypad switch closure occurs. When a key is depressed, the $\overline{IRQ}$ line is pulled low. This causes the processor to exit the STOP mode and enter the interrupt service routine. The interrupt service routine polls (scans) the keypad rows and columns to determine which key was depressed. After the depressed key location is verified, the interrupt service routine is exited. Processing then continues at the instruction that follows the STOP instruction that was last executed.

The location of the depressed keypad key may be used in conjunction with a jump table to initiate the execution of any one of a number of routines, or a conversion table to translate the key location into a value or a character. When keypad input is required, all that need be done to accept it is to execute the STOP instruction. The interrupt mask is automatically cleared by the STOP instruction, the depressed keypad key causes an interrupt, and the depressed key location is returned in the accumulator.

5.4.2 60 Hz Interrupt For Time of Day Clock

By attenuating the 60 Hz standard 110 Vac power line and inputting this signal into the M6805 HMOS/M146805 CMOS Family MCU as shown in Figure 5-6, a time of day clock can be controlled. Since the 60 Hz line voltage is constantly monitored and regularly corrected by the power company, its average frequency is maintained as close to 60 Hz as possible. This accurate frequency and ready availability make the standard power line ideal for accurate timekeeping. The circuit shown in Figure 5-6 first attenuates the line voltage to a level that meets the maximum input voltage specification of the $\overline{INT}$ pin. The capacitor serves to eliminate dc from the $\overline{INT}$ pin input and the diodes limit the peak-to-peak voltage. A Schmitt trigger, which is internal to the MPU/MCU, ensures that noise does not generate false interrupts. The diodes clamp the input ac voltage to ensure that it does not exceed the rated peak-to-peak input, while, at the same time, providing 60 falling edges per second. Thus, the MPU/MCU enters the interrupt service routine 60 times per second.

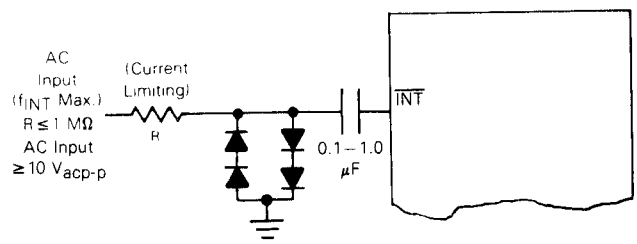


Figure 5-6. Typical Zero Crossing Interrupt Circuit Schematic Diagram

The software illustrated in Figure 5-7 is necessary to count the number of interrupts and convert that number to seconds, minutes, and hours. Also included in the software of Figure 5-7 is a procedure that initializes the clock.

```
PAGE  001  CLOCK   .SA:0

00001                          *
00002                          *  RAM VARIABLES
00003                          *
00004A 0064                          ORG    $64       ON CHIP RAM
00005                          *
00006A 0064     0004      A CLOCK  RMB    4         TIME-OF-DAY CLOCK
00007           0064      A HRS    EQU    CLOCK     HOURS IN CLOCK
00008           0065      A MINS   EQU    CLOCK+1   MINUTES IN CLOCK
00009           0066      A SECS   EQU    CLOCK+2   SECONDS IN CLOCK
00010                          *
00011A 0080                          ORG    $80
00012                          *
00013                          *  MAXIMUM COUNTER VALUES FOR TIME OF DAY
00014                          *  CHANGE 13 TO 24 FOR 24 HOUR CLOCK
00015                          *  CHANGE JIFFIES FROM 60 TO 50 FOR 50 Hz OPERATION.
00016                          *
00017A 0080     0D        A MODULO FCB    13        HOURS
00018A 0081     3C        A        FCB    60        MINUTES
00019A 0082     3C        A        FCB    60        SECONDS
00020A 0083     3C        A        FCB    60        JIFFIES  (SIXTIETH)
00021                          *
00022                          *  TICK --- 60 HZ INTERRUPT FOR TIME OF DAY CLOCK
00023                          *
00024A 0084 AE 03         A TICK   LDX    #3        BEGIN AT LSB OF CLOCK
00025A 0086 6C 64         A TICK2  INC    CLOCK,X   BUMP THIS DIGIT
00026A 0088 E6 64         A        LDA    CLOCK,X   SEE IF IT OVERFLOWED
00027A 008A E1 80         A        CMP    MODULO,X  COMPARE WITH MODULO VALUES
00028A 008C 25 07       0095       BLO    CLKOUT    DONE IF LOWER THAN MODULO
00029A 008E 6F 64         A        CLR    CLOCK,X   RESET THIS COUNTER AND
00030A 0090 5A                     DECX             GO TO NEXT WITH OVERFLOW
00031A 0091 2A F3       0086       BPL    TICK2     WHILE NOT AT HOURS COUNTER
00032A 0093 3C 64         A        INC    HRS       REMOVE FOR 24 HOUR CLOCK
00033A 0095 80               CLKOUT RTI
00034                          *
00035                          *  INTERRUPT VECTOR
00036                          *
00037A 07FA                          ORG    $7FA
00038                          *
00039A 07FA     0084      A        FDB    TICK      12/24 HOUR CLOCK VECTOR
00040                          *
00041                                END
```

Figure 5-7. Time of Day Clock Software Listing

5.5 CMOS DESIGN CONSIDERATIONS

Digital devices may be implemented in any number of processing technologies, and, as shown in Table 5-1, each processing technology has its advantages and disadvantages. For applications requiring low power consumption, CMOS has been the dominant technology; however, until recently, CMOS could not match the speeds found in other processes. With the advent of silicon-gate CMOS and the emerging high-density CMOS (HCMOS) processes, CMOS technology is not only replacing NMOS in many designs, but is responsible for a whole new field of products.

The M146805 CMOS Family of MPU/MCUs, and the M74HCXX Family of CMOS interface logic, combine the CMOS low power consumption with the speeds of NMOS/HMOS and TTL. However, since CMOS requires a larger silicon area than NMOS or HMOS, it is more expensive.

Table 5-1. Comparison of Processing Techniques

Process	Advantages	Disadvantages	Comments
TTL	Fast with high drive capability.	Consumes more power than NMOS/HMOS, CMOS or HCMOS.	TTL has a high drive capability compared to NMOS and is used in interface devices.
NMOS/HMOS	Fast, high density, inexpensive, consumes less power than TTL.	Restrictive voltage supply requirements for portable applications.	HMOS is high-speed, high-density version of NMOS.
CMOS	Consumes very little power, uses a wider voltage range than NMOS, Si-gate versions are as fast as NMOS.	More expensive than NMOS; metal-gate versions are slow.	CMOS densities are approaching those of NMOS.
HCMOS	Fast, dense, inexpensive, low-power.	Consumes more power than CMOS but less than NMOS.	Currently available in 74HCXX series of CMOS interface logic. Combines NMOS and CMOS devices to get the best of both processes.

The following two paragraphs provide a design criteria discussion that should be considered in order to use CMOS effectively and reliably. These discussions include: (1) factors that contribute to CMOS power consumption and how the effects of these factors can be reduced, and (2) the phenomenon of CMOS latch-up and how it can be avoided.

5.5.1 Power Consumption

The two factors which greatly affect CMOS power consumption are supply voltage and operating frequency. Reducing the supply voltage (V_{DD}) proportionally reduces power consumption since the EI product is lower. A "side effect" of lowering the supply voltage is a reduction in the maximum operating frequency of the device. This is the result of reduced internal drive caused by lowered V_{DD}.

The power consumption of a CMOS device is primarily affected by capacitive loading rather than resistive loading as for HMOS or NMOS. Each CMOS cell is basically composed of two complementary transistors (a P channel and an N channel), and, in the steady state, only one transistor is turned on. The active P-channel transistor sources current when the output is a logic high, and presents a high impedance when the output is a logic low. Thus, the overall result is extremely low power consumption because there is no power loss through the active P-channel transistor. Since only one transistor is turned on during the steady state, power consumption is determined by leakage currents.

During a transition, both transistors pass through the active regions of their operating characteristics. The actual time spent simultaneously in these active regions directly affects the power consumption. The higher the operating frequency, the more time is spent in these simultaneous active regions, thus, higher power consumption. By reducing the number of transitions within the CMOS device, power consumption can be reduced. Also, since power consumption depends upon the time spent in transition, the rise and fall times of the signals should be as fast as possible. This can be accomplished by minimizing capacitive loading. It is important to note that although slower operating frequencies have longer rise and fall times, the effects of this additional time are generally negligible when compared to effects of reducing operating frequency.

5.5.2 CMOS Latch-Up

Due to the required layout of CMOS devices, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become "latched" in a mode that may result in excessive current drain and eventual destruction of the device. Although the M146805 CMOS Family is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltage specification is not exceeded. Some systems may require that the CMOS circuitry be isolated from voltage transients; others may require no additional circuitry.

5.6 32-kHz OSCILLATOR

The M146805 CMOS Family can operate at frequencies down to dc; however, the on-chip oscillator cannot be used with series type crystals. Because low frequency crystals are series type, additional circuitry is necessary. To generate this clock input, an external oscillator similar to that shown in Figure 5-8 is required. The MC14069 CMOS hex inverter was chosen for this circuit because of its low power consumption, and its ability to operate in the linear region with reasonable stability. Only two resistors are required for the oscillator: bias resistor R1 ensures linear operation and R2 provides current limiting protection for the crystal. Two load capacitors (C1 and C2) ensure proper loading plus correct start-up frequency. Variable capacitor C1 also allows limited tuning of the output frequency.

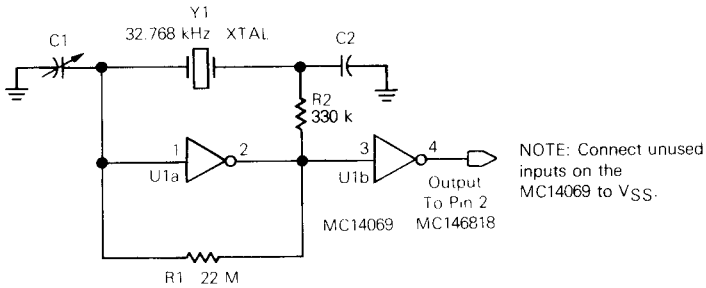
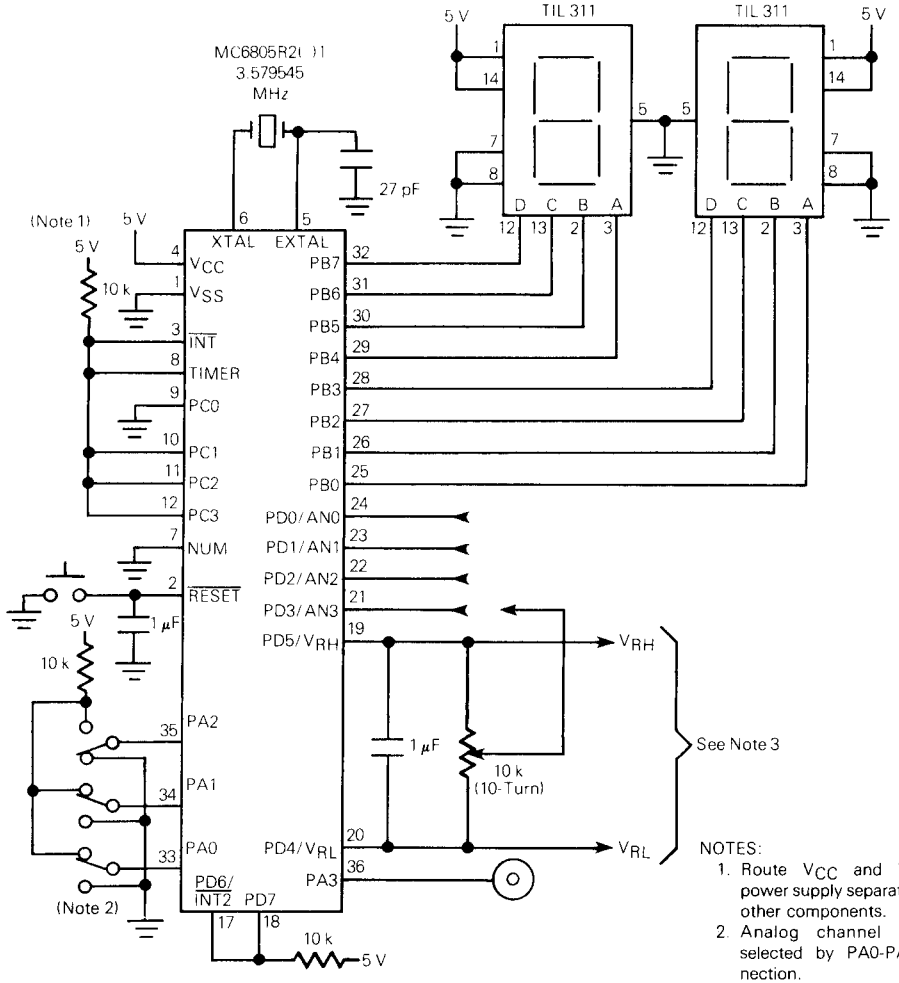


Figure 5-8. 32.768 kHz Square Wave Oscillator Schematic Diagram

The 32-kHz oscillator described above functions properly and exhibits relatively good frequency stability over ambient temperature ranges. However, there is a possibility of minor frequency variations resulting from voltage fluctuation. The 32 kHz oscillator circuit, shown in Figure 5-8, will react only slightly to a decrease in V_{DD} from 5 V down to 3.9 V. The actual change in frequency over this 1.1 V range would be about 0.1 Hz and could result in an error of about 7.9 seconds per month.

With R2 as a 330 k resistor, the oscillator is very sensitive to the values of capacitors C1 and C2, and at times the R2 value must be chosen to match the crystal. With R2 removed or decreased in value to 2 k, the oscillator is less sensitive to C1 and C2; however, it is considerably more prone to frequency changes resulting from voltage variations. For example, with R2 at a value of 2 k, a 1.1 volt change in V_{DD} could result in a 1.2 Hz frequency change. This amounts to an error of 87 seconds in a month.

In many cases, either of the above discussed errors (7.9 or 87 seconds) is not acceptable. In these cases, there are two suggestions which might be helpful. The first, and possibly the easiest to implement, is to keep the battery backup voltage equal to V_{DD}. This would require a slightly higher power consumption from the backup battery but the frequency drift would be lessened or eliminated. A second method would be to use a voltage and temperature compensated oscillator to provide a stable 32.768 kHz source. The latter method is more complex and requires more power; however, in systems where accurate time is a requirement, a simple oscillator is not adequate. Higher frequency crystals exhibit similar voltage-frequency drift characteristics even when attached directly to an M146805 CMOS Family device.



NOTES:
1. Route V_{CC} and V_{SS} to power supply separately from other components.
2. Analog channel AN3 is selected by PA0-PA2 connection.
3. V_{RH} and V_{RL} should be furnished by a separate power source (not V_{CC}). The sum of V_{RH} and V_{RL} must not exceed V_{CC}.

Figure 5-9. Stand-Alone A/D Converter Schematic Diagram

5.7 STAND-ALONE ANALOG-TO-DIGITAL CONVERTER (AN-869)

The stand-alone A/D converter shown in Figure 5-9 is configured using an MC6805R2( )1 MCU. The circuit uses three SPDT switches to control the multiplexer selection (a 1-of-8 on-chip select multiplexer which is controlled via the A/D control register from inputs at PA0-PA2). Table 5-2 lists the inputs to the A/D control register which select either the AN0-AN3 inputs or an internal calibration level. The eight bit result of the A/D conversion is output on port B (PB0-PB7). The output on PB3 may be used to indicate that the port B data is valid.

Table 5-2. A/D Control Inputs For Selecting AN0-AN3 and Calibration Channels

Channel	PC2	PC1	PC0
AN0	0	0	0
AN1	0	0	1
AN2	0	1	0
AN3	0	1	1
V_{RH} (Calibration)	1	0	0
V_{RL} (Calibration)	1	0	1
$V_{RH/4}$ (Calibration)	1	1	0
$V_{RH/2}$ (Calibration)	1	1	1

As shown in Figure 5-9, the output of the 10 k 10-turn potentiometer can be used to select a voltage value between V_{RH} and V_{RL}. An input voltage to the selected AN0-AN3 input, which is equal to V_{RH}, converts to FF (full scale) on the LCD. Conversely an input which is equal to V_{RL} converts to 00 on the LCD. Input levels between V_{RH} and V_{RL} provide corresponding indications on the LCD. Figure 5-10 contains the program listing for the A/D conversion routine which is used in the MC6805R2( )1.

5.8 FREQUENCY SYNTHESIZER USING THE MC6805T2L1 (AN-871)

The MC6805T2L1 Microcomputer Unit (MCU) contains seven distinct program modules, one of which is referred to as the frequency synthesis program (synthesizer [PLL05] mode). The synthesizer mode allows the MC6805T2L1 to function in a phase-locked loop (PLL), which controls the output frequency of a variable frequency oscillator (VFO). The program is written in a way that it can be used to synthesize a complete set of TV channels for either Europe, Japan, or USA. The firmware program is located in masked ROM, and automatically takes into account differences in intermediate frequencies, first and last channel numbers, channel spacing, etc., as they exist between the systems used in those countries/lands. The desired mode option configuration is entered by selecting the PLL-( ) country code shown in Table 5-3.

Figure 5-11 provides a schematic diagram of the MC6805T2L1 used in a synthesizer mode configuration (USA selected). All peripheral devices are shown, except for the VCO (tuner) and prescaler (if used).

```
                    *       SAD --- STAND ALONE ANALOG TO DIGITAL CONVERTER
                    *
                    *       IN THIS MODE, THE 68Ø5R2 OPERATES AS AN 8 CHANNEL
                    *       MULTIPLEXED ANALOG TO DIGITAL CONVERTER. INPUT TO THE
                    *       CONVERTER IS VIA THREE CHANNEL SELECT LINES ON PORT A.
                    *       THE DESIRED CHANNEL IS TRANSFERRED TO THE A TO D CONTROL
                    *       REGISTER AND THE PROGRAM WAITS FOR A CONVERSION TO
                    *       COMPLETE. AFTER COMPLETION, THE RESULT REGISTER IS
                    *       TRANSFERRED TO PORT B. AN EXTERNAL END OF CONVERSION BIT
                    *       IS ALSO PROVIDED TO SYNCHRONIZE THE RESULTS ON PORT B.
                    *       THIS BIT (PORT A BIT 3) IS LOW WHEN THE OUTPUT OF PORT B
                    *       IS CHANGING AND HIGH OTHERWISE.
                    *       I/O REGISTER ADDRESSES
                    *
        ØØØØ      A PORTA  EQU    $ØØØ      I/O PORT Ø
        ØØØ1      A PORTB  EQU    $ØØ1      I/O PORT 1
        ØØØ2      A PORTC  EQU    $ØØ2      I/O PORT 2
        ØØØ3      A PORTD  EQU    $ØØ3      I/O PORT 3 (ALSO A/D INPUT STUFF)
        ØØØ4      A DDR    EQU    4         DATA DIRECTION REGISTER OFFSET
        ØØØ8      A TIMER  EQU    $ØØ8      8-BIT TIMER REGISTER
        ØØØ9      A TCR    EQU    $ØØ9      TIMER CONTROL REGISTER
        ØØØA      A MISC   EQU    $ØØA      MISCELLANEOUS REGISTER (INT2 FLAGS)
        ØØØE      A ADCSR  EQU    $ØØE      A TO D CONTROL/STATUS REGISTER
        ØØØF      A RESULT EQU    $ØØF      A TO D RESULT REGISTER
        Ø4Ø       A RAM    EQU    $Ø4Ø      START OF ON-CHIP RAM AREA
        Ø8Ø       A ZROM   EQU    $Ø8Ø      START OF PAGE ZERO ROM
        Ø7CØ      A ROM    EQU    $7CØ      START OF MAIN ROM AREA
        1ØØØ      A MEMSIZ EQU    $1ØØØ     MEMORY ADDRESS SPACE SIZE
                    *
                    *       BITS IN VARIOUS CONTROL REGISTERS
                    *
        ØØØ7      A EOC    EQU    7         END OF CONVERSION BIT IN ADCSR
        ØØØ7      A INT2F  EQU    7         INT2 FLAG BIT IN MISC
        ØØØ6      A INT2E  EQU    6         INT2 ENABLE BIT IN MISC
                    *
ØDC5 17 ØØ        A SAD    BCLR   3,PORTA   INITIALIZE OUTPUT INVALID
ØDC7 A6 Ø8        A        LDA    #%1ØØØ    MAKE BIT 3 OUTPUT, 2-Ø INPUTS
ØDC9 B7 Ø4        A        STA    PORTA+DDR
ØDCB A6 FF        A        LDA    #$FF      AND MAKE B ALL OUTPUTS
ØDCD B7 Ø5        A        STA    PORTB+DDR
ØDCF B6 ØØ        A        LDA    PORTA     PICKUP CHANNEL #
ØDD1 A4 Ø7        A        AND    #%111     CLEAR GARBAGE
ØDD3 B7 ØE        A        STA    ADCSR     START CONVERSION
ØDD5 ØF ØE FD ØDD5         BRCLR  EOC,ADCSR,* WAIT FOR IT TO FINISH
        ØDD8      A SADLP  EQU    *
ØDD8 B6 ØØ        A        LDA    PORTA     GET NEXT CHANNEL
ØDDA A4 Ø7        A        AND    #%111     MASK GARBAGE
ØDDC BE ØF        A        LDX    RESULT    PICKUP LATEST RESULT
ØDDE B7 ØE        A        STA    ADCSR     START NEXT CONVERSION
ØDEØ 17 ØØ        A        BCLR   3,PORTA   DATA ABOUT TO CHANGE
ØDE2 BF Ø1        A        STX    PORTB     DATA CHANGING
ØDE4 16 ØØ        A        BSET   3,PORTA   DATA NOW VALID
ØDE6 2Ø FØ     ØDD8        BRA    SADLP
```

Figure 5-10. A/D Conversion Routine Software

Table 5-3. PLL Country/Land Selection Configuration

MC6805T2L1 Pins					Mode Option
PC0	PC1	PC2	PB0	PB1	
X	1	1	1	0	PLL-Europe
X	1	1	0	1	PLL-USA
X	1	1	1	1	PLL-Japan

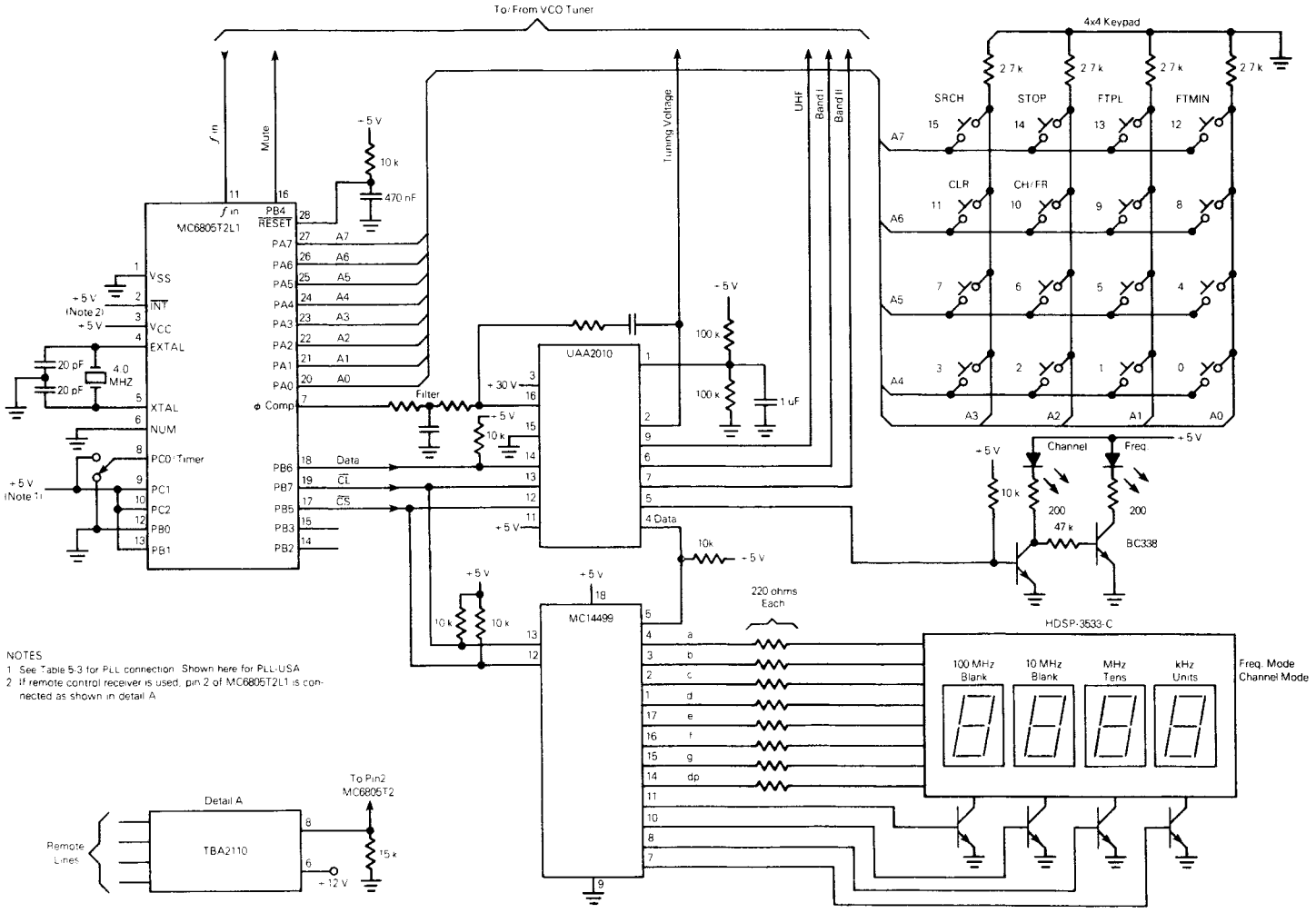


Figure 5-11. Synthesizer Mode Configuration Schematic Diagram

By using a keypad and display, any channel from 00-99 may be selected and displayed. The program calculates the frequency code (divide ratio) and stores it in the PLL registers (Hi and Lo). The contents of the PLL register are then loaded into a variable divider where it controls the f_{in} division. The variable divider output frequency is then compared to a reference divider frequency and the result of this comparison (ϕ COMP) is used to control the synthesizer frequency. Actually, the VCO frequency is divided in a prescaler in order to develop the f_{in} input at pin 11. A complete list of all synthesized channels is shown in Tables 5-4, 5-5, and 5-6.

In the synthesizer mode of operation configuration shown in Figure 5-11, the MC6805T2L1 program provides the following functions in conjunction with the 4 × 4 keypad.

1. channel select (keys 0-9)
2. channel or frequency display (CH/FR, key 10)
3. clear after one digit selected (CLEAR, key 11)
4. decrement frequency in 62.5 kHz steps (FTMIN, key 12)
5. increment frequency in 62.5 kHz steps (FTPL, key 13)
6. stop search (STOP, key 14)
7. channel search incrementing by one repeatedly (SRCH, key 15)

NOTE

In the description which follows, a European system is assumed. For USA and Japan differences refer to Tables 5-5 and 5-6.

At reset, the system of Figure 5-11 synthesizes and displays channel number 00 (lowest channel) and the channel indicator lights. Depressing the CH/FR key (10) causes the corresponding channel frequency (331.1) in MHz to appear on the 4-digit display, and the frequency indicator lights. The value shown can now be incremented in 62.5 kHz steps by depressing the FTMIN key (12). Only hundreds of kHz are displayed (331.125 displays as 331.1); therefore, the display might not change with each 62.5 kHz step.

A channel search operation can be activated by depressing the SRCH key (15). Depressing the SRCH key starts the search at the current channel and increments the channel every 350 milliseconds. When channel 99 (USA 83, Japan 62) is reached, the search cycle is repeated from channel 00 (USA 02, Japan 01). While the channel number is advanced, the corresponding frequency is also synthesized successively. Since the CH/FR key remains active, either the channel or resultant frequency is visible. To stop the search, it is only necessary to depress the STOP key (14).

For the USA and Japan PLL configurations, all channel numbers are not used; therefore, entering a non-existant channel (for example, 98 or 00) is interpreted by the program as a reset. After reset, the USA configuration display is 02 and the Japan configuration display is 01. A channel search operation is only made on existing channels.

The CLR key (11) allows the first selected digit (tens) of the channel number to be cleared in case of error during entry.

Table 5-4. Channel Characteristics for Europe

Channel No.	Band I	Band III	Band UHF	Divide Ratio Hex	Divide Ratio Decimal	Osc. Frequency MHz
00	0	1	0	14D2	5298	331.125
01	1	0	0	0552	1362	85.125
02	1	0	0	572	1394	87.125
03	1	0	0	5E2	1506	94.125
04	1	0	0	652	1618	101.125
05	0	1	0	D62	3426	214.125
06	0	1	0	DD2	3538	221.125
07	0	1	0	E42	3650	228.125
08	0	1	0	EB2	3762	235.125
09	0	1	0	F22	3874	242.125
10	0	1	0	F92	3986	249.125
11	0	1	0	1002	4098	256.125
12	0	1	0	1072	4210	263.125
13	1	0	0	5CA	1482	92.625
14	1	0	0	652	1618	101.125
15	1	0	0	792	1938	121.125
16	0	1	0	D62	3426	214.125
17	0	1	0	DEA	3554	222.125
18	0	1	0	E72	3698	231.125
19	0	1	0	F02	3842	240.125
20	0	1	0	F92	3986	249.125
21	0	0	1	1FE2	8162	510.125
22	0	0	1	2062	8290	518.125
23	0	0	1	20E2	8418	526.125
24	0	0	1	2162	8546	534.125
25	0	0	1	21E2	8674	542.125
26	0	0	1	2262	8802	550.125
27	0	0	1	22E2	8930	558.125
28	0	0	1	2362	9058	566.125
29	0	0	1	23E2	9186	574.125
30	0	0	1	2462	9314	582.125
31	0	0	1	24E2	9442	590.125
32	0	0	1	2562	9570	598.125
33	0	0	1	25E2	9698	606.125
34	0	0	1	2662	9826	614.125
35	0	0	1	26E2	9954	622.125
36	0	0	1	2762	10082	630.125
37	0	0	1	27E2	10210	638.125
38	0	0	1	2862	10338	646.125
39	0	0	1	28E2	10466	654.125
40	0	0	1	2962	10594	662.125
41	0	0	1	29E2	10722	670.125
42	0	0	1	2A62	10850	678.125
43	0	0	1	2AE2	10978	686.125
44	0	0	1	2BC2	11106	694.125
45	0	0	1	2BE2	11234	702.125
46	0	0	1	2C62	11362	710.125
47	0	0	1	2CE2	11490	718.125
48	0	0	1	2D62	11618	726.125
49	0	0	1	2DE2	11746	734.125
50	0	0	1	2E62	11874	742.125

Table 5-4. Channel Characteristics for Europe (Continued)

Channel No.	Band I	Band III	Band UHF	Divide Ratio Hex	Divide Ratio Decimal	Osc. Frequency MHz
51	0	0	1	2EE2	12002	750.125
52	0	0	1	2F62	12130	758.125
53	0	0	1	2FE2	12258	766.125
54	0	0	1	3062	13386	774.125
55	0	0	1	30E2	12514	782.125
56	0	0	1	3162	12642	790.125
57	0	0	1	31E2	12770	798.125
58	0	0	1	3262	12898	806.125
59	0	0	1	32E2	13026	814.125
60	0	0	1	3362	13154	822.125
61	0	0	1	33E2	13282	830.125
62	0	0	1	3462	13410	838.125
63	0	0	1	34E2	13538	846.125
64	0	0	1	3562	13666	854.125
65	0	0	1	35E2	13794	862.125
66	0	0	1	3662	13922	870.125
67	0	0	1	36E2	14050	878.125
68	0	0	1	3762	14178	886.125
69	0	0	1	37E2	14306	894.125
70	1	0	0	602	1538	96.125
71	1	0	0	672	1650	103.125
72	1	0	0	7D2	2002	125.125
73	1	0	0	862	2146	134.125
74	1	0	0	8D2	2258	141.125
75	0	1	0	B12	2834	177.125
76	0	1	0	F82	3970	248.125
77	0	1	0	FF2	4082	255.125
78	1	0	0	6C2	1730	108.125
79	1	0	0	732	1842	115.125
80	1	0	0	7A2	1954	122.125
81	1	0	0	902	2306	144.125
82	0	1	0	972	2418	151.125
83	0	1	0	9E2	2530	158.125
84	0	1	0	A52	2642	165.125
85	0	1	0	AC2	2754	172.125
86	0	1	0	B32	2866	179.125
87	0	1	0	BA2	2978	186.125
88	0	1	0	C12	3090	193.125
89	0	1	0	C82	3202	200.125
90	0	1	0	CF2	3314	207.125
91	0	1	0	10E2	4322	270.125
92	0	1	0	1152	4434	277.125
93	0	1	0	11C2	4546	284.125
94	0	1	0	1232	4658	291.125
95	0	1	0	12A2	4770	298.125
96	0	1	0	1312	4882	305.125
97	0	1	0	1382	4994	312.125
98	0	1	0	13F2	5106	319.125
99	0	1	0	1462	5218	326.125

Table 5-5. Channel Characteristics for USA

Channel No.	Band I	Band III	Band UHF	Divide Ratio Hex	Divide Ratio Decimal	Osc. Frequency MHz
02	1	0	0	650	1616	101.000
03	1	0	0	6B0	1712	107.000
04	1	0	0	710	1808	113.000
05	1	0	0	7B0	1968	123.000
06	1	0	0	810	2064	129.000
07	0	1	0	DD0	3536	221.000
08	0	1	0	E30	3632	227.000
09	0	1	0	E90	3728	233.000
10	0	1	0	EF0	3824	239.000
11	0	1	0	F50	3920	245.000
12	0	1	0	FB0	4016	251.000
13	0	1	0	1010	4112	257.000
14	0	0	1	2050	8272	517.000
15	0	0	1	20B0	8368	523.000
16	0	0	1	2110	8464	529.000
17	0	0	1	2170	8560	535.000
18	0	0	1	21D0	8656	541.000
19	0	0	1	2230	8752	547.000
20	0	0	1	2290	8848	553.000
21	0	0	1	22F0	8944	559.000
22	0	0	1	2350	9040	565.000
23	0	0	1	23B0	9136	571.000
24	0	0	1	2410	9232	577.000
25	0	0	1	2470	9328	583.000
26	0	0	1	24D0	9424	589.000
27	0	0	1	2530	9520	595.000
28	0	0	1	2590	9616	601.000
29	0	0	1	25F0	9712	607.000
30	0	0	1	2650	9808	613.000
31	0	0	1	26B0	9904	619.000
32	0	0	1	2710	10000	625.000
33	0	0	1	2770	10096	631.000
34	0	0	1	27D0	10192	637.000
35	0	0	1	2830	10288	643.000
36	0	0	1	2890	10384	649.000
37	0	0	1	28F0	10480	655.000
38	0	0	1	2950	10576	661.000
39	0	0	1	29B0	10672	667.000
40	0	0	1	2A10	10768	673.000
41	0	0	1	2A70	10864	679.000
42	0	0	1	2AD0	10960	685.000
43	0	0	1	2B30	11056	691.000
44	0	0	1	2B90	11152	697.000
45	0	0	1	2BF0	11248	703.000
46	0	0	1	2C50	11344	709.000
47	0	0	1	2CB0	11440	715.000
48	0	0	1	2D10	11536	721.000
49	0	0	1	2D70	11632	727.000
50	0	0	1	2DD0	11728	733.000
51	0	0	1	2E30	11824	739.000
52	0	0	1	2E90	11920	745.000
53	0	0	1	2EF0	12016	751.000
54	0	0	1	2F50	12112	757.000
55	0	0	1	2FB0	12208	763.000
56	0	0	1	3010	12304	769.000
57	0	0	1	3070	12400	775.000
58	0	0	1	30D0	12496	781.000
59	0	0	1	3130	12592	787.000
60	0	0	1	3190	12688	793.000

Table 5-5. Channel Characteristics for USA (Continued)

Channel No.	Band I	Band III	Band UHF	Divide Ratio Hex.	Divide Ratio Decimal	Osc. Frequency MHz
61	0	0	1	31F0	12784	799.000
62	0	0	1	3250	12880	805.000
63	0	0	1	32B0	12976	811.000
64	0	0	1	3310	13072	817.000
65	0	0	1	3370	13168	823.000
66	0	0	1	33D0	13264	829.000
67	0	0	1	3430	13360	835.000
68	0	0	1	3490	13456	841.000
69	0	0	1	34F0	13552	847.000
70	0	0	1	3550	13648	853.000
71	0	0	1	35B0	13744	859.000
72	0	0	1	3610	13840	865.000
73	0	0	1	3670	13936	871.000
74	0	0	1	36D0	14032	877.000
75	0	0	1	3730	14128	883.000
76	0	0	1	3790	14224	889.000
77	0	0	1	37F0	14320	895.000
78	0	0	1	3850	14416	901.000
79	0	0	1	38B0	14512	907.000
80	0	0	1	3910	14608	913.000
81	0	0	1	3970	14704	919.000
82	0	0	1	39D0	14800	925.000
83	0	0	1	3A30	14896	931.000

Table 5-6. Channel Characteristics for Japan

Channel No.	Band I	Band III	Band UHF	Divide Ratio Hex.	Divide Ratio Decimal	Osc. Frequency MHz
01	1	0	0	960	2400	150.000
02	1	0	0	9C0	2496	156.000
03	1	0	0	A20	2592	162.000
04	0	1	0	E60	3680	230.000
05	0	1	0	EC0	3776	236.000
06	0	1	0	F20	3872	242.000
07	0	1	0	F80	3968	248.000
08	0	1	0	FC0	4032	252.000
09	0	1	0	1020	4128	258.000
10	0	1	0	1080	4224	264.000
11	0	1	0	10E0	4320	270.000
12	0	1	0	1140	4416	276.000
13	0	0	1	2120	8480	530.000
14	0	0	1	2180	8576	536.000
15	0	0	1	21E0	8672	542.000
16	0	0	1	2240	8768	548.000
17	0	0	1	22A0	8864	554.000
18	0	0	1	2300	8960	560.000
19	0	0	1	2360	9056	566.000
20	0	0	1	23C0	9152	572.000
21	0	0	1	2420	9248	578.000
22	0	0	1	2480	9344	584.000
23	0	0	1	24E0	9440	590.000
24	0	0	1	2540	9536	598.000
25	0	0	1	25A0	9632	602.000
26	0	0	1	2600	9728	608.000
27	0	0	1	2660	9824	614.000
28	0	0	1	26C0	9920	620.000
29	0	0	1	2720	10016	626.000
30	0	0	1	2780	10112	632.000
31	0	0	1	27E0	10208	638.000
32	0	0	1	2840	10304	644.000
33	0	0	1	28A0	10400	650.000
34	0	0	1	2900	10496	656.000
35	0	0	1	2960	10592	662.000
36	0	0	1	29C0	10688	668.000
37	0	0	1	2A20	10784	674.000
38	0	0	1	2A80	10880	680.000
39	0	0	1	2AE0	10976	686.000
40	0	0	1	2B40	11072	692.000
41	0	0	1	2BA0	11168	698.000
42	0	0	1	2C00	11264	704.000
43	0	0	1	2C60	11360	710.000
44	0	0	1	2CC0	11456	716.000
45	0	0	1	2D20	11552	722.000
46	0	0	1	2D80	11648	728.000
47	0	0	1	2DE0	11744	734.000
48	0	0	1	2E40	11840	740.000
49	0	0	1	2EA0	11936	746.000
50	0	0	1	2F00	12032	752.000

Table 5-6. Channel Characteristics for Japan (Continued)

Channel No.	Band I	Band III	Band UHF	Divide Ratio Hex.	Divide Ratio Decimal	Osc. Frequency MHz
51	0	0	1	2F60	12128	758.000
52	0	0	1	2FC0	12224	764.000
53	0	0	1	3020	12320	770.000
54	0	0	1	3080	12416	776.000
55	0	0	1	30E0	12512	782.000
56	0	0	1	3140	12608	788.000
57	0	0	1	31A0	12704	794.000
58	0	0	1	3200	12800	800.000
59	0	0	1	3260	12896	806.000
60	0	0	1	32C0	12992	812.000
61	0	0	1	3320	13088	818.000
62	0	0	1	3380	13184	824.000

A flowchart showing the main synthesizer (PLL05) mode routine is shown in Figure 5-12 and selection of the various programs in the MC6805T2L1 is shown in Figure 5-13. Note that in Figure 5-13 the reset routine will exit to one of the eight modes depending upon the configuration of PB0, PB1, PC0, PC1, and PC2 per Table 1.

5.9 KEYLESS ENTRY SYSTEM USING THE MC146805F2( )1 (AN-863)

5.9.1 Introduction

The keyless entry system (also referred to as a digital lock) is a dedicated MC146805F2( )1 Microcomputer Unit (MCU), executing a program, that can control a larger configuration to form a security system. Figure 5-14 contains a schematic diagram of the digital lock complete with keypad and liquid crystal display.

NOTE

The keyless entry system using the MC146805F2( )1 8-Bit Microcomputer Unit is not intended to be used by itself in a secure entry system. It is intended to be used only as an aid in better understanding the MC146805F2 MCU and how it can fit into a secure entry system.

The digital lock accepts inputs from the 3 × 4 keypad, and, if the inputs are in the corrently coded sequence, generates an output which indicates the lock is open. The digital lock MCU has a feature which protects against "trial-and-error" attempts to gain entry. If two incorrect code combinations are entered, an alarm output is generated (PB2 goes high). The alarm condition remains active until the combination is entered or power is disconnected.

The user interfaces with the digital lock MCU through a 3 × 4 keypad and a "wake-up" pushbutton. This allows multiple users to gain access to a secure area without the necessity of carrying a key. The LCD displays a dash for each keypad entry. This ensures that the user knows how many of the required keypad entries have been made. Once the correct combination has been entered via the keypad, the LCD spells out the word OPEN. From this time, the user has eight seconds to open the door or other locked device.

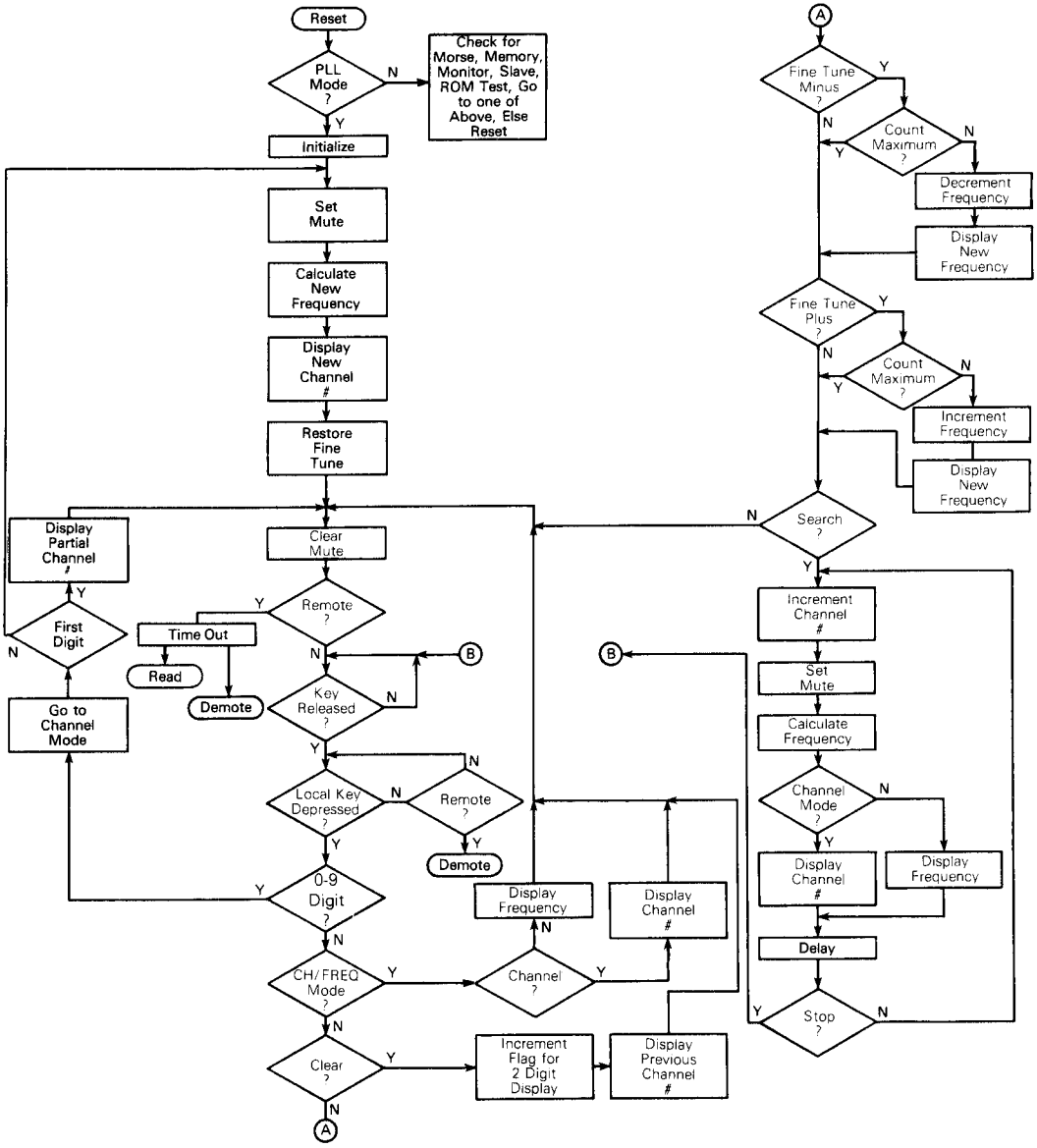


Figure 5-12. Main Synthesizer (PLL05) Routine Flowchart

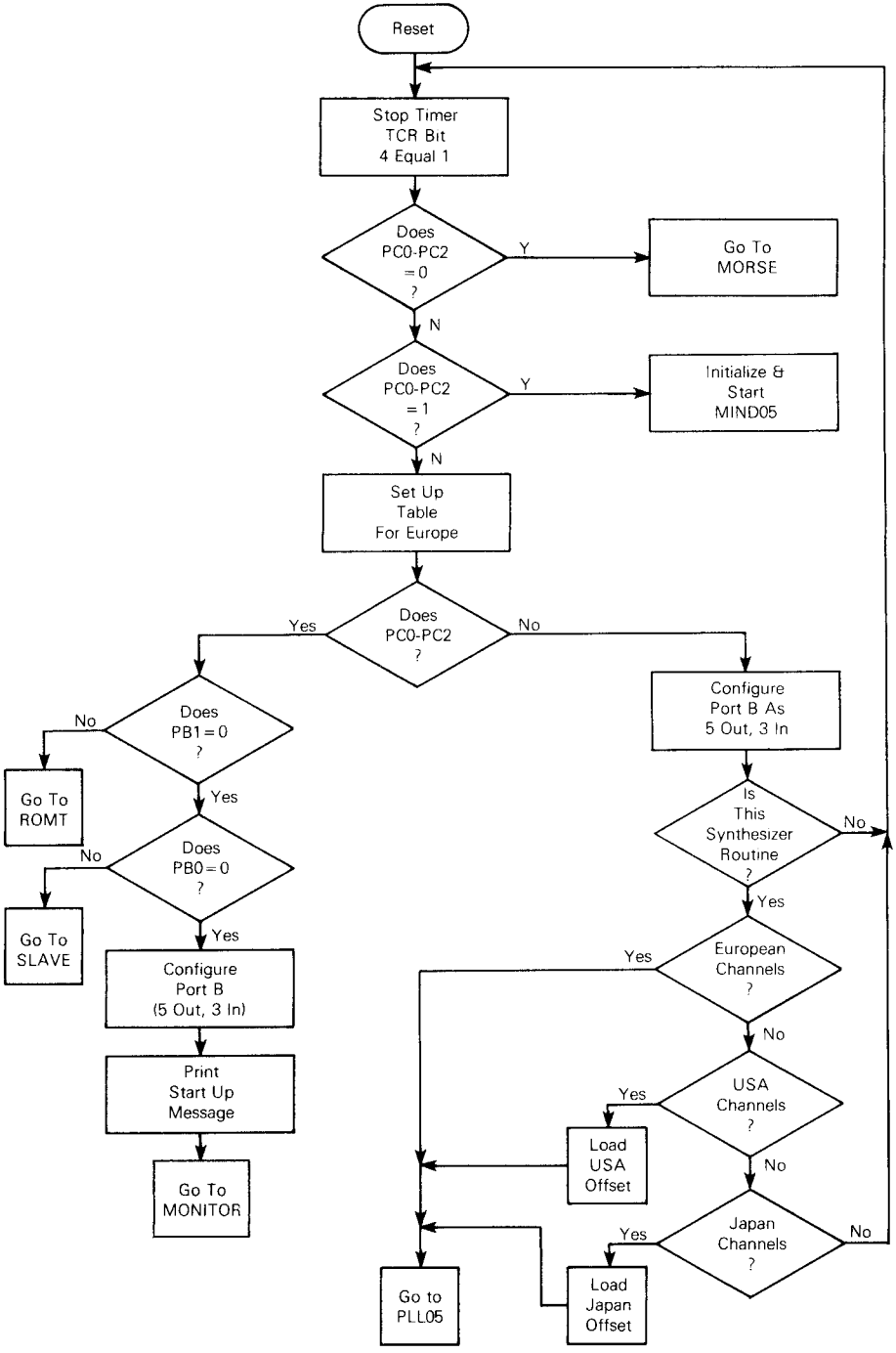


Figure 5-13. Reset Routine Flowchart

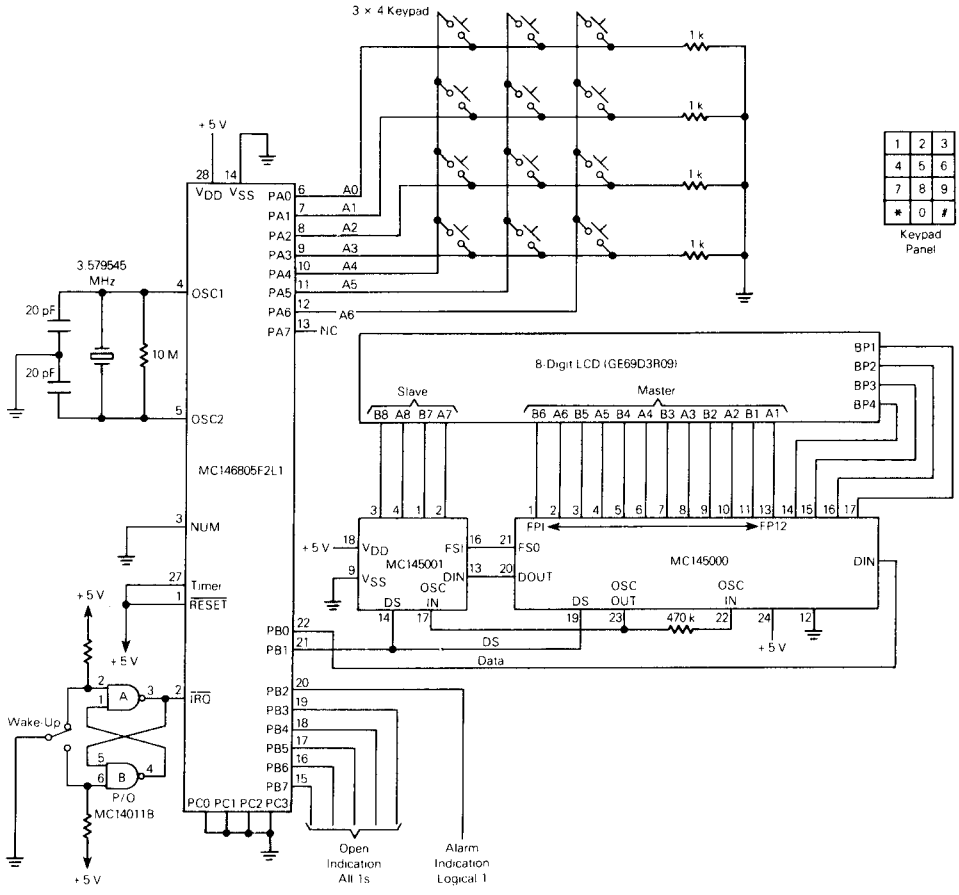


Figure 5-14. Digital Lock System Schematic Diagram

5.9.2 Initialization

When power is initially applied or if power is lost and then reapplied, the 8-digit combination code is lost in RAM. It now becomes necessary to enter a new 8-digit combination. This can be done by performing the procedure outlined in the Changing The Coded Sequence paragraph.

5.9.3 Operation

Two operating modes are described below. One is the normal user procedure to open the digital lock and the other describes a method to change the coded sequence combination.

5.9.3.1 OPENING THE DIGITAL LOCK. To open the digital lock proceed as follows:

1. Press the "wake-up" pushbutton and check that the LCD is clear.
2. Use the keypad to enter the 8-digit combination code. Note that each time a keypad switch is depressed a dash will appear, on the LCD, to indicate that a digit is entered. The total number of digits entered is equal to the total number of dashes.
3. Once the correct 8-digit combination code is entered, the LCD displays the word "OPEN". The open signal is then active for approximately eight seconds. If the user fails to mechanically open the door (or other entry device) during the 8-second time period, the above procedure must be repeated to again gain entry.

NOTE

If an incorrect code is entered for the second time, the alarm signal becomes active. The alarm will stay active until the correct code is entered, as described above, or power is removed.

5.9.3.2 CHANGING THE CODED SEQUENCE. To change the digital lock coded sequence (combination), proceed as follows:

1. Press the "wake-up" pushbutton and check that the LCD is clear.
2. Use the keypad to enter the 8-digit "change combination code" number 14680502. Note that each time a keypad switch is depressed, a dash will appear, on the LCD, to indicate that a digit is entered. Once all eight digits are entered, the LCD goes blank.
3. Use the keypad to enter the new 8-digit combination code. As before, a dash appears each time a keypad switch is depressed.
4. Once the eight new digits are entered, the word "VERIFY" appears on the LCD. This is a prompt for the user to enter the same 8-digit combination code as in 3 above. If the second 8-digit entry is not exactly the same as the first, the word "ERROR" is displayed on the LCD. In this case, the user must repeat the procedure from 3 above.

NOTE

Changing the combination coded sequence does not open the lock. Once the new code has been verified, the LCD goes blank. The lock can then be opened as described above in the Opening The Digital Lock paragraph.

5.10 BICYCLE COMPUTER USING THE MC146805G2( )1 (AN-858)

5.10.1 Introduction

In the configuration shown in Figure 5-15, the MC146805G2( )1 is used as a bicycle computer. Features provided by the bicycle computer include: (1) instantaneous speed, (2) average speed, (3) resettable trip odometer, (4) resettable long distance odometer, (5) cadence (pedal crank revolutions per minute), (6) selection of English or metric units, and (7) calibration for wheel size.

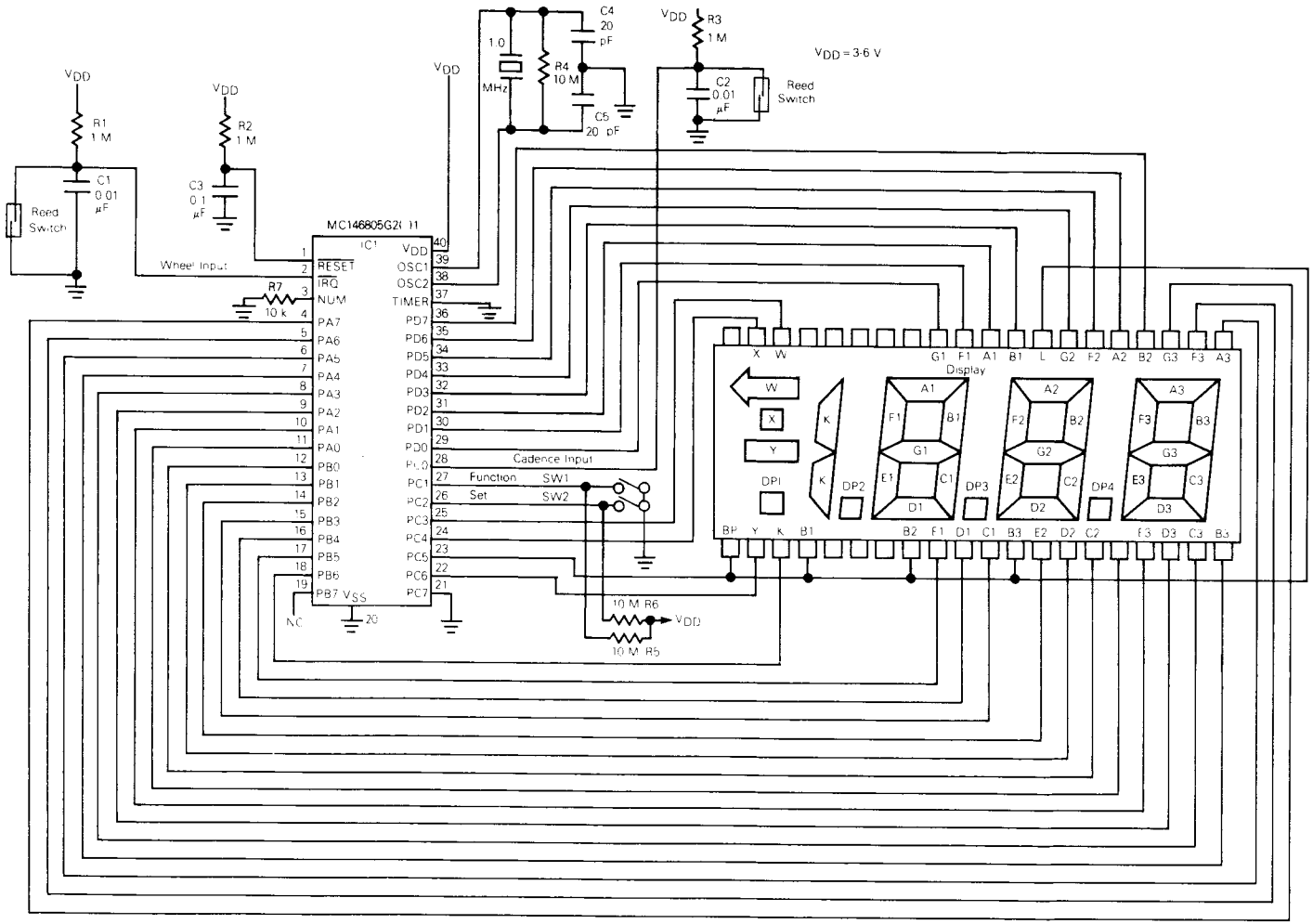
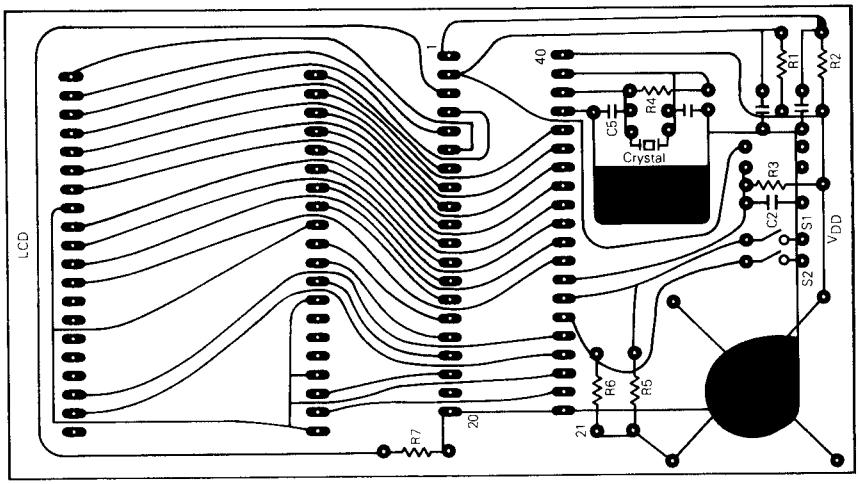
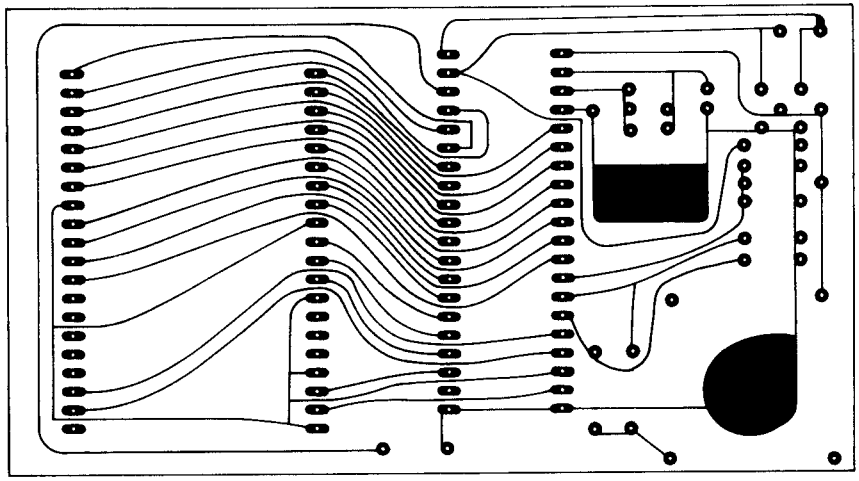


Figure 5-15. Bicycle Computer Schematic Diagram



a. Parts Location



b. Circuit Board Art
(Actual Size)

Figure 5-16. Bicycle Computer Circuit Board

5.10.2 Hardware Configuration

A schematic diagram for the bicycle computer is shown in Figure 5-15 and Figure 5-16 shows a parts layout diagram plus circuit board art. As shown on the schematic diagram, the MC146805G2( )1 and the liquid crystal display (LCD) are the only major components required for the bicycle computer. All necessary drive signals for the LCD are contained in firmware. Two pushbutton switches (S1 and S2, function and set) are required to furnish two momentary ground inputs, and two sensor inputs (one from the wheel and one

from the pedal crank) are required as an interrupt and to pulse certain counters. Each sensor is a normally-open switch which is activated by a magnet mounted on the wheel and pedal crank.

Figure 5-15 shows the layout of a PCB that may be used when assembling the bicycle computer. The printed circuit board (PCB) is designed to fit in a Wonder-Lite case. The Wonder-Lite is designed to mount on a bicycle and provide nighttime illumination. Dimensions for this bord are 4.5" × 2.5" and could require some tailoring before fitting into the mounting case. However, an equivalent size wire-wrap type board using the wire-wrap connections and mounting sockets could be used with an equivalently sized case.

5.10.3 Bicycle Computer Function

When power is initially applied to the circuit or when the MC146805G2( )1 is reset, the bicycle computer program is selected and the bicycle computer displays the current instantaneous speed on the display (Function 1). Each time the "function" button (S1) is pushed, the bicycle computer will step to the next function. The functions are:

1. instantaneous speed
2. average speed
3. resettable trip odometer
4. resettable long distance odometer
5. cadence
6. English or metric units selection
7. wheel size calibration

Each time the function switch is pushed, the program steps to the next function; however, after function 7 it returns to function 1. Some functions may require resetting. For example, at the beginning of each bicycle trip it may be desirable to reset the trip odometer to zero for miles or kilometers. The "set" pushbutton (S2) is provided to perform this task. If the set button is pushed while in function 3, the trip odometer is reset to zero. However, it is not desirable to have the "set" button enabled at all times. For example, if the "set" button were accidentally pushed during a trip, the trip odometer would be reset to zero. Therefore, the "set" button is only enabled for the first five seconds after a new function is selected. Pushing the "set" button after five seconds will not affect the function. During the five seconds that the "set" button is enabled, the bicycle computer displays a fixed function identification display. For example, the trip odometer will display " odo " during this function 3 time. After five seconds the selected function value is displayed and remains displayed until the "function" button is again pushed, stepping to the next function. Complete descriptions for these functions are provided in Motorola Application Note AN-858.

Wonder-Lite is a trademark of Wonder Corp. of America

5.11 AVAILABLE APPLICATION NOTES

Several application notes for the M6805 HMOS/M146805 CMOS Family are (or will be) available as of the printing of this users manual. A list of these application notes is provided in Table 5-7.

Table 5-7. List of Available Application Notes

AN#	Title
823	CBUG05 Monitor Program for MC146805E2 Microprocessor Unit
852	Monitor for the MC146805G2L1 Microcomputer
853	M146805 CMOS Family Emulators
855	Versatile Thermostat using CMOS MC146805E2 MPU
857	MC68705P3/R3/U3 EPROM Microcomputer Programming Module
858	Bicycle Computer using the MC146805G2L1 Microcomputer
863	Keyless Entry System using an MC146805F2( )1 8-Bit Microcomputer Unit
869	Application Summary for the MC6805R2( )1 Single-Chip Microcomputer With A/D Converter
871	AN Applications Summary for the MC6805T2L1 Single-Chip Microcomputer With Phase-Lock-Loop
883	A Radio Set Phase-Lock-Loop (PLL) using an MC6805T2( )2 Single-Chip Microcomputer

In addition, the TWX, TELEX, DITEL, and telephone numbers plus the mailing address of the Literature Distribution Center (where the application notes are available) are listed below.

The Literature Distribution Center, located in Phoenix, Arizona, offers a method by which a sales office or customer can order the application notes listed in Table 5-7. A listing of various methods to communicate with the Literature Distribution Center is shown below.

Phone:	Literature Distribution Center	602-994-6561
TWX:	(MOT SEMI PHX)	901-951-1334 (LDC)
DITEL:	(Motorola Facilities)	234-6561
Mail Drop:	Broadway Bldg. (BB100)	
Address:	Motorola Semiconductors Products, Inc. Literature Distribution Center P. O. Box 20924 Phoenix, Az 85036	