

Providing users with concise, up-to-date information on Motorola's M6805 HMOS/M146805 CMOS family, this manual shows how various family members can be used for design of control and instrumentation as well as other diverse applications. Basic design differences between 15 of the family devices are listed in this easy-to-use manual:

MC6805P2	MC68705P3
MC6805P4	MC68705R3
MC6805P6	MC68705U3
MC6805R2	MC1468705G2
MC6805R3	MC146805E2
MC6805T2	MC146805F2
MC6805U2	MC146805G2
MC6805U3	

This versatile family of microcomputers and a microprocessor offers many versions for diverse applications with the latest features including EPROM for easy prototype system design, low power versions, low cost, and powerful architecture.

Detailed information on software (descriptions and applications) and hardware (features and applications) is provided in the main chapters. Also included are chapters on the EPROM programmer and on the self-test, the on-chip firmware test capability. Appendices are included to provide designers with the latest M6805 HMOS/M146805 CMOS family programming information.



MOTOROLA

**M6805 HMOS
M146805 CMOS
FAMILY
MICROCOMPUTER/MICROPROCESSOR
USER'S MANUAL**

SECOND EDITION

CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION TO THE M6805 HMOS/M146805 CMOS FAMILY

The continuing technological evolution in microprocessors and microcomputers has resulted in larger, more complex, and more powerful devices which contain characteristics of both mini and mainframe computers. The technological evolution of the MC6800 to the M6809 Family and the 16-bit MC68000 is a clear example of devices which evolved upward from the mini and mainframe computer architecture. The experience gained during this upward evaluation has greatly enhanced the expertise needed to design more powerful low- and mid-range devices. By using the architectural characteristics of the mini and mainframe computers, the microprocessor/microcomputer hardware and software becomes regular and versatile, yet simple.

The demanding requirements of the mid-range control-oriented microprocessor market (low cost) can be met with the M6805 HMOS/M146805 CMOS Families of microcomputer (MCU) and microprocessor (MPU). The M6805 HMOS/M146805 CMOS Families are the first to provide the software and hardware capabilities of more advanced computers to the controller market. Previously, designers and manufacturers were required to choose between "no processor at all" or a processor that functioned more like a calculator than a computer.

Control-oriented microprocessors have evolved from two different bases: calculator based and computer based. The calculator-based design was at first considered as a natural building block for controllers since, most often, a controller was required to be a complete self-contained unit. However, calculator based control-oriented microprocessors use a split memory architecture containing separate data paths between the CPU and peripherals (memory or I/O or registers). In addition, calculator-based I/O, display, and keypad were separated from program and data storage memory. Because of this, separate address maps were required which forced the inclusion of many special purpose instructions and resulted in an irregular architecture. As a result, these calculator based devices required that hardware and software designers remember and consider many special cases in order to perform any task. Thus, the software and hardware became very random, irregular, and difficult to update.

The computer-based design led to another group of processors, like the MC6800, which contained many features of large computers. These devices contain a single data bus which allows access to a single address map, eliminating the need for split memory architecture. In this one-address map design, all I/O, program, and data may be accessed with the same instruction; therefore, there are fewer instructions to remember. The

actual number of unique instructions is increased by a variety of addressing modes which define how an instruction accesses any data required for the operation. For example, depending upon which addressing mode is used, the accumulator may be loaded (LDA instruction) with data in six different ways. This effectively provides the programmer with more tools to work with but fewer things to remember. Thus, because of regularity of the architecture, the hardware is regular and can be implemented more efficiently.

All members of the M6805 HMOS/M146805 CMOS Family of MCUs and MPUs are designed around a common core which consists of CPU, timer, oscillator, ROM (EPROM, masked, or none), control section (for interrupts and reset), and varying amounts of bidirectional I/O lines. In addition to this common core, additional items can be added such as: additional memory, A/D converter, phase-lock-loop, and additional I/O lines. As of the printing of this manual in late 1982, this versatile common core design has already provided 11 different M6805 HMOS Family devices and four different M146805 CMOS Family devices. These 15 different family members allow the user to choose the device best suited for his particular application. The increased number of devices could preclude paying for a supplied feature that is not needed or paying extra to externally add a needed feature that is not included.

Information describing I/O options and general operation of the M6805 HMOS/M146805 CMOS Family members is included in this chapter. Detailed information concerning device operation is included in the following chapters as well as appendices. Chapters discussing hardware and software applications are also included to illustrate some of the family features and provide a useful tool for the user.

The M6805 HMOS/M146805 CMOS Family architecture and instruction set are very similar to that of Motorola's MC6800. Any programmer who has worked with the MC6800 can attain equivalent proficiency with the M6805 HMOS/M146805 CMOS Family in a relatively short time. In some respects the M6805 HMOS/M146805 CMOS Family is more powerful than the MC6800 (depending upon the application) as a result of architecture optimization. Appendix A summarizes the architectural and instruction set differences between the M6805 HMOS/M146805 CMOS and M6800 Families.

1.2 OPTIMIZED FOR CONTROLLER APPLICATIONS

The M6805 HMOS/M146805 CMOS Family architecture has been optimized for controller applications, rather than general purpose data processing operations. Several features contribute to this optimization.

1.2.1 Instruction Set

The instruction set, used with the M6805 HMOS/M146805 CMOS Family, is specifically designed for byte-efficient program storage. Byte efficiency permits a maximum amount of program function to be implemented within a finite amount of on-chip ROM. Improved ROM efficiency allows the M6805 HMOS/M146805 CMOS Family to be used in applications where other processors might not perform the task in the available ROM space.

More features may be included in applications where ROM space is more than adequate. In some cases the user might wish to include programs for more than one application. In such cases the appropriate program could be selected by the power-up initialization program. The ability to nest subroutines, the addition of true bit test and bit manipulation instructions, the multi-function instructions, and the versatile addressing modes all contribute to byte efficiency.

Superficial comparisons of the number of bytes per instruction for the M6805 HMOS/M146805 CMOS Family, when compared to other machines in this class, can be very misleading. A single M6805 HMOS/M146805 Family instruction occupying 2 or 3 bytes accomplishes as much real programming work as several single byte instructions, or a subroutine, would accomplish in many other processors.

The bit test and bit manipulation instructions permit the program to:

- branch on bit set
- branch on bit clear
- set bit
- clear bit.

These instructions operate on any individual bit in the first 256 address spaces (page zero). As such, the bit manipulations access I/O pins, RAM bits, and ROM bits.

In the M6805 HMOS/M146805 CMOS Family, a page consists of 256 consecutive memory locations. Page zero includes the lowest-numbered 256 memory addresses (\$00 through \$FF), page one the next 256 memory addresses (\$100 through \$1FF), etc. The first 128 bytes of page zero memory locations (\$00 through \$7F) are used primarily for I/O function registers, timer, PLL, RAM, and the stack. The next 128 bytes of page zero (\$80 through \$FF) contain ROM which is available for the user program. An efficient use of pages zero and one would be for storage of tables since these two pages are easily accessed by the indexed addressing mode.

1.2.2 Addressing Modes

One of the chief measures of the effectiveness of a computer architecture is its ability to access data. The M6805 HMOS/M146805 CMOS Family has several major memory addressing modes. They include immediate, direct, and extended, plus three distinct indexed modes. The programmer is thus given the opportunity to optimize the code to the task. The indexed addressing modes permit conversion tables, jump tables, and data tables to be located anywhere in the address space. The use of tables is an important tool in controller type applications.

Efficient addressing methods are coupled with instructions which manipulate memory without disturbing the program registers. Thus, RAM may be used for the same functions that other processors use general purpose registers (increment, decrement, clear, complement, test, etc.). The M6805 HMOS/M146805 CMOS Family members have a very versatile, efficient, and easy-to-use I/O structure. All microcomputer I/O function registers are memory mapped into the first 16 processor addresses. Advantage is thus taken of the efficient addressing modes, the many memory reference instructions, and the use of

RAM (or I/O registers) as general purpose registers. As an example, there are 64 unique instructions which permit the programmer to modify an I/O port. The programmer's problem is not so much how to accomplish a given I/O task, but rather to choose the most effective method from the many methods available. In addition, as with other M6800 Family I/O devices, most M6805 HMOS/M146805 CMOS Family I/O pins are individually programmed as inputs or outputs under software control.

1.3 CHOICE OF TECHNOLOGIES

The first option to be selected by the system designer is the choice between HMOS or CMOS as a processor technology.

1.3.1 HMOS Features

The NMOS (N-Channel Metal Oxide on Silicon) technology has been the mainstay of the M6800 Family. The current state of the continual shrinking of NMOS is called HMOS (High-Density NMOS).

The prime consideration in choosing an M6805 HMOS Family microcomputer is its lower price. Motorola's highly-efficient fabrication process results in a greater yield than other processes. The decreased production costs ultimately result in lower selling prices. The economics of large scale production also contribute to a low selling price.

The high speed of Motorola's HMOS, when compared to PMOS or other NMOS processors, produces a very high performance/price ratio.

A low voltage inhibit (LVI) feature may be selected on HMOS versions. The LVI option forces a reset when the supply voltage drops below a threshold which guarantees correct operation. The CMOS Family members offer wide operating voltage and clock speed ranges, which preclude establishing an LVI threshold.

1.3.2 CMOS Features

An emerging microcomputer technology is CMOS (Complementary MOS, both P- and N-Channel devices). The unique properties of CMOS are increasingly attractive. Some applications are simply not feasible with PMOS, NMOS, or HMOS microcomputers.

Maximum power consumption of CMOS parts ranges from 1/15 to 1/200 of that of an equivalent HMOS part. Low power consumption is important in several classes of applications; thus, CMOS microcomputers are desirable.

(a) Portable Equipment — Hand-held and other portable units operated from self-contained batteries. Battery drain is frequently important in such applications.

(b) Battery Back-Up — CMOS is appropriate in ac powered applications when some or all system functions must continue during a power outage. A small, rechargeable battery keeps a CMOS MCU operable.

(c) **Storage Batteries** — Automotive and telephone equipment operate from larger batteries. Automobile battery drain must be low when the engine is not running. Telephones must operate independently of ac power.

(d) **Heat Dissipation** — Packaging constraints sometimes preclude dissipating electronics-generated heat, or the heat is costly to dissipate. In addition, dissipation of heat directly effects device reliability.

(e) **Power Costs** — The cost of electricity to power the equipment becomes a significant factor in calculating the total life cycle cost of equipment which operates continuously.

The CMOS technology inherently operates over a wide range of supply voltages. Thus, CMOS is used where the supply voltage fluctuates, such as in battery powered equipment; or if line power is available, a lower-cost, loosely regulated supply may be used.

An additional advantage of CMOS is that circuitry is fully static. CMOS microcomputers may be operated at any clock rate less than the guaranteed maximum. This feature may be used to conserve power, since power consumption increases with higher clock frequencies. Static operation may also be advantageous during product developments.

1.4 HARDWARE

Every M6805 HMOS/M146805 CMOS Family microcomputer or microprocessor contains hardware common to all versions, plus a combination of options unique to a particular version. There are also several differences among family members of which potential users should be aware.

1.4.1 Hardware Common To All Devices

Figure 1-1 details the hardware functional blocks common to all M6805 HMOS/M146805 CMOS Family devices.

The central processor unit (CPU) contains the 8-bit arithmetic logic unit, accumulator, program counter, index register, stack pointer, condition code register, instruction decoder, and timing and control logic. These elements resemble the M6800 Family of microprocessors which reflect the M6805 HMOS/M146805 CMOS Family heritage.

The M6805 HMOS/M146805 CMOS Family has on-chip RAM, permitting the microcomputer versions to operate without external memory. The addressing modes and register-like memory operations use this RAM to the fullest extent possible.

Parallel I/O capability, with pins programmable as input or output, is built into every unit.

The external interrupt input, and the capability for multiple nesting of subroutine and interrupts, are features usually found on much more powerful architectures. They permit an M6805 HMOS/M146805 CMOS Family MCU to be used in projects usually considered too complex for microcomputers.

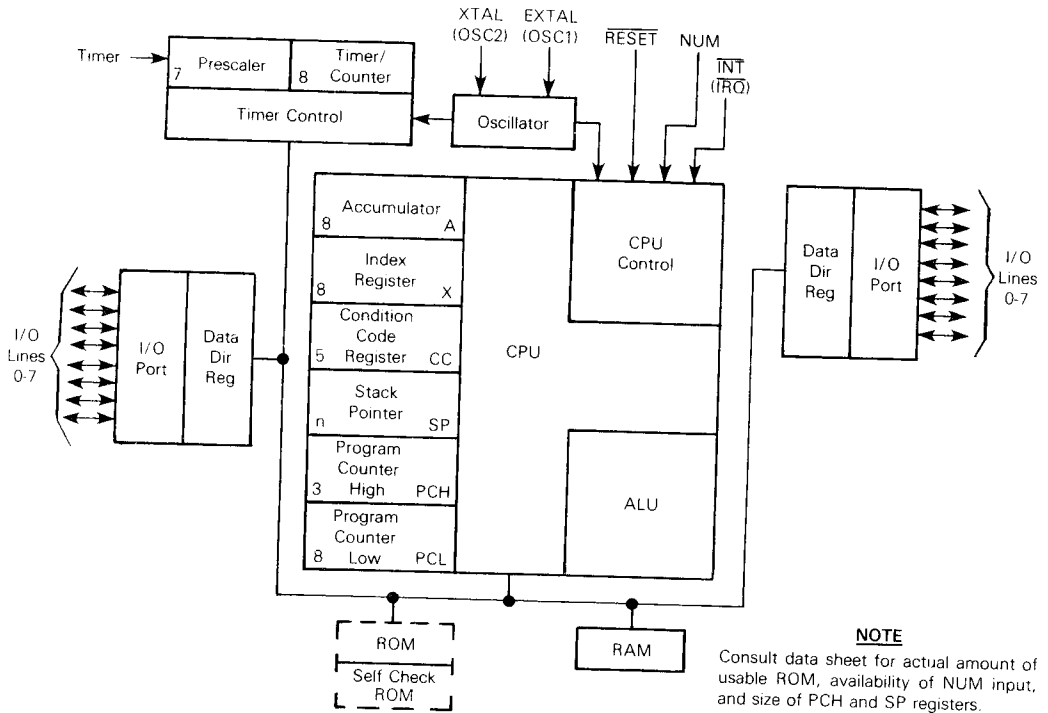


Figure 1-1. M6805 HMOS/M146805 CMOS Family Basic Microcomputer Block Diagram

A feature which greatly simplifies software development and extends the capability of a microcomputer is an on-chip timer/counter. This 8-bit counter and its prescaler can be programmed for innumerable functions. It can generate an interrupt at software selected intervals. It can also be used as an event counter to generate an interrupt after some software selected number of external events. The timer/counter can also be used for timekeeping, measuring and generating pulses, and counting external events. In the case of the M146805 CMOS Family devices, the timer can be set to "wake-up" the processor from the power-saving WAIT mode.

The external interrupt and timer/counter interrupt are vectored to different service routine addresses. This greatly simplifies interrupt programming. It also speeds execution of interrupt routines, by eliminating software interrupt polling, for determining the source of the interrupt.

The first 16 processor addresses are reserved for memory mapped I/O registers. The programmer of the M6805 HMOS/M146805 CMOS Family may take full advantage of the versatile addressing modes and the register-like RAM operations of the Family.

1.4.2 Family Options

In addition to the common hardware described previously, users can make selections from among devices having a combination of hardware options. Potential users should consult their local Motorola sales representative or the most recent data brochures to determine which versions have reached production. Table 1-1 provides a listing of the features included in each family member. Figure 1-2 illustrates the part number nomenclature of three different members of the M6805 HMOS/M146805 CMOS Family.

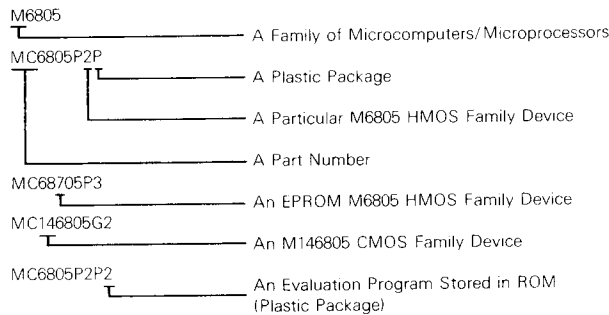


Figure 1-2. M6805 HMOS/M146805 CMOS Family Nomenclature Example

The first option to be selected by the system designer is the choice of technology. In general, the HMOS units would be selected unless the application specifically requires one of the unique characteristics of CMOS.

User ROM sizes range from none, for the microprocessor, to 4K and larger. Future versions will have additional ROM sizes. When self-check ROM is a part of the device, the ROM area used in the self-check operation is not included in the published ROM sizes. The entire ROM space is available to the user for his program.

A portion of the ROM is located in page zero (the direct page) to facilitate more efficient access to look up tables using all available addressing modes. This ROM can, of course, be used for program storage as well as look-up tables.

The initial M6805 HMOS/M146805 CMOS Family devices contain either 64 or 112 bytes of on-chip RAM which is located in page zero. Future devices may accommodate additional or differing amounts of RAM.

Package size options permit as many as four, full 8-bit bidirectional I/O ports. Each pin is defined under software control as an input or output by loading a data direction register.

Table 1-1. M6805 HMOS/M146805 CMOS Family List of Features

M6805 HMOS Family MCUs

Features	MC6805P2	MC6805P4	MC6805P6	MC6805R2	MC6805R3	MC6805T2	MC6805U2	MC6805U3
Technology	HMOS	HMOS	HMOS	HMOS	HMOS	HMOS	HMOS	HMOS
Number of Pins	28	28	28	40	40	28	40	40
On-Chip RAM (Bytes)	64	112*	64	64	112	64	64	112
On-Chip User ROM (Bytes)	1.1K	1.1K	1.8K	2K	3.8K	2.5K	2K	3.8K
External Bus	None	None	None	None	None	None	None	None
Bidirectional I/O Lines	20	20	20	24	24	19	24	24
Unidirectional I/O Lines	None	None	None	6 Inputs	6 Inputs	None	8 Inputs	8 Inputs
Other I/O Features	Timer	Timer	Timer	Timer, A/D	Timer, A/D	Timer, PLL	Timer	Timer
External Interrupt Inputs	1	1	1	2	2	2	2	2
EPROM Version	MC68705P3	MC68705P3	MC68705P3	MC68705R3	MC68705R3	None	MC68705U3	MC68705U3
STOP and WAIT	No	No	No	No	No	No	No	No

*Indicates standby RAM

M6805 HMOS/M146805 CMOS Family EPROM MCUs

Features	MC68705P3	MC68705R3	MC68705U3	MC1468705G2
Technology	HMOS	HMOS	HMOS	CMOS
Number of Pins	28	40	40	40
On-Chip RAM (Bytes)	112	112	112	112
On-Chip User ROM (Bytes)	1.8K EPROM	3.8K EPROM	3.8K EPROM	2K EPROM
External Bus	None	None	None	None
Bidirectional I/O Lines	20	24	24	32
Unidirectional I/O Lines	None	6 Inputs	8 Inputs	None
Other I/O Features	Timer	Timer, A/D	Timer	Timer
External Interrupt Inputs	1	2	2	1
EPROM Version	-	-	-	-
STOP and WAIT	No	No	No	Yes

M146805 CMOS Family MPU/MCUs

Features	MC146805E2	MC146805F2	MC146805G2
Technology	CMOS	CMOS	CMOS
Number of Pins	40	28	40
On-Chip RAM (Bytes)	112	64	112
On-Chip User ROM (Bytes)	None	1K	2K
External Bus	Yes	None	None
Bidirectional I/O Lines	16	16	32
Unidirectional I/O Lines	None	4 Inputs	None
Other I/O Features	Timer	Timer	Timer
External Interrupt Inputs	1	1	1
EPROM Version	None	None	MC1468705G2
STOP and WAIT	Yes	Yes	Yes