54S/74S258
54LS/74LS258A

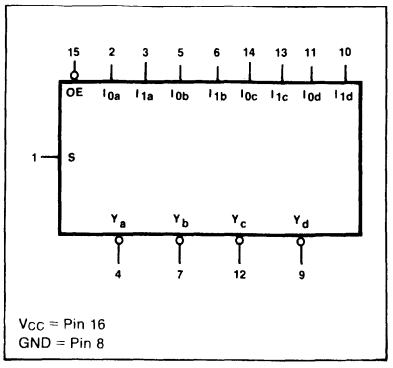
DESCRIPTION

The "258" is a Quad 2-Input Multiplexer with 3-State outputs which can select four bits of data from two sources using a common Data Select input. The four outputs of the device present data in the complementary (inverted) form. The outputs may be set to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) Inputs allowing the outputs to interface directly with 3-State bus-organized systems.

FEATURES

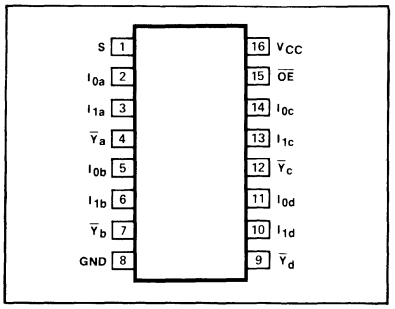
- **Multifunction capability**
- **Inverting data path**
- **3-State outputs**
- **See "257" for non-inverting version**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = -55°C to +125°C
Plastic DIP	N74S258N • N74LS258AN	
Ceramic DIP	N74S258F • N74LS258AF	S54S258F • S54LS258AF
Flatpak		S54S258W • S54LS258AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE [a]

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S	Select input	I_{IH} (μA) I_{IL} (mA)		100 -4.0	40 -0.8
$\overline{OE}$	Output Enable (Active LOW) input	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
I_{0a} - I_{0d}	Data inputs from Source 0	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
I_{1a} - I_{1d}	Data inputs from Source 1	I_{IH} (μA) I_{IL} (mA)		50 -2.0	20 -0.4
$\overline{Y}_a$ - $\overline{Y}_d$	3-State outputs	I_{OH} (mA) I_{OL} (mA)		-2/-6.5 [a] 20	-1/-2.6 [a] 12/24 [a]

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

FUNCTIONAL DESCRIPTION

The "258" has four identical 2-Input Multiplexers with 3-State outputs which select four bits of data from two sources under control of a common Data Select Input (S). The I_0 inputs are selected when the Select Input is LOW and the I_1 inputs are selected when the Select Input is HIGH. Data appears at the outputs in inverted (complementary) form.

The "258" is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

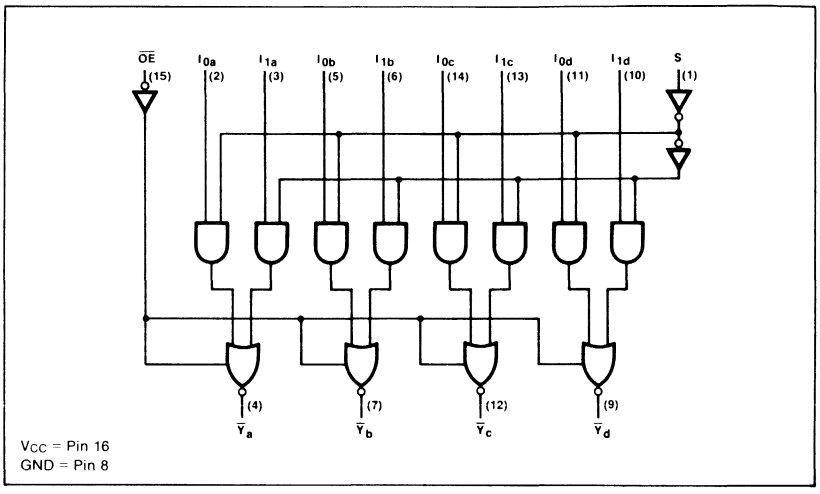
Outputs are forced to a high impedance "off" state when the Output Enable Input ($\overline{OE}$) is HIGH. All but one device must be in the high impedance state to avoid currents exceeding the maximum ratings if outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE [b]

PARAMETER		TEST CONDITIONS		54/74		54S/74S		54LS/74LS		UNIT
				Min	Max	Min	Max	Min	Max	
V_{OL}	Output LOW voltage	V_{CC} = Min	I_{OL} = 20mA				0.5			V
			I_{OL} = 12mA						0.4	V
			I_{OL} = 24mA						0.5 [c]	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = See Fan Out Table				2.4		2.4		V
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V				-40	-100	-30	-100	mA
I_{CC}	Supply current	V_{CC} = Max	Outputs HIGH				56		7.0	mA
			Outputs LOW				81		14	mA
			Outputs "off"				87		19	mA

NOTES

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

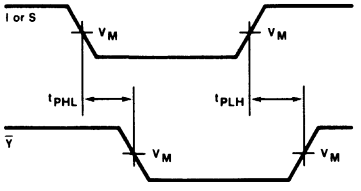
c. This parameter for Commercial range only.

AC CHARACTERISTICS T_A = 25°C (See Section 4 for Test Circuits and Conditions)

PARAMETER		TEST CONDITIONS		54/74		54S/74S C_L = 15pF R_L = 280Ω		54LS/74LS C_L = 45pF R_L = 667Ω		UNIT
				Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Figure 1					6.0 6.0		14 14	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Figure 1					12 12		21 24	ns ns
t_{PZH}	Output enable to HIGH level	Figure 2					19.5		16	ns
t_{PZL}	Output enable to LOW level	Figure 3					21		24	ns
t_{PHZ}	Output disable from HIGH level	Figure 2	C_L = 5pF				8.5		15	ns
			C_L = 45pF						43	
t_{PLZ}	Output disable from LOW level	Figure 3	C_L = 5pF				14		15	ns
			C_L = 45pF						19	

AC WAVEFORMS

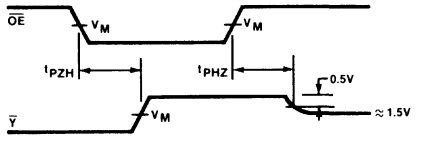
PROPAGATION DELAY DATA AND SELECT OUTPUT



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.

Figure 1

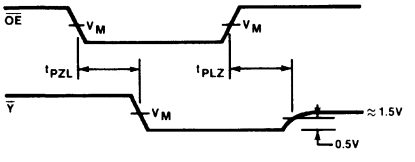
3-STATE ENABLE TIME TO HIGH LEVEL & DISABLE TIME FROM HIGH LEVEL



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.

Figure 2

3-STATE ENABLE TIME TO LOW LEVEL & DISABLE TIME FROM LOW LEVEL



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.

Figure 3