55/75460 • 55/75461 • 55/75462
55/75463 • 55/75464
DUAL HIGH VOLTAGE HIGH CURRENT PERIPHERAL DRIVERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The 55/75460 Peripheral Driver Series converts TTL and DTL logic levels to HIGH voltage, HIGH current levels. The 55/75460 Series is directly interchangeable with the 55/75450 Series and affords higher breakdown at the expense of speed. The 55/75460 Series features two 54/74 TTL input gates and two HIGH voltage HIGH current npn uncommitted transistors.

The 55/75461, 55/75462, 55/75463 and 55/75464 feature two standard 54/74 TTL input gates in AND, NAND, OR and NOR configurations, respectively. The logic gates are internally connected to the bases of the npn transistors.

- **NO OUTPUT LATCH-UP AT 30 V**
- **MEDIUM SWITCHING SPEED**
- **300 mA OUTPUT CURRENT CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**
- **INPUT CLAMP DIODES**
- **+5 V SUPPLY VOLTAGE**

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TEST TABLE 1 – Operating Temperature Range and Supply Voltage Range

	55460 Series	75460 Series
Temperature, T_A	−55°C to +125°C	0°C to 70°C
Supply Voltage, V_{CC}	+4.5 V to +5.5 V	+4.75 V to +5.25 V

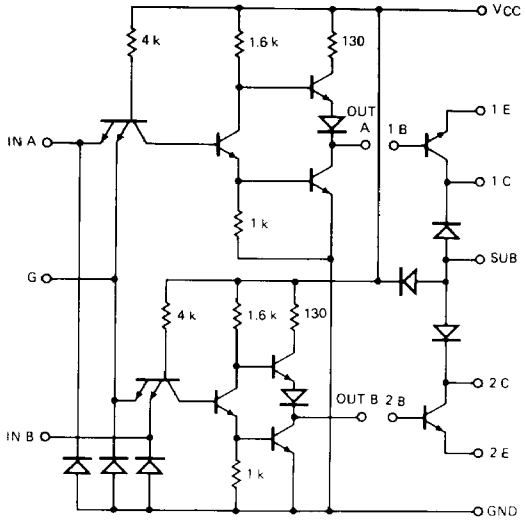
ABSOLUTE MAXIMUM RATINGS

	55460	75460	55461 55462 55463 55464	75461 75462 75463 75464
Supply Voltage, V_{CC} (Note 1)	7 V	7 V	7 V	7 V
Input Voltage (Note 1)	5.5 V	5.5 V	5.5 V	5.5 V
Interemitter Voltage (Note 2)	5.5 V	5.5 V	5.5 V	5.5 V
V_{CC} to Substrate Voltage (Note 6)	40 V	40 V		
Collector to Substrate Voltage (Note 6)	40 V	40 V		
Collector to Base Voltage	40 V	40 V		
Collector to Emitter Voltage (Note 3)	40 V	40 V		
Emitter to Base Voltage	5 V	5 V		
Output Voltage (Notes 1 and 4)			35 V	35 V
Continuous Collector Current (Note 5)	300 mA	300 mA		
Continuous Output Current (Note 5)			300 mA	300 mA
Continuous Total Power Dissipation (Note 7)	800 mW	800 mW	800 mW	800 mW
Operating Ambient Temperature Range	−55°C to +125°C	0°C to 70°C	−55°C to +125°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Pin Temperature				
Molded DIP (Soldering, 10 s)		260°C	260°C	260°C
Hermetic DIP (Soldering, 30 s)	300°C	300°C	300°C	300°C

NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter input transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This is the maximum voltage which should be applied to any output when it is in the off state.
5. Both halves of these dual curcuits may conduct rated current simultaneously.
6. For the 55460 and 75460 only, the substrate (Pin 8), must always be at the most negative device voltage for proper operation.
7. Above 70°C ambient temperature, derate linearly at 8.3 mW/°C for hermetic DIP.
   For plastic Mini DIP and hermetic Mini DIP derate above 30°C at 6.7 mW/°C.

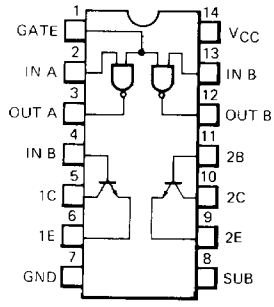
55460/75460
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT



All resistor values in ohms.

CONNECTION DIAGRAM
14-PIN DIP
(TOP VIEW)
PACKAGE OUTLINES 6A 9A
PACKAGE CODES D P



LOGIC FUNCTION

Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = \overline{XY}$ (gate and transistor)

ORDER INFORMATION

TYPE	PART NO.
55460	55460DM
75460	75460DC
75460	75460PC

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

TTL Gates

SYMBOL	CHARACTERISTICS		TEST FIGURE	CONDITIONS		MIN	TYP (Note 8)	MAX	UNITS
V_{IH}	Input HIGH Voltage		1			2			V
V_{IL}	Input LOW Voltage		2					0.8	V
V_{CD}	Input Clamp Diode Voltage		3	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
V_{OH}	Output HIGH Voltage		2	V_{CC} = MIN, V_{IL} = 0.8 V I_{OH} = -400 µA		2.4	3.3		V
V_{OL}	Output LOW Voltage		1	V_{CC} = MIN, V_{IH} = 2 V	55460		0.25	0.5	V
				I_{OL} = 16 mA	75460		0.25	0.4	
I_I	Input Current at Maximum Input Voltage	Input A, B	4	V_{CC} = MAX, V_I = 5.5 V				1	mA
		Gate						2	
I_{IH}	Input HIGH Current	Input A, B	4	V_{CC} = MAX, V_I = 2.4 V				40	µA
		Gate						80	
I_{IL}	Input LOW Current	Input A, B	3	V_{CC} = MAX, V_I = 0.4 V				-1.6	mA
		Gate						-3.2	
I_{OS}	Short Circuit Output Current (Note 9)		5	V_{CC} = MAX		-18	-35	-55	mA
I_{CCH}	Supply Current, Output HIGH		6	V_{CC} = MAX, V_I = 0 V			2.8	4	mA
I_{CCL}	Supply Current, Output LOW			V_{CC} = MAX, V_I = 5 V			7	11	

NOTES:
8. All typical values at V_{CC} = 5 V, T_A = 25°C.
9. Not more than one output should be shorted at a time.

55460/75460

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

Output Transistors

SYMBOL	CHARACTERISTICS	CONDITIONS		MIN	TYP (Note 10)	MAX	UNITS
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0		40			V
$V_{(BR)CER}$	Collector to Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		40			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio (Note 11)	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C		25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			
		V_{CE} = 3 V, I_C = 100 mA	55460 T_A=−55°C	10			
			75460 T_A=0°C	20			
		V_{CE} = 3 V, I_C = 300 mA	55460 T_A=−55°C	15			
			75460 T_A=0°C	25			
$V_{BE(sat)}$	Base to Emitter Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55460		0.85	1.2	V
			75460		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA	55460		1.0	1.4	V
			75460		1.0	1.2	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage (Note 11)	I_B = 10 mA, I_C = 100 mA	55460		0.25	0.5	V
			75460		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA	55460		0.45	0.8	V
			75460		0.45	0.7	V

NOTES:
10. All typical values are at V_{CC} = 5 V, T_A = 25°C.
11. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

TTL Gates

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	12	C_L = 15 pF, R_L = 400 Ω		22		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				8		ns

Output Transistors

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS (Note 12)	MIN	TYP	MAX	UNITS
t_d	Delay Time	13	I_C = 200 mA, $V_{BE(off)}$ = −1 V		10		ns
t_r	Rise Time		$I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA		16		ns
t_s	Storage Time		C_L = 15 pF, R_L = 50 Ω		23		ns
t_f	Fall Time				14		ns

Gates and Transistors Combined

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω		45	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				35	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				10	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_C \approx$ 300 mA R_{BE} = 500 Ω	V_S −10			mV

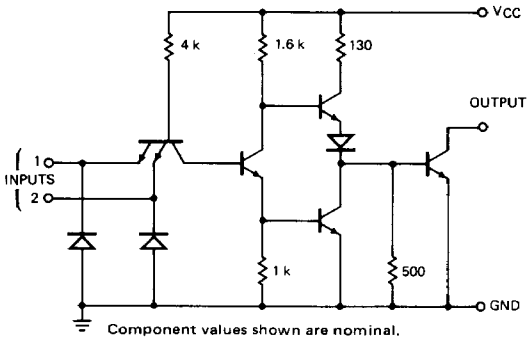
NOTE 12. Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

7

55461/75461

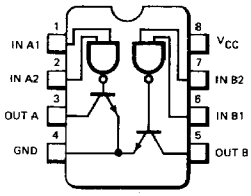
DUAL POSITIVE AND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUT		OUTPUT
1	2	
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55461	55461RM
75461	75461RC
75461	75461TC

Positive Logic: $Z = XY$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated.

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 13)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IH} = 2 V	55461			300	μA
				75461			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55461		.16	0.5	V
				75461		.16	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55461		.35	0.8	
				75461		.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			61	76	mA

NOTE 13. All typical values are at V_{CC} = 5 V, T_A = 25°C.

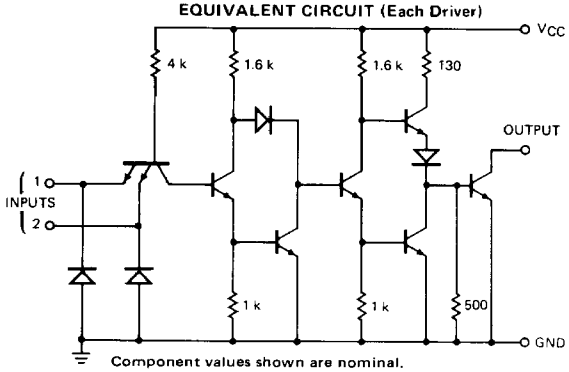
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

55462/75462

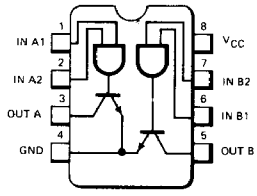
DUAL POSITIVE NAND PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAM
8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	H	(off state)
L	H	H	(off state)
H	L	H	(off state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level.

ORDER INFORMATION

TYPE	PART NO.
55462	**7562RM**
75462	75462RC
75462	75462TC

Positive Logic: $Z = \overline{XY}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 14)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA			-1.2	-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IL} = 0.8 V	55462			300	μA
				75462			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55462		.16	0.5	V
				75462		.16	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55462		.35	0.8	
				75462		.35	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	10	V_{CC} = MAX, V_I = 0 V			13	17	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			65	76	mA

NOTE 14. All typical values are at V_{CC} = 5 V, T_A = 25°C.

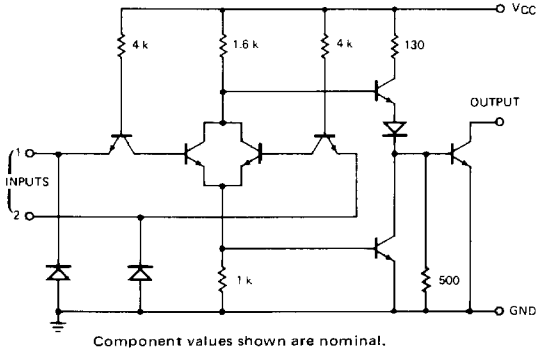
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				40	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

55463/75463

DUAL POSITIVE OR PERIPHERAL DRIVER

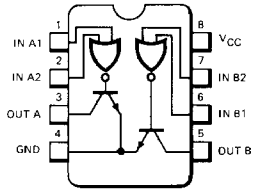
EQUIVALENT CIRCUIT (Each Driver)



Component values shown are nominal.
All resistor values in ohms.

CONNECTION DIAGRAM

8-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9T 6T
PACKAGE CODE T R



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	L	(on state)
L	H	H	(off state)
H	L	H	(off state)
H	H	H	(off state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55463	55463RM
75463	75463RC
75463	75463TC

Positive Logic: $Z = X + Y$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 15)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = −12 mA			−1.2	−1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IH} = 2 V	55463			300	μA
				75463			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA	55463		0.18	0.5	V
				75463		0.18	0.4	
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA	55463		0.39	0.8	
				75463		0.39	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			−1.0	−1.6	mA
I_{CCH}	Supply Current Output HIGH	11	V_{CC} = MAX, V_I = 5 V			8.0	11	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 0 V			63	76	mA

NOTE 15 All typical values are at V_{CC} = 5 V, T_A = 25°C.

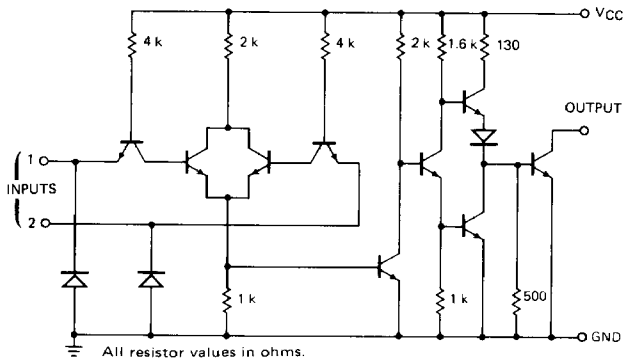
AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		45	55	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				30	40	ns
t_{TLH}	Transition Time, Output LOW to HIGH				8	25	ns
t_{THL}	Transition Time, Output HIGH to LOW				10	25	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S −10			mV

55464/75464

DUAL POSITIVE NOR PERIPHERAL DRIVER

EQUIVALENT CIRCUIT (Each Driver)



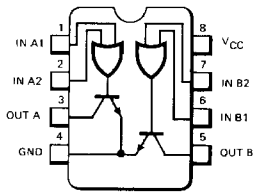
CONNECTION DIAGRAM

8-PIN DIP

(TOP VIEW)

PACKAGE OUTLINE 9T 6T

PACKAGE CODE T R



TRUTH TABLE

INPUT		OUTPUT	
1	2		
L	L	H	(off state)
L	H	L	(on state)
H	L	L	(on state)
H	H	L	(on state)

H = HIGH Level, L = LOW Level

ORDER INFORMATION

TYPE	PART NO.
55464	**55464RM**
75464	75464RC
75464	75464TC

Positive Logic: $Z = \overline{X + Y}$

ELECTRICAL CHARACTERISTICS: Guaranteed over Operating Temperature Range and Supply Voltage Range, use Test Table 1, pg. 1, unless otherwise indicated

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS		MIN	TYP (Note 16)	MAX	UNITS
V_{IH}	Input HIGH Voltage	7			2			V
V_{IL}	Input LOW Voltage	7					0.8	V
V_{CD}	Input Clamp Diode Voltage	8	V_{CC} = MIN, I_I = -12 mA				-1.5	V
I_{OH}	Output HIGH Current	7	V_{CC} = MIN, V_{OH} = 35 V, V_{IL} = 0.8 V	55464			300	μA
				75464			100	
V_{OL}	Output LOW Voltage	7	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA	55464		0.17	0.5	V
				75464		0.17	0.4	
			V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA	55464		0.38	0.8	
				75464		0.38	0.7	
I_I	Input Current at Maximum Input Voltage	9	V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	Input HIGH Current	9	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Input LOW Current	8	V_{CC} = MAX, V_I = 0.4 V			-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	11	V_{CC} = MAX, V_I = 0 V			14	19	mA
I_{CCL}	Supply Current Output LOW		V_{CC} = MAX, V_I = 5 V			72	85	mA

NOTE 16. All typical values are at V_{CC} = 5 V, T_A = 25°C.

AC CHARACTERISTICS: V_{CC} = 5 V, T_A = 25°C

SYMBOL	CHARACTERISTICS	TEST FIGURE	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	14	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω		50	65	ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				40	50	ns
t_{TLH}	Transition Time, Output LOW to HIGH				12	20	ns
t_{THL}	Transition Time, Output HIGH to LOW				15	20	ns
V_{OH}	HIGH Level Output Voltage After Switching	15	V_S = 30 V, $I_O \approx$ 300 mA	V_S -10			mV

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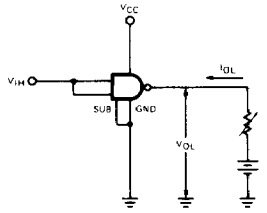
CHARACTERISTICS MEASUREMENT INFORMATION

DC TEST CIRCUIT†

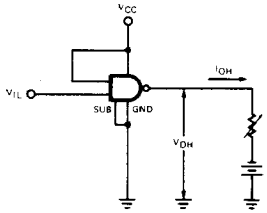
V_{IH}, V_{OL}



Both inputs are tested simultaneously.

Fig. 1

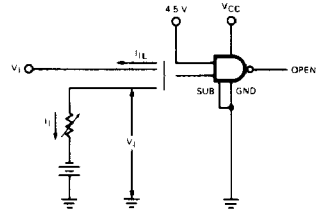
V_{IL}, V_{OH}



Each input is tested separately.

Fig. 2

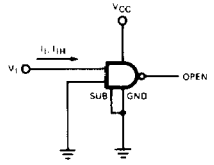
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing V_{CD}, input not under test is open.

Fig. 3

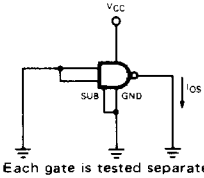
I_I, I_{IH}



Each input is tested separately

Fig. 4

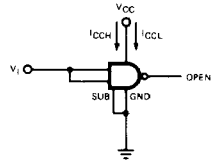
I_{OS}



Each gate is tested separately.
(55460/75460 only)

Fig. 5

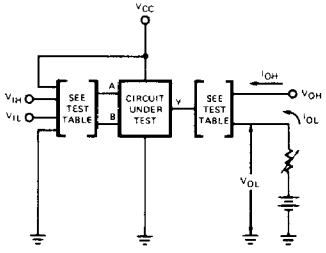
I_{CCH}, I_{CCL}



Both gates are tested simultaneously.

Fig. 6

V_{IH}, V_{IL}, I_{OH}, V_{OL}



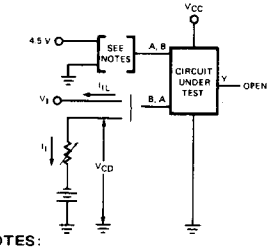
NOTE: Each input is tested separately.

Fig. 7

TEST TABLE II

CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
55/75461	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75462	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
55/75463	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
55/75464	V_{IH} V_{IL}	GND V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

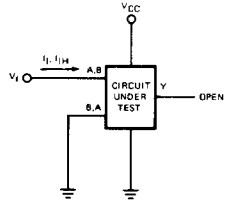
V_{CD}, I_{IL}



NOTES:
A. Each input is tested separately.
B. When testing I_{IL} 55/75463 and 55/75464, the input not under test is grounded. For all other circuits it is at 4.5V.
C. When testing V_{CD}, input not under test is open.

Fig. 8

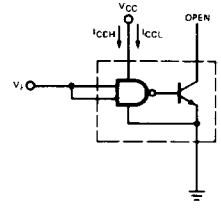
I_I, I_{IH}



Each input is tested separately.

Fig. 9

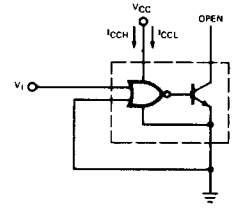
I_{CCH}, I_{CCL} FOR AND, NAND CIRCUITS



Both gates are tested simultaneously.

Fig. 10

I_{CCH}, I_{CCL} FOR OR, NOR CIRCUITS



Both gates are tested simultaneously.

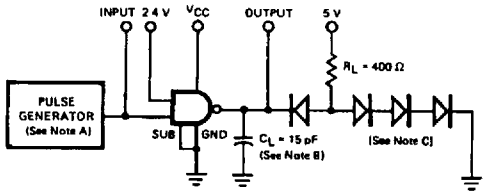
Fig. 11

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

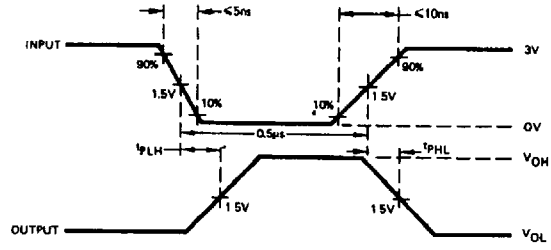
CHARACTERISTICS MEASUREMENT INFORMATION
SWITCHING CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE
(55460, 75460 ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES: A. The pulse generator has the following characteristics:
PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are FD777.

Fig. 12

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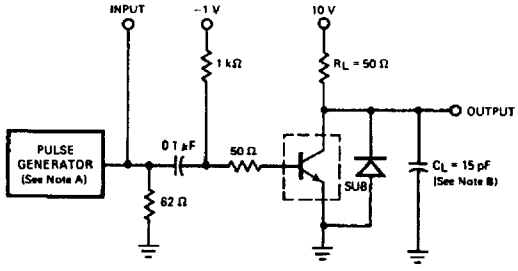
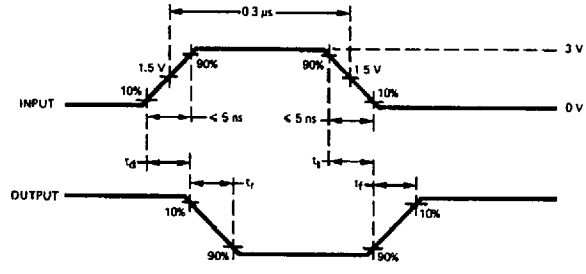
SWITCHING TIMES, EACH TRANSISTOR
(55460, 75460 ONLY)

TEST CIRCUIT



VOLTAGE WAVEFORMS

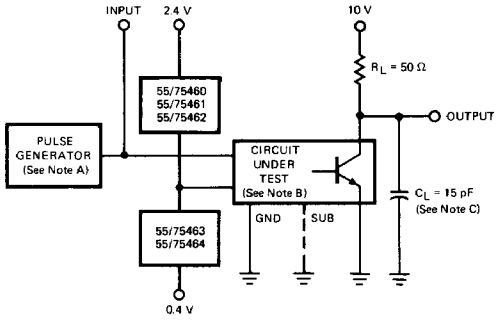


NOTES: A. The pulse generator has the following characteristics:
duty cycle < 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

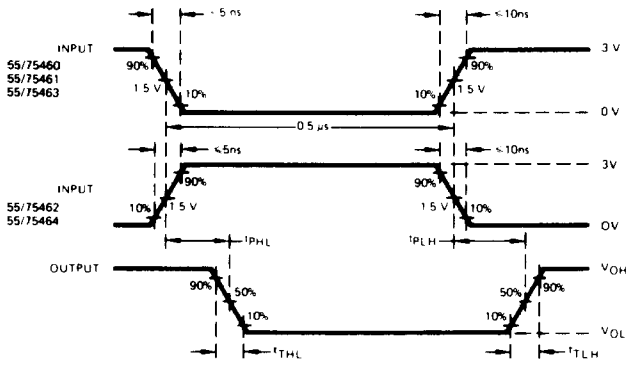
Fig. 13

SWITCHING TIMES OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

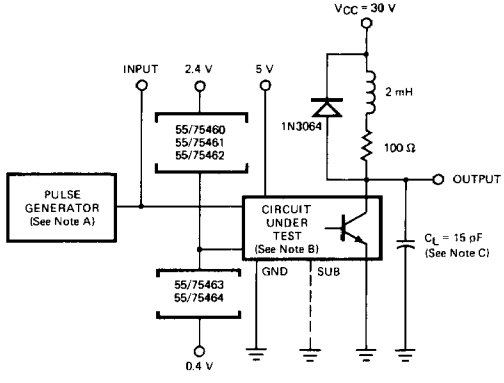


NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. When testing 55460/75460, connect output Y to transistor base and ground the substrate terminal
C. C_L includes probe and jig capacitance.

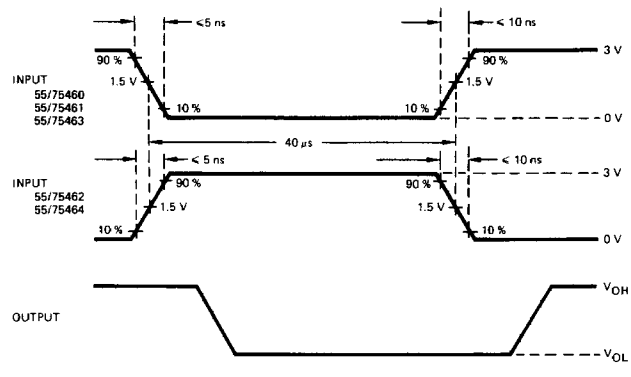
Fig. 14

LATCH-UP TEST OF COMPLETE DRIVERS

TEST CIRCUIT



VOLTAGE WAVEFORMS

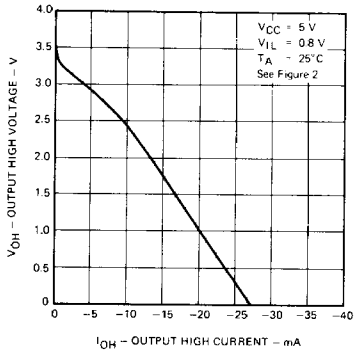


NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing 55460 or 75460, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

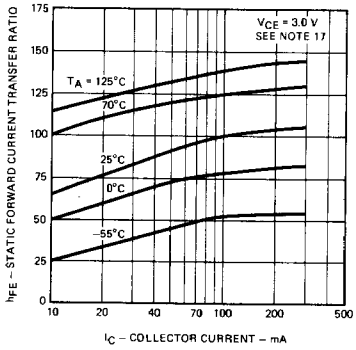
Fig. 15

TYPICAL PERFORMANCE CURVES FOR 55460/75460 SERIES

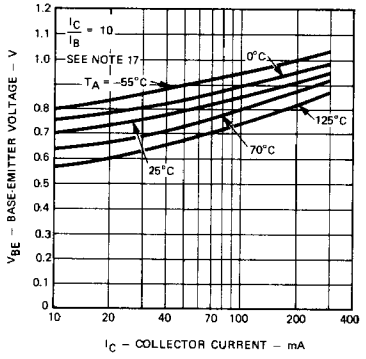
55460/75460 TTL GATE OUTPUT HIGH VOLTAGE AS A FUNCTION OF OUTPUT HIGH CURRENT



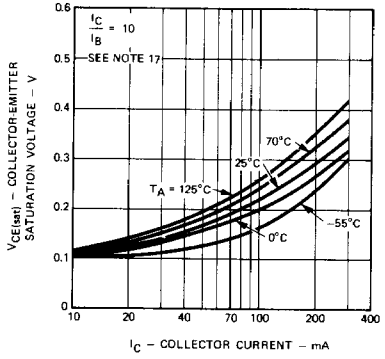
55460/75460 TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT



55460/75460 TRANSISTOR BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



TRANSISTOR COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT



NOTE 17. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

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