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APPLICATION BRIEF

AB-13

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TTL Library for EPLD Designs

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INTEL CORPORATION

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The following designs are examples taken from Intel's TTL design library. In most cases the designs were generated using the Logic Builder and schematics presented in the TTL data book. The designs in the library contain many techniques that may be useful in other applications of EPLDs.

The complete TTL library is available in the Advanced Design File (ADF) format via an auto-answer modem link at Intel. For more information, interested parties should contact their local Intel sales office.

74160 ADF

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JRD
Intel
March 31, 1986
74160
0
5C060
5C060 file for 74160 decade counter
LB Version 3.0, Baseline 17x, 9/26/85
PART:
        5C060
INPUTS:
        LOAD, DATA_A, DATA_B, CLOCK, DATA_C, DATA_D, CLEAR, EN_P, EN_T
OUTPUTS:
        QA, QB, QC, QD, RCO
NETWORK:
        CLK = INP(CLOCK)
        LOAD = INP(LOAD)
        DATAA = INP(DATA_A)
        DATAB = INP(DATA_B)
        DATAC = INP(DATA_C)
        DATAD = INP(DATA_D)
        CLR = INP(CLEAR)
        ENP = INP(EN_P)
        ENT = INP(EN_T)
        RCO = CONF(RCOIN, VCC)
        QD, QDF = TOTF(NDD, CLK, CLRNOT, GND, VCC)
        QC, QCF = TOTF(NCD, CLK, CLRNOT, GND, VCC)
        QB, QBF = TOTF(NBD, CLK, CLRNOT, GND, VCC)
        QA, QAF = TOTF(NAD, CLK, CLRNOT, GND, VCC)
EQUATIONS:
        RCOIN = QDF * QAF * ENT;

        CLRNOT = CLR';

        NAD = QAF * LOAD' * DATAA'
                + QAF' * LOAD' * DATAA
                + ENP * ENT * LOAD;

        NBD = QBF * LOAD' * DATAB'
                + QBF' * LOAD' * DATAB
                + QAF * ENP * ENT * QDF' * LOAD;

        NCD = QCF * LOAD' * DATAC'
                + QCF' * LOAD' * DATAC
                + QBF * QAF * ENP * ENT * LOAD;

        NDD = QDF * LOAD' * DATAD'
                + QDF' * LOAD' * DATAD
                + QDF * QAF * LOAD * ENP * ENT
                + QCF * QBF * QAF * LOAD * ENP * ENT;

END$
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292017-1

7485 ADF

```
JRD
Intel
April 1, 1986
7485
0
5C031
5C031 implementation of a 7485
LB Version 3.0, Baseline 17x, 9/26/85
PART:
        5C031
INPUTS:
        A3, B3, A2, B2, A1, B1, A0, B0, AGTB, ALTB, AEQB
OUTPUTS:
        A>B, A<B, EQUAL, A3XORB3, A2XORB2, A1XORB1, A0XORB0
NETWORK:
        A3 = INP(A3)
        B3 = INP(B3)
        A2 = INP(A2)
        B2 = INP(B2)
        A1 = INP(A1)
        B1 = INP(B1)
        A0 = INP(A0)
        B0 = INP(B0)
        AGTB = INP(AGTB)
        ALTB = INP(ALTB)
        5 = INP(AEQB)
        A>B = CONF(AGREATB, VCC)
        A<B = CONF(ALESSB, VCC)
        EQUAL = CONF(EQ, VCC)
        A3XORB3, A3XB3F = COIF(A3XORB3, VCC)
        A2XORB2, A2XB2F = COIF(A2XORB2, VCC)
        A1XORB1, A1XB1F = COIF(A1XORB1, VCC)
        A0XORB0, A0XB0F = COIF(A0XORB0, VCC)
EQUATIONS:
        A0XORB0 = B0' * A0
                + B0 * A0';

        A1XORB1 = B1' * A1
                + B1 * A1';

        A2XORB2 = B2' * A2
                + B2 * A2';

        A3XORB3 = B3' * A3
                + B3 * A3';

        EQ = 5 * A3XB3F' * A2XB2F' * A1XB1F' * A0XB0F';

        ALESSB = B3 * A3'
               + B2 * A3XB3F' * A2'
               + A3XB3F' * A2XB2F' * B1 * A1'
               + A3XB3F' * A2XB2F' * A1XB1F' * ALTB * A0XB0F'
               + A3XB3F' * B0 * A2XB2F' * A1XB1F' * A0';

        AGREATB = A3 * B3'
                + A2 * B2' * A3XB3F'
                + A3XB3F' * A1 * B1' * A2XB2F'
                + A3XB3F' * A2XB2F' * A1XB1F' * AGTB * A0XB0F'
                + A3XB3F' * A2XB2F' * A0 * B0' * A1XB1F';

END$
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292017-2

74164 ADF

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JRD
INTEL
March 31, 1986
74164
0
5C031
5C031 IMPLEMENTATION OF 74164
LB Version 3.0, Baseline 17x, 9/26/85
PART:
        5C031
INPUTS:
        CLEAR, CLOCK, INPA, INPB
OUTPUTS:
        QA, QB, QC, QD, QE, QF, QG, QH
NETWORK:
        CLK = INP(CLOCK)
        CLEAR = INP(CLEAR)
        INPA = INP(INPA)
        INPB = INP(INPB)
        QH = RONF(NHD, CLK, CLEARNOT, GND, VCC)
        QG, QGF = RORF(NGD, CLK, CLEARNOT, GND, VCC)
        QF, QFF = RORF(NFD, CLK, CLEARNOT, GND, VCC)
        QE, QEF = RORF(NED, CLK, CLEARNOT, GND, VCC)
        QD, QDF = RORF(NDD, CLK, CLEARNOT, GND, VCC)
        QC, QCF = RORF(NCD, CLK, CLEARNOT, GND, VCC)
        QB, QBF = RORF(NBD, CLK, CLEARNOT, GND, VCC)
        QA, QAF = RORF(NAD, CLK, CLEARNOT, GND, VCC)
EQUATIONS:
        NHD = QGF;

        NGD = QFF;

        NFD = QEF;

        NED = QDF;

        NDD = QCF;

        NCD = QBF;

        NBD = QAF;

        CLEARNOT = CLEAR';

        NAD = INPA * INPB;

END$
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292017-3

4020 ADF

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JRD
INTEL
April 1, 1986
4020
0
5C060
5C060 IMPLEMENTATION OF A 4020 14-BIT COUNTER
LB Version 3.0, Baseline 17x, 9/26/85
PART:
        5C060
INPUTS:
        CLR, CLK, VCC
OUTPUTS:
        QA, QD, QE, QF, QG, QH, QI, QJ, QK, QL, QM, QN, QC, QB
NETWORK:
        CLR = INP(CLR)
        CLK = INP(CLK)
        HIGH = INP(VCC)
        CLKBUF = CLKB(CLK)

        QA, QAF = TOTF(HIGH, CLKBUF, CLR, GND, VCC)
        QABUF = CLKB(QAF)

        QB, QBF = TOTF(HIGH, QABUF, CLR, GND, VCC)
        QBBUF = CLKB(QBF)

        QC, QCF = TOTF(HIGH, QBBUF, CLR, GND, VCC)
        QCBUF = CLKB(QCF)

        QD, QDF = TOTF(HIGH, QCBUF, CLR, GND, VCC)
        QDBUF = CLKB(QDF)

        QE, QEF = TOTF(HIGH, QDBUF, CLR, GND, VCC)
        QEBUF = CLKB(QEF)

        QF, QFF = TOTF(HIGH, QEBUF, CLR, GND, VCC)
        QFBUF = CLKB(QFF)

        QG, QGF = TOTF(HIGH, QFBUF, CLR, GND, VCC)
        QGBUF = CLKB(QGF)

        QH, QHF = TOTF(HIGH, QGBUF, CLR, GND, VCC)
        QHBUF = CLKB(QHF)

        QI, QIF = TOTF(HIGH, QHBUF, CLR, GND, VCC)
        QIBUF = CLKB(QIF)

        QJ, QJF = TOTF(HIGH, QIBUF, CLR, GND, VCC)
        QJBUF = CLKB(QJF)

        QK, QKF = TOTF(HIGH, QJBUF, CLR, GND, VCC)
        QKBUF = CLKB(QKF)

        QL, QLF = TOTF(HIGH, QKBUF, CLR, GND, VCC)
        QLBUF = CLKB(QLF)

        QM, QMF = TOTF(HIGH, QLBUF, CLR, GND, VCC)
        QMBUF = CLKB(QMF)

        QN = TONF(HIGH, QMBUF, CLR, GND, VCC)
EQUATIONS:
END$
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292017-4

74178 ADF

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jrd
intel
April 3, 1986
74178
0
5C031
5C031 IMPLEMENTATION OF 74178 SHIFT REG
LB Version 3.0, Baseline 17x, 9/26/85
PART:
        5C031
INPUTS:
        SERIAL, DATA_A, LOAD, DATA_B, DATA_C, DATA_D, SHIFT, CLK
OUTPUTS:
        QA178, QB178, QC178, QD178
NETWORK:
        NCLK = INP(CLK)
        NSERIAL = INP(SERIAL)
        NDATAA = INP(DATA_A)
        NLOAD = INP(LOAD)
        NDATAB = INP(DATA_B)
        NDATAC = INP(DATA_C)
        NDATAD = INP(DATA_D)
        NSHIFT = INP(SHIFT)
        QD178, NQDF = RORF(N3D, NCLK, GND, GND, VCC)
        QC178, NQCF = RORF(N2D, NCLK, GND, GND, VCC)
        QB178, NQBF = RORF(N1D, NCLK, GND, GND, VCC)
        QA178, NQAF = RORF(N0D, NCLK, GND, GND, VCC)
EQUATIONS:
        N0D = NSERIAL * NSHIFT
                + NQAF * NSHIFT' * NLOAD'
                + NSHIFT' * NDATAA * NLOAD;

        N1D = NQAF * NSHIFT
                + NQBF * NSHIFT' * NLOAD'
                + NSHIFT' * NDATAB * NLOAD;

        N2D = NQBF * NSHIFT
                + NQCF * NSHIFT' * NLOAD'
                + NSHIFT' * NDATAC * NLOAD;

        N3D = NQCF * NSHIFT
                + NQDF * NSHIFT' * NLOAD'
                + NSHIFT' * NDATAD * NLOAD;

END$
```

292017-5