intel

APPLICATION NOTE

AP-176

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2001 Non-Volatile RAM Protects Critical System Data at Low Cost

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INTRODUCTION: NON-VOLATILE RAM INCREASES SYSTEM FLEXIBILITY

The 2001 Non-Volatile RAM, or NVRAM, provides the system designer with RAM-like memory that always retains data, regardless of whether system power is on or off. The 2001 has the non-volatility of an E2PROM, and the unlimited write capability of static RAM. This allows the 2001 NVRAM to be used in applications requiring RAM flexibility as well as non-volatility. During normal operating conditions, the 2001's 128 byte RAM array is used like any static RAM memory. When the system is powered down, the RAM data is saved in non-volatile memory with one 10 millisecond STORE operation.

The 2001 is ideal for use with the Intel MCS®-51 microcontroller and the iAPX 188 microprocessor. The 2001's address and data lines are multiplexed together to allow direct connection to the address/data bus of the MSC-51 and iAPX 188, without the need for an external address latch. The multiple chip enable/selects on the 2001 eliminate the need for system memory decoding. This is useful in MCS-51 systems requiring a minimum parts count.

The 2001 is a fully integrated device, with the RAM array, non-volatile storage array, programming voltage supply (for the STORE operation), STORE sequencing circuitry, Data Protection circuit (which inhibits STORE operation when V_{CC} is below V_{LKO}), and address latch all included on-chip. The on-chip STORE sequencing circuitry allows the CPU to initiate a STORE operation with only a standard write pulse (with $\overline{NE}$ low). The on-chip STORE circuitry performs all the necessary steps to transfer the 1,024 bits of the RAM array data to the non-volatile storage array in 10 milliseconds.

Applications for the 2001 NVRAM include storage of critical system parameters during power-down or power-fail conditions, scratchpad memory for the CPU, or non-volatile memory for real-time event or error logging. In all of these cases, the 2001 can be written as often as desired, at microprocessor speeds. Data written to NVRAM remains stored indefinitely, intact during periods when no power is applied to the system. Non-volatile storage in the 2001 is guaranteed for at least 10 years. The 2001 NVRAM is a completely solid-state device, providing a rugged and reliable medium for storing critical information.

Because the 2001 NVRAM is very similar to Intel's 2004 NVRAM the methods of implementing power-down STORE operation are identical. For detailed information on implementing power-down STORE, and for additional examples of NVRAM applications, refer to Application Note AP-173 ("Designing the 2004 Non-Volatile RAM into your System").

This Application Note discusses a few of the many applications for NVRAMs, and shows how to design the 2001 NVRAM into systems using either the MCS-51 microcontroller or the iAPX 188 microprocessor.

DEVICE OPERATION

The 2001 has a 128 X 8 static RAM array that is backed up, bit for bit, by a non-volatile storage array. (See Figure 1) The non-volatile storage array uses Intel's proven FLOTOX technology.

Table 1 shows the operational modes for the 2001.

Read/Write Cycles

Writing data to and reading data from the 2001 NVRAM is done in the same manner as with any static RAM. Standard microprocessor read and write cycle timing is used. Read access time is 180 ns for the 2001-2. During read and write cycles the $\overline{NE}$ (Non-Volatile Enable) input is held high.

RECALL/STORE Operations

Performing a read cycle on the 2001 with $\overline{NE}$ held low initiates a RECALL operation. The RECALL operation transfers the data in the non-volatile storage array to the RAM array in 5 microseconds. The CPU can perform a RECALL at any time to reload the static RAM array from the non-volatile array. When power is initially applied to the 2001, an automatic RECALL occurs.

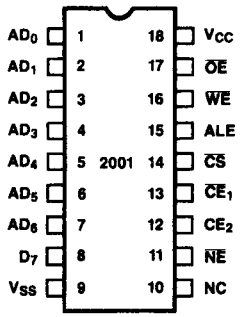
When a write cycle is performed on the 2001 with $\overline{NE}$ held low, a STORE operation is initiated. The STORE operation transfers the data in the RAM array to the non-volatile storage array. Once a STORE operation is started, the 2001 NVRAM on-chip circuitry peforms the necessary sequencing to write all the RAM array data into the non-volatile storage array. The programming voltage for writing the RAM data into the non-volatile storage cells is generated on-chip. During the STORE operation the 2001's data outputs go to a high impedance state, and all control signal inputs are ignored until the operation is completed. This allows the CPU to use the system bus for other processing tasks.

The STORE operation takes 10 milliseconds on the 2001.

STORE Endurance

The STORE endurance specification for the 2001 NVRAM is a minimum of 10,000 cycles. This means

2001 Pin Configuration



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2001 Functional Diagram

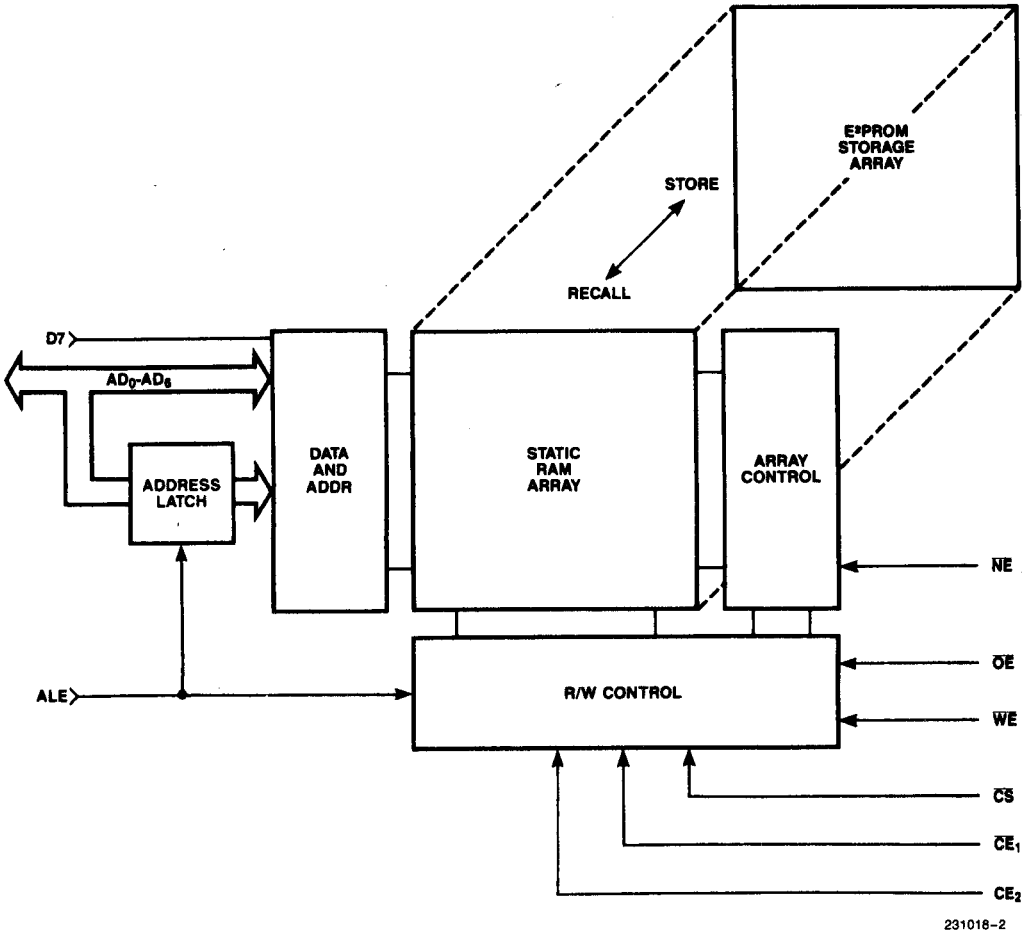

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Figure 1.

Table 1. 2001 Operational Modes $V_{CC} = 5V$

Mode \ Pin	$\overline{CE}_1$	CE_2	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{NE}$	Data
Standby	V_{IH}	X	X	X	X	X	Hi-Z
	X	V_{IL}	X	X	X	X	Hi-Z
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data In
Automatic RECALL At V_{CC} Power Up	X	X	X	X	X	X	Hi-Z
Normal RECALL	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Hi-Z
STORE	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Hi-Z

NOTES:

1. X = Don't Care.

2. The $\overline{CE}_1$ and CE_2 inputs are latched by the falling edge of ALE for Read and Write cycles. For STORE and RECALL initiation cycles, ALE may be either pulsed as in Write and Read cycles (see Write and Read cycles timing diagrams) or ALE can be held at V_{IH} for the active duration of $\overline{CS}$. In the latter case $\overline{CE}_1$ and CE_2 should also be held active for as long as $\overline{CS} = V_{IL}$.

that a minimum of 10,000 STORE operations can be reliably performed on the 2001. Each time a STORE operation is performed, all 128 bytes of the non-volatile storage array are written. In a system where a STORE operation is performed each time the system is powered down, it is important that the number of system power up/down cycles not exceed 10,000 during the product life of the system.

The key reason for using NVRAM is the ability to retain often-changed data during periods when no power is applied to the system. This is accomplished by accessing the NVRAM's RAM array during normal system operation, then performing a STORE operation each time the system is powered down. If a system is powered up and down more frequently than the critical data is changed, however, E2PROM memory such as the Intel 2817A may be the better choice for non-volatile storage of data. E2PROM memory need only be written as often as the data stored in the E2PROM is changed, which may not be as often as the system is powered up and down.

On-Chip STORE Lockout Circuit Provides Data Protection

Intel's 2001 NVRAM has an on-chip data protection circuit which prevents spurious STORE operations from occurring during system power up and power down. A spurious STORE can be initiated in an unprotected NVRAM by the unstable control signals in a system when V_{CC} is rising or falling. The 2001 has a STORE lockout circuit that inhibits the STORE function whenever the V_{CC} pin is below 4V (V_{LKO}). For more information about data protection, see Application Note AP-165.

Using The Multiple Chip Select/ Enables For Memory Decoding

The 2001 has three chip select/enable inputs. By connecting these inputs to system address lines the 2001 can be memory-mapped to a specific address range. This allows system memory decoding to be done without an external decoder package. In the MCS-51 example in Figure 5 the three chip select/enable inputs are connected to system addresses A_{13} – A_{15} in order to select the 2001 at address range 8000H – 807FH. In the iAPX 188 example in Figure 7 the $\overline{CE}_1$ and CE_2 inputs are used to select the 2001 within address block 80000H-C0000H. (See section "iAPX-188 Interface" for more details on Figure 7.)

APPLICATIONS FOR THE 2001 NVRAM

Figure 2 shows a 2001 NVRAM being used to save engine performance information for an MCS-51 subsystem in an aircraft. The performance log can be constantly updated and the data saved through system power-down and power interruptions. Multiple sub-systems such as this can be used to monitor a wide range of functions and sub-systems aboard the aircraft, freeing the main supervisory processor for overall system control.

The 2001 NVRAM in Figure 3 is used to store fault and performance information, as well as the system usage time, in an MCS-51 sub-system in a copying machine.

The intelligent terminal design in Figure 4 is based on an iAPX-188 microprocessor using the Intel 82730 Text Coprocessor. The 2001 NVRAM in the system

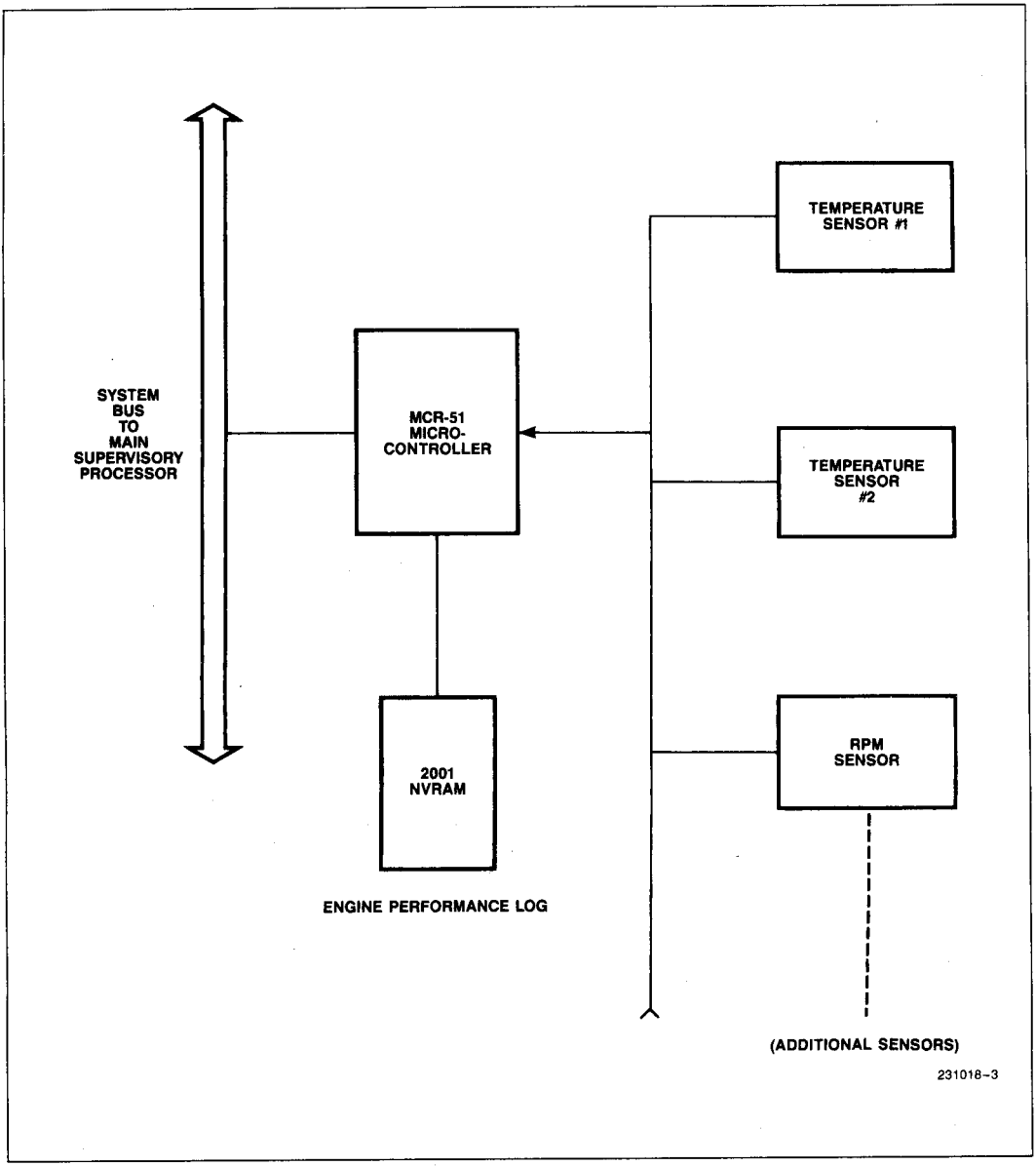

Figure 2. MCS®-51/2001 NVRAM in an Aircraft Engine Monitor

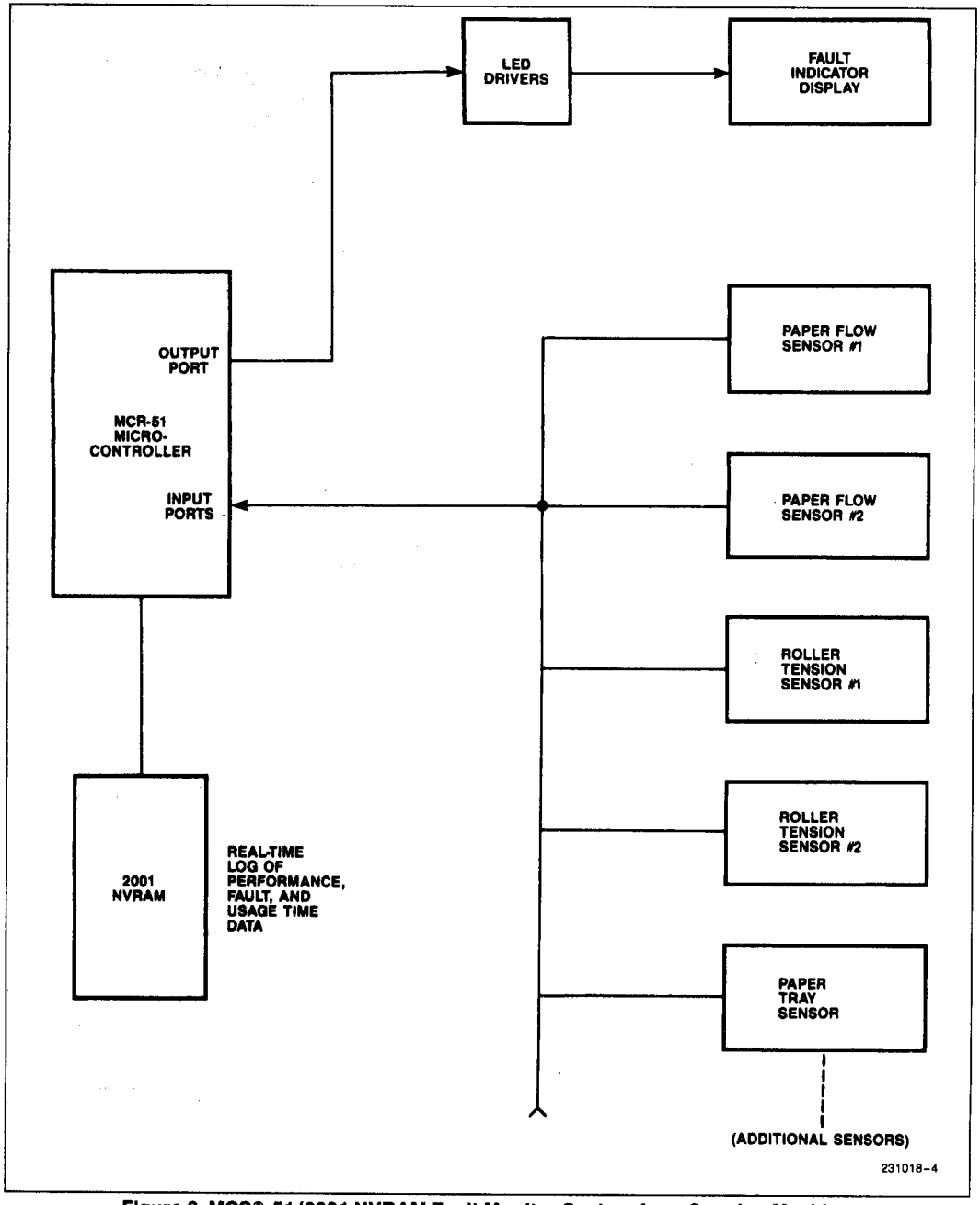

Figure 3. MCS®-51/2001 NVRAM Fault Monitor System for a Copying Machine

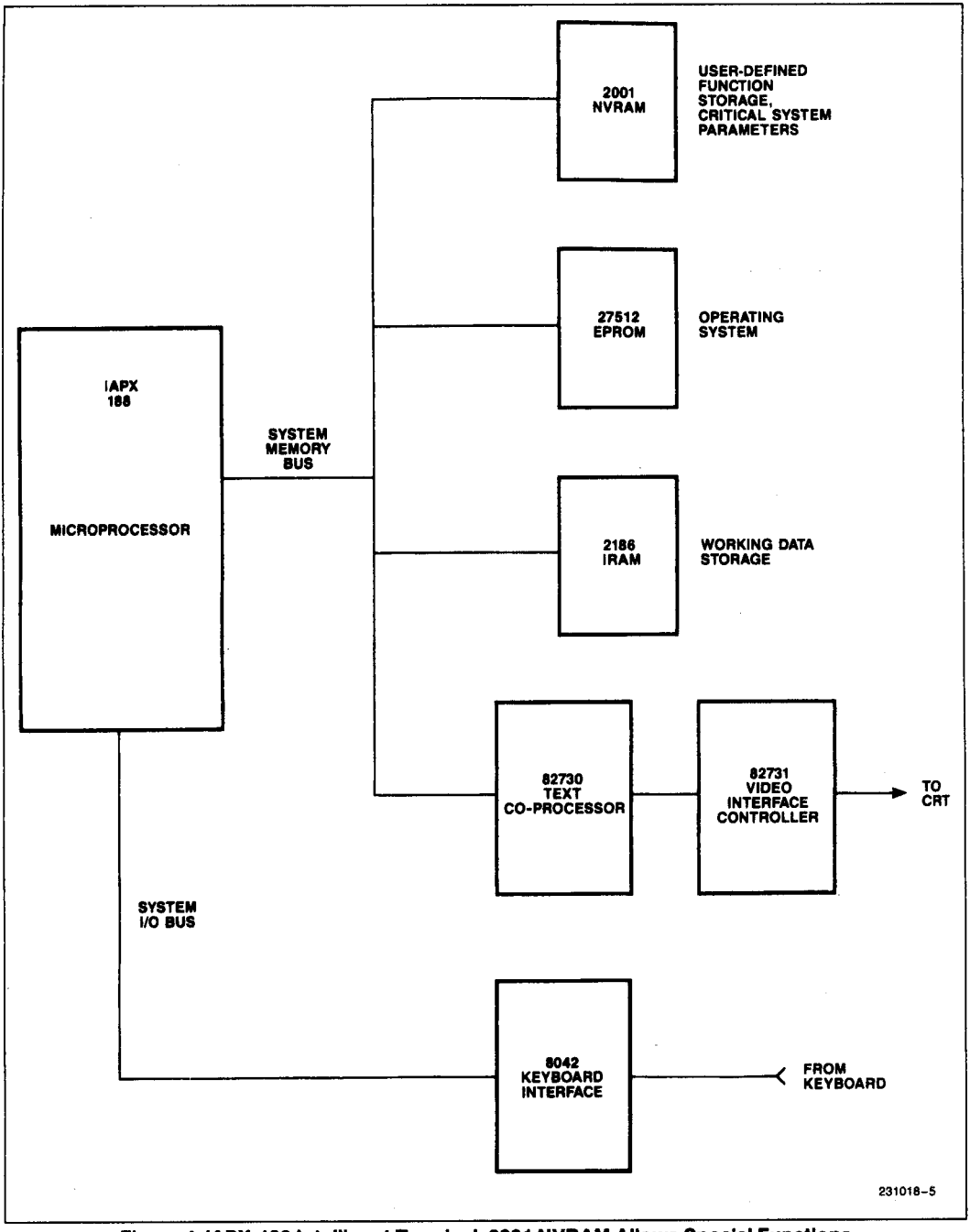

Figure 4. iAPX-188 Intelligent Terminal: 2001 NVRAM Allows Special Functions to be Defined by User Via Keyboard.

stores user-defined key functions. In this manner the user can define special functions that combine a series of standard terminal functions, to be activated upon one of a set of "soft" keys. The sequence is kept in the low-cost non-volatile 2001, and can be re-defined at any time from the keyboard. The 2001 can also be used to save constantly-changing critical system parameters during periods when the system is powered down.

A COMPLETE SYSTEM: THE MCS®-51 MICROCONTROLLER AND THE 2001 NVRAM

MCS-51 microcomputers have on-chip RAM, timers, and I/O ports, including a full-duplex UART serial port. The MCS-51 family has extensive bit manipulation capability as well as multiply and divide instructions. The MCS-51 family of single chip microcomputers includes the 8051 (4k ROM on-chip), the 8751 (4k EPROM on-chip), and the 8031 (no on-chip ROM or EPROM). An 8051 is used in the example in Figure 5.

The $\overline{CS}$, $\overline{CE}_1$, and CE_2 inputs to the 2001 are connected to address lines A_{13}, A_{14} and A_{15}, respectively, for the example shown in Figure 5. This causes the 2001 to be selected for the external memory address range of 8000H to 807FH. The port bit P1.2 drives the $\overline{NE}$ input to the 2001. For normal read/write access to the 2001, $\overline{NE}$ is held high. To perform either a STORE or a RECALL operation, the $\overline{NE}$ input is brought low.

A power-down STORE operation is initiated automatically in this system when the $\overline{POWER\ DOWN}$ signal from the power down detect module goes low. The activation of the $\overline{POWER\ DOWN}$ signal causes an interrupt to occur in the 8051. If there is any data in the 8051's internal RAM that is to be saved, the power down interrupt routine writes that data to the NVRAM. The $\overline{NE}$ input is then brought low by setting the P1.2 bit to "0". A write cycle is executed to the 2001, initiating a STORE operation. The V_{CC} supply will stay above 4.75V for the next 10 milliseconds while the STORE operation is completed. After initiating the STORE operation, the CPU can finish up any remaining system tasks before halting. The code sequence in Figure 6 is an example of a typical power-down STORE interrupt service routine.

USING THE 2001 IN AN iAPX 188 SYSTEM

The iAPX 188 is a microprocessor with an internal 16-bit wide data path, 16-bit wide registers and operations, and an 8-bit wide external data bus. In addition, the iAPX 188 has a number of peripheral functions built on-chip: an enhanced 8088-2 CPU, a clock generator, 2 independent DMA channels, a programmable interrupt controller, 3 programmable 16-bit timers, programmable memory and peripheral chip-select logic, a programmable wait-state generator, and a local bus controller. The iAPX 188 can directly address up to one megabyte of memory.

Figure 7 shows a block diagram example of an iAPX 188 system with a 2001 NVRAM. The integrated CPU component itself is called an 80188. For the example in Figure 7, read and write cycles to the 2001 are performed at address range 80000H-8007FH. The STORE/RECALL functions are memory-mapped at address 80800H. These addresses are determined by the 80188's MPCS and MMCS registers. The 2001's $\overline{CE}_1$ and CE_2 inputs are connected to addresses A_{18} and A_{19}, respectively, in order to power down the 2001's internal circuitry whenever the device is not being accessed. The $\overline{MCS0}/\overline{MCS1}$ outputs are not used to drive $\overline{CE}_1$ and CE_2 because of the ALE setup time requirement for these inputs.

The system EPROM and RAM memory devices for this example are mapped at addresses FC000H and 0H, respectively. A 27512 64k x 8 EPROM can be used to store the 80188's program code and a 2186 8k x 8 iRAM can be used as the system RAM for high-density working data storage.

The code in Figure 8 is an example for initiating a STORE operation in a system such as the one in Figure 7.

This code sequence can be used in a power down interrupt subroutine to save critical system parameters.

SUMMARY

This Application Note has discussed the operation of the 2001 NVRAM and has shown how to design the 2001 into systems that use the latest 8-bit microprocessors and microcomputers. The 2001 gives a system a non-volatile memory media that is inexpensive, reliable, and easy to use. By designing with all solid-state memories such as Intel's 2001 and 2004 NVRAMs and the 2817A and 2864 E2PROM, the flexibility and reliability of any system is greatly increased.

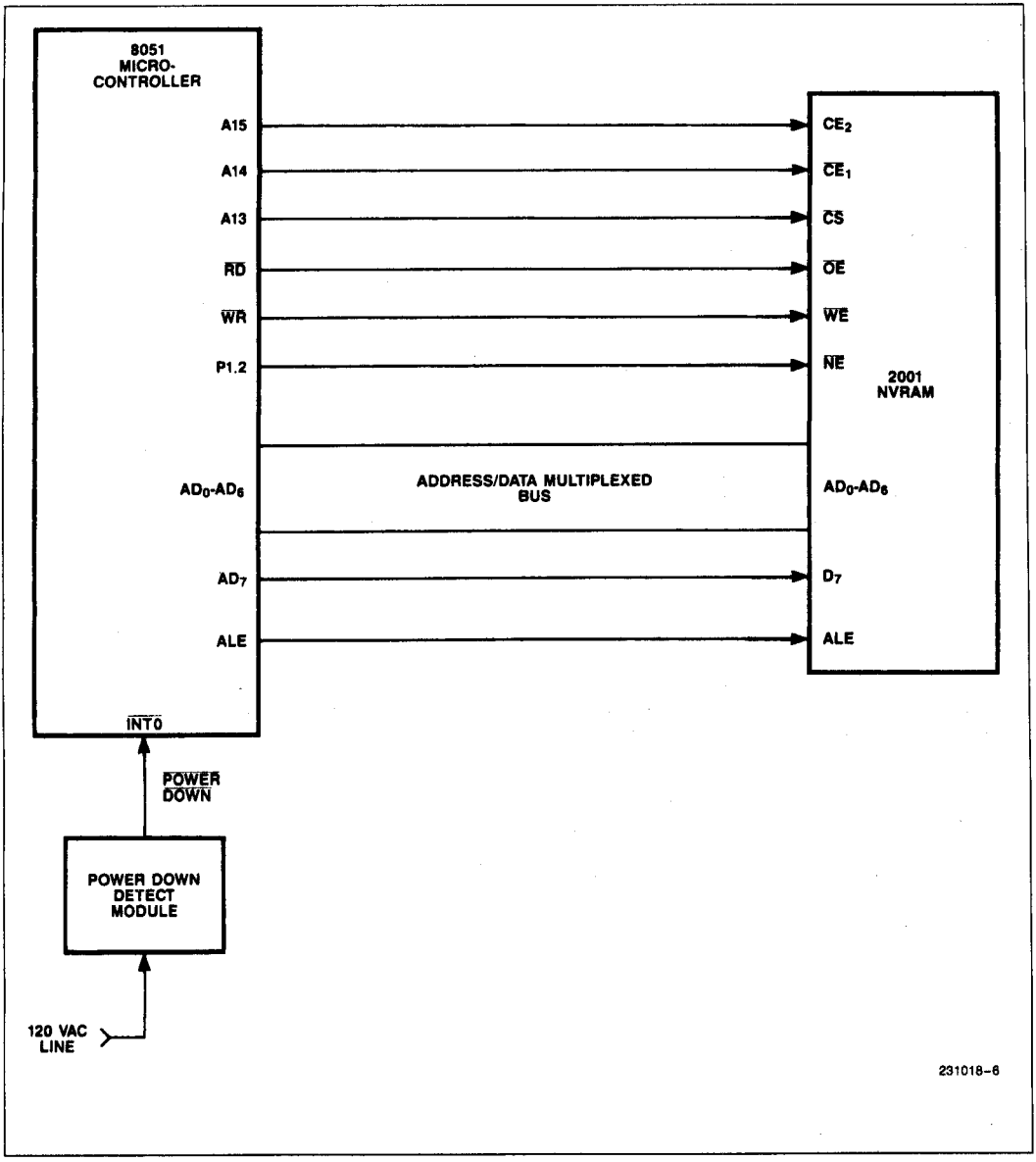

Figure 5. 2001/MCS®-51 System
Example: 2001 NVRAM mapped at External Memory Range 8000H-807FH

(Here code can be included to save internal 8051 RAM data by writing that data to the RAM array in the 2001. The code below STOREs that data in the 2001's non-volatile array.)

```
;
;
POWER DOWN STORE:
;
;
        CLR     P1.0            ;BRING NE LOW
;
        MOV     DPTR, #8000H    LOAD NVRAM ADDRESS
;
        MOVX    @DPTR, A        INITIATE A STORAGE OPERATION
;
        SETB    @P1.0           BRING NE HIGH
;
```

(V_{CC} is held up for 10 milliseconds. During this time any remaining system tasks can be finished up.)

```
;
;
        SJMP$                   ;TERMINATE PROCESSING
```

Figure 6

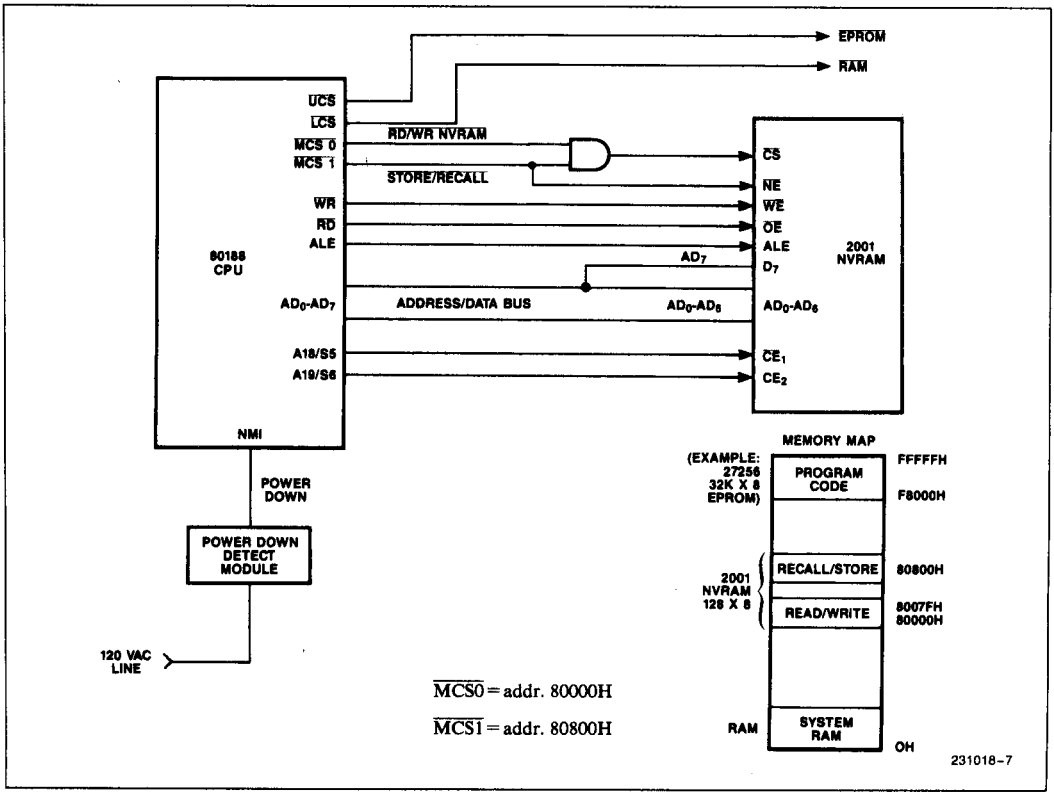

Figure 7. Using the 2001 NVRAM in an iAPX-188 System

```
;
;
        PUSH    ES                  ;SAVE ES REG.
        MOV     AX,8000H
        MOV     ES,AX               ;SET ES=8000H
;
        MOV     DI,800H
        MOV     ES:[DI],AL          ;INITIATE STORE OPERATION IN 2001
                                    ;AT ADDRESS 80800H
                                    ;(VALUE OF AL REG. = DON'T CARE)
;
        POP     ES                  ;RESTORE ES
;
;
;
;
```

Figure 8.