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Designing the 2004 NVRAM Into Your Microcontroller System Enhances Performance and Flexibility

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APPLICATION NOTE

Designing the 2004 NVRAM Into Your Microcontroller System Enhances Performance and Flexibility

By Justin Orion and Don Larson

The MCS®-96 microcontroller, with its 16-bit CPU and integrated I/O features, provides a cost-effective answer for real time control applications. The 2004 Non-Volatile Random Access Memory, or NVRAM, enhances the power and flexibility of MCS-96 based systems by adding RAM-like memory that is completely non-volatile.

The 2004 NVRAM combines the non-volatility of an E²PROM with the read/write functions of a static RAM. The 2004 serves as fast working memory and power-down or power-fail storage of critical system parameters. Real time data or event logging may also be performed with an NVRAM. In all cases, the NVRAM can be written as often as desired at microprocessor speeds. Data written into an NVRAM is stored indefinitely and remains intact when no power is applied to the system. The NVRAM is a completely solid-state device, providing a rugged and highly reliable medium for storing critical information.

This article highlights applications for the MCS-96 microcontroller, discusses the operation of the 2004 NVRAM, and promotes a highly functional and integrated kit solution for demanding real time control applications. Design considerations are detailed, including interfacing and the generation of appropriate control signals. Techniques for obtaining power-down detection signals and for delaying the fall of Vcc during power-down STORE operations are also discussed.

The MCS-96 Microcontroller Family

The MCS-96 family of 16-bit microcontrollers is designed for real time control applications requiring high throughput and system integration. Applications cut across most major market segments. In the industrial world, the MCS-96, with its high speed math processing and high speed I/O, is targeted for complex motor control and axis control systems. Applications include three-phase large horsepower AC motors and robotics.

With on-chip A/D conversion, the MCS-96 is also geared for data acquisition systems and closed loop analog controllers. In instrumentation such as a gas-chromatograph, the MCS-96 will prove useful by combining analog processing with high speed number crunching. These same attributes make the MCS-96 a desirable component for aerospace applications such as missile guidance and control.

In the communications market, high performance and the high level of integration will drive the MCS-96 into high speed modem, line card control, and cellular radio applications, among others. Finally, the MCS-96 will prove to be a powerful and cost effective controller for computer peripherals.

The 2004 NVRAM

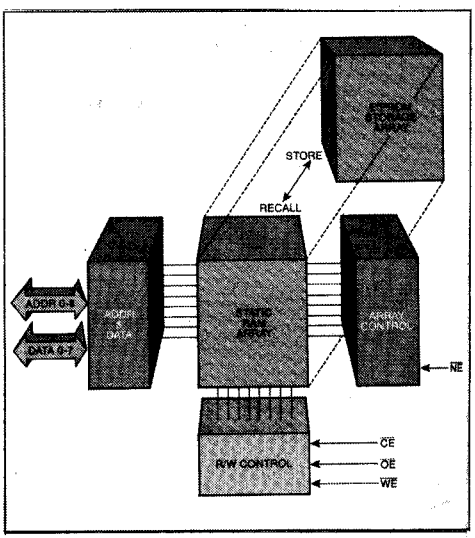
The 2004 NVRAM extends the functions of MCS-96-based systems and provides a highly integrated kit to OEMs. The 2004 gives the system designer RAM-like memory that always retains its data, regardless of whether system power is on or off. The 2004 NVRAM achieves this high level of memory functionality by combining the non-volatility of an industry-proven E²PROM with the read/write flexibility of a static RAM, all on the same chip. This allows the NVRAM to be used in applications that require RAM flexibility, as well as non-volatility.

Unlike an E²PROM, an NVRAM does not require a long cycle to write each byte. And, unlike the battery-backed RAMs, the NVRAM does not require batteries, or their necessary "glue" circuits to provide non-volatility. During normal operation the 2004's 512 byte RAM array is used like any static RAM memory. When system power is removed or lost, the entire contents of the RAM array can be saved in non-volatile memory with one 10 millisecond STORE operation. Upon restoration of system power, the data held in the non-volatile array are transferred automatically to the static RAM array. The RAM array, non-volatile array, programming voltage supply, and STORE sequencing circuitry are all contained on the chip.

NVRAM Operation

The 2004 has a 512 × 8 static RAM array that is backed up, bit for bit, by a non-volatile storage array. (See Figure 1.) The non-volatile array uses Intel's proven FLOTOX technology.

Figure 1. 2004 NVRAM Operational Diagram



READ/WRITE Cycles
Writing data to and reading from the 2004 NVRAM is done in the same manner as with any static RAM. (See Table 1.) Standard microprocessor read and write cycle timing is used. Read/write access time is 200 ns for the 2004-2; the write plus width can be as short as 120 ns. During the read and write cycles the $\overline{NE}$ Non-Volatile Enable input is held high.

Table 1. 2004 Operational Modes

	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{NE}$	Outputs
Standby	V_{IH}	X	X	X	Hi-Z
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data Out
Write	V_{IL}	X	V_{IL}	V_{IH}	Data In
RECALL-Power Up	X	X	X	V_{IH}	Hi-Z
RECALL-Standard	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Hi-Z
STORE	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Hi-Z

RECALL/STORE Operations
Performing a read cycle on the 2004 with $\overline{NE}$ held low initiates a RECALL operation. This operation transfers the data in the non-volatile storage array to the RAM array in less than 10 microseconds. The CPU can perform a RECALL at any time to reload the static RAM array from the non-volatile array. On power-up, RECALL is automatic, allowing immediate access to the NVRAM.

When a write cycle is performed on the 2004 with $\overline{NE}$ held low, a STORE operation is initiated. The STORE operation transfers the data in the RAM array to the non-volatile storage array. Once a STORE operation is started, the 2004 NVRAM on-chip circuitry performs the necessary sequencing to write all of the RAM array data into the non-volatile storage array. The STORE initiation pulse can be as short as 120 nanoseconds. The programming voltage for writing the RAM data into the non-volatile storage cells is generated on-chip. When the STORE operation is started, the 2004's data pins go to a high impedance state, and all control signal inputs are ignored until the operation is completed. Once the STORE operation has been initiated, the CPU can use the system bus for other processing tasks, including the initiation of STORE operations on other NVRAMs. The STORE operation takes 10 milliseconds on the 2004. Data retention for each non-volatile STORE operation is specified for a minimum of ten years.

STORE Operations on 2004 Arrays
In a system with multiple NVRAMs, a STORE operation can be performed on all devices at the same time. In 16-bit systems, this is achieved by doing a STORE initiation cycle on the first NVRAM pair (high/low byte), then doing a STORE initiation on the second pair, and so on. Each STORE initiation cycle is actually a standard system write cycle with $\overline{NE}$ held low. Upon receiving a WRITE pulse, the on-chip circuitry does all the necessary sequencing to write the contents of the RAM array to the on-chip non-volatile storage array. For example, a STORE operation can be started on each 2004 in an array of eight NVRAMs within 10 to 20 microseconds, and 10 milliseconds later 4K bytes of data would be saved in the non-volatile storage arrays of the NVRAMs.

Data Protection
When the power of a system is turned off and the Vcc supply drops below the normal operating range, TTL devices in the system can become unstable. Instability typically occurs when Vcc is below 3.5 volts. In this range, the read and write control signals may become unstable, which can result in an unwanted STORE operation being initiated (during a Vcc power transition). This could occur after the normal power-down STORE operation. A second inadvertent STORE operation could result in incorrect data being stored in the NVRAM's non-volatile array. An unwanted spurious STORE could also be initiated by unstable signals when the system is powering up.

Intel's 2004 NVRAM has on-chip data protection circuitry which prevents spurious STORE operations from occurring by inhibiting the STORE function whenever Vcc is below 4V. Integration of on-chip data protection circuitry enhances data integrity and in general eliminates the need for board level data protection circuits.

NVRAM Applications
The 2004 NVRAM enhances the functions of the MCS-96 in high performance control applications. The NVRAM serves as fast working memory and power-down/power-fail storage of critical system parameters.

In industrial control applications, the NVRAM stores the current position of a robot arm or machine tool. If power fails, the NVRAM guarantees that systems never "lose their place." In instrumentation, such as a gas chromatograph, the NVRAM stores configuration parameters. Non-volatility avoids lengthy re-entry of configuration parameters, delays that might jeopardize sample integrity. Also, configurations can be downloaded in a distributed environment, and the NVRAM can buffer data transmitted to the host.

Within the communications market, the NVRAM stores frequency information in cellular radio applications. High speed modems can use the NVRAM to store configuration parameters entered via the system console or downloaded from a host modem. In data processing systems, peripheral controllers can use the NVRAM to store configuration parameters entered through the console, removing front panel switches. And, error logs can be stored in the NVRAM to improve system maintenance. Finally, in automotive or aircraft applications, the NVRAM can store frequently changed data that must be saved under extreme vibration and temperature conditions.

Generating $\overline{NE}$ ($\overline{NON\text{-}VOLATILE\ ENABLE}$) In A System
There are a number of ways to derive the $\overline{NE}$ signal for the 2004 NVRAM. In MCS-96 systems, the availability of I/O ports on the microcontroller allows simple generation of the

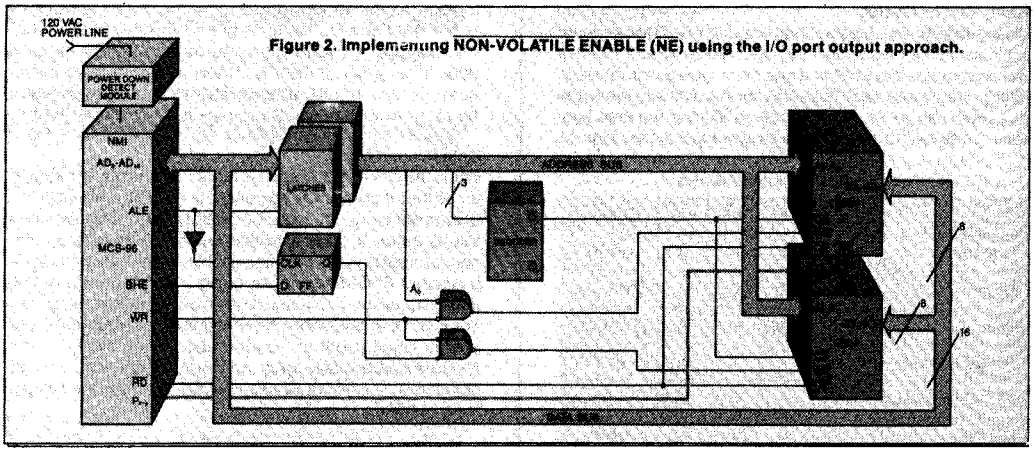


Figure 2. Implementing NON-VOLATILE ENABLE (NE) using the I/O port output approach.

NE signal. To perform a STORE operation, the NE line is brought low via an I/O port. A WRITE cycle is then executed on each 2004 that a STORE operation is to be performed upon. Figure 2 shows the 2004 in an MCS-96 system with NE controlled by an I/O port output. In microcontroller applications where I/O ports are available, this is the preferred approach. Also, in systems with more than two NVRAMs, the I/O port approach uses fewer components, yielding the minimum chip count solution.

Memory Mapped STORE/RECALL

In MCS-96 based systems where all applicable I/O ports are utilized, a memory mapped approach can be used for generating the CE signal (see Figure 3). The concept here is to divide addressable memory space into blocks. One block can be used for normal read/write access to the RAM array, and another for transferring data to and from the non-volatile array. Three address lines are decoded, and the decoder outputs are OR-tied to produce the CE signal. The memory mapping approach is effective in applications that are I/O constrained, and where memory space is not constrained.

Power-Down STORE Implementation

An NVRAM is accessed just like a static RAM memory when the system is powered-up. When system power is removed, whether due to an intended power-down or an unscheduled power loss, a STORE operation is performed to save the data in the non-volatile storage array of the NVRAM.

A store operation can be made to occur automatically in a system by connecting a power-down detection signal to an interrupt input to the CPU. When the signal goes active, the CPU is interrupted, and the software jumps to a short routine which executes a STORE initiation cycle (bring NE low, then do a write cycle to the NVRAM). The Vcc supply to the NVRAM is maintained above 4.75V (Vcc min) for the 10 millisecond duration of the STORE operation.

In a system with more than two NVRAMs, the STORE operations can be done in parallel.

Detecting System Power-Down

A system power-down can be detected in advance in a number of ways. Many commercially available power supplies provide a POWER FAIL signal. There are also power-fail detection "modules" available from several popular power supply manufacturers. An example is the PFM-1 Power Fail Monitor from Power-One, Inc. Both of these methods use a circuit that monitors the 120 VAC power line to determine when power is failing. VAC detection usually gives an earlier indication of an approaching power-down than alternatives that monitor the system's Vcc power supply output. VAC detection is the preferred approach.

120 VAC Input Power-Down Detection Modules

If an AC power-down detection module is used to generate a POWER DOWN signal, the AC input of the module is connected to the 120 VAC line. The output of the module is normally connected to the Non-Maskable Interrupt line of the MCS-96. On some AC power-fail detection modules, the AC level trip point is adjustable. The AC trip point should be set just below the lowest AC level that the system is likely to see under normal operating conditions. The reason for this is to avoid activating the POWER DOWN signal when the AC power line is at the lower end of its operating range. A trip level of 105 VAC is typically used for 120 VAC power lines. In some areas the 120 VAC power line may drop below 105 VAC under normal operating conditions, and the trip point may have to be set correspondingly lower.

Maintaining Vcc During a STORE Operation

After a STORE operation has been initiated, the Vcc supply voltage must be held at or above Vccmin (4.75V) for 10 milliseconds. Switching power supplies generally will hold their output up longer, after the AC input starts falling, than

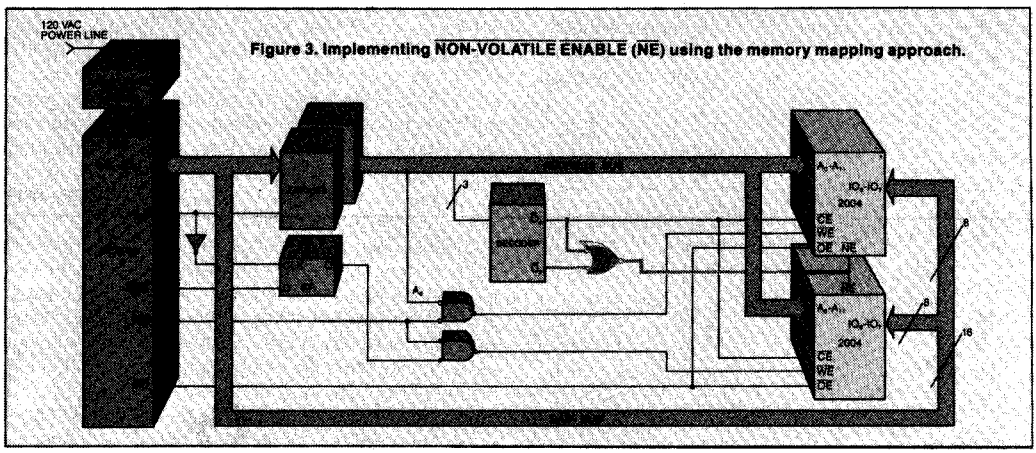


Figure 3. Implementing NON-VOLATILE ENABLE (NE) using the memory mapping approach.

linear power supplies. In addition, power supply manufacturers usually specify hold-up time under full load. Typical hold-up times range from 20 to 30 milliseconds.

If a power supply is used that has no specific Vcc hold-up time, the hold-up time can be measured with a storage oscilloscope. The POWER DOWN signal can be used to trigger the oscilloscope. Vcc should stay above Vccmin for at least 10 milliseconds after the POWER DOWN signal goes active. (Additional hold-up time may be required for systems where a lot of data will be transferred to the NVRAM's RAM array prior to starting the STORE operation.) If a given Vcc power supply cannot hold Vcc up long enough after the POWER DOWN signal, a power supply with a bigger current output rating can be used to maintain VCC for a longer period of time.

MCS-96 Interface

An integrated kit solution including the MCS-96 microcontroller, program memory (in on-chip ROM), and 1K bytes of non-volatile working memory is illustrated in Figure 2. The eight-bit latches demultiplex address bits A0-A7 and A8-A15 from the multiplexed address/data bus. Three higher order addresses are decoded to provide the chip enable ($\overline{CE}$) signal. Non-volatile enable ($\overline{NE}$) is controlled by an I/O port on the MCS-96. For normal read/write access to NVRAM, the I/O port output bit is high. To perform either a STORE or RECALL operation, $\overline{NE}$ is brought low via the output bit. Finally, AO and Byte High Enable ($\overline{BHE}$) are used to select between the upper and lower bytes of an NVRAM.

A power-down STORE operation is initiated automatically when the POWER DOWN signal connected to the Non-Maskable interrupt pin goes active. If there is any data in the MCS-96 internal RAM that is to be saved, such as the register files, the power-down interrupt routine writes the data to the NVRAM. The $\overline{NE}$ input is brought low, and a write cycle to any location is executed to initiate the self-timed STORE operation. The Vcc supply will stay above 4.75V for 10 milliseconds while the STORE operation is completed. After initiating the STORE operation, the MCS-96 can finish any remaining tasks before halting. The following code sequence is an example of a typical power-down STORE interrupt service routine:

```
    PORT [0,1,2] EQU [OEH, OFH,10H]
    STORE - RECALL EQU OFEH, 11111110
    NVRAM          EQU OAOOOH
POWER - DOWN - STORE:
;
;
(Here, code can be included to save MCS-96 RAM data by
writing the data to the 2004. The code below stores that data
in the 2004's non-volatile array.)
ANDB PORTX, STORE RECALL
ST   OOH, NVRAM
:
:
(Vcc is held up for 10 milliseconds. During this time any
remaining system tasks can be performed.)
HALT: BR HALT
```

Summary

This article has discussed the operation of the 2004 NVRAM, and has shown how to design the 2004 into systems that use the state-of-the-art 16-bit MCS-96 microcontroller. The 2004 gives the MCS-96 systems greater capabilities by saving constantly changing data during periods when system power is removed. The 2004 may be interfaced with all Intel 8-bit or 16-bit microprocessors and microcontrollers. By designing with all solid state memory, such as the 2004, the flexibility, user-friendliness, and reliability of any system is increased. □