

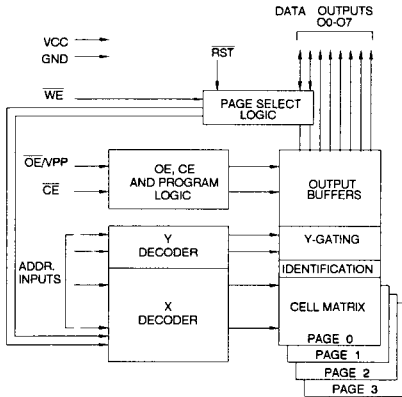
## Features

- Paged Configurations with Page Reset on Power-Up or  $\overline{\text{RST}}$  Signal
- 4 Pages, 16K x 8
- Low Power CMOS Operation
  - 100  $\mu\text{A}$  max. Standby
  - 20 mA max. Active at 5 MHz
- Fast Read Access Time - 120ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC and OTP PLCC
- 5V  $\pm$  10% Supply
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100 $\mu\text{s}$ /byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Military, Commercial and Industrial Temperature Ranges
- Fully Compatible with 27128, 27513, 27011

**512K (4x16Kx8)**  
**UV**  
**Erasable**  
**Paged CMOS**  
**EPROM**

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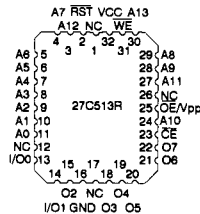
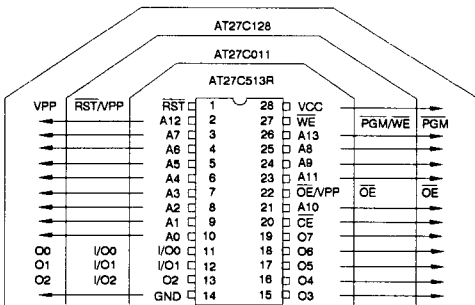
## Block Diagram



Address Pins	Number of Pages	Bits per Page
A0-A13	4	131,072

Pin Name	Function
A0-A13	Addresses
O2-O7	Outputs
I/O0-I/O1	Input/Output
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE/VPP}}$	Output Enable
$\overline{\text{WE}}$	Page Write Enable
RST	Page Reset
NC	No Connect

## Pin Configurations



Note: JEDEC standard pinouts for AT27C011 and AT27C128 are shown for comparison only.

Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.





## Description

The AT27C513R is a low-power, high performance 524,288 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). This device requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 120ns, making this part compatible with high performance microprocessor systems by eliminating the need for speed-reducing WAIT states.

The AT27C513R features page mode addressing. Atmel's 27C513R has 4 pages, each organized 16K x 8, and provides a compatible upgrade for existing 128K EPROM based designs. Increased memory capacity and improved system performance can now be easily retrofitted without using costly additional board space.

The AT27C513R has an automatic page latch clear circuit to ensure consistent page selection during system bootstrapping. The page latches are automatically reset to page 0 upon power-up (resets typically for  $V_{CC} \leq 3.8V$ ) or when RST is brought low ( $V_{IL}$ ).

The AT27C513R meets or exceeds all specifications for the AT27C513. Atmel's 1.2 micron scaled CMOS technology additionally provides lower active power consumption, and significantly faster programming. Power consumption is typically only 8mA in Active Mode and less than 10uA in Standby.

The AT27C513R is available in a choice of industry standard JEDEC-approved packages including; 28-pin DIP in ceramic or one time programmable (OTP) plastic, and 32-pad ceramic leadless chip carrier (LCC) or OTP plastic J-leaded chip carrier (PLCC). All devices feature a two line control

( $\overline{CE}, \overline{OE}$ ) to give designers the flexibility to prevent bus contention.

With a high density 64K byte storage capability, the Atmel 512K EPROMs allow firmware to be stored reliably and to be quickly accessed by the system without the delays of mass storage media.

The AT27C513R has additional features to ensure high quality and efficient production use. The rapid programming algorithm reduces the time required to program the chip and guarantees reliable programming. Programming time is typically 100μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturing origin. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

## Page Selection Data <sup>(1)</sup>

Page Selection	Page D <sub>IN</sub>	
	I/O1	I/O0
Select Page 0	V <sub>IL</sub>	V <sub>IL</sub>
Select Page 1	V <sub>IL</sub>	V <sub>IH</sub>
Select Page 2	V <sub>IH</sub>	V <sub>IL</sub>
Select Page 3	V <sub>IH</sub>	V <sub>IH</sub>

Note: 1. The AT27C513R automatically resets to page 0 whenever  $V_{CC} \leq 3.8V$  (typical conditions).

## Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}/V_{PP}$	$\overline{WE}$	$\overline{RST}$	A <sub>i</sub>	$V_{CC}$ <sup>(3)</sup>	Outputs	I/O <sub>i</sub>
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	A <sub>i</sub>	V <sub>CC</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X <sup>(1)</sup>	V <sub>CC</sub>	High Z	High Z
Standby	V <sub>IH</sub>	X	X	V <sub>IH</sub>	X	V <sub>CC</sub>	High Z	High Z
Rapid Program <sup>(2)</sup>	V <sub>IL</sub>	V <sub>PP</sub>	V <sub>IH</sub>	V <sub>IH</sub>	A <sub>i</sub>	V <sub>CC</sub>	D <sub>IN</sub>	D <sub>IN</sub>
PGM Verify	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	A <sub>i</sub>	V <sub>CC</sub>	D <sub>OUT</sub>	D <sub>OUT</sub>
PGM Inhibit	V <sub>IH</sub>	V <sub>PP</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	V <sub>CC</sub>	High Z	High Z
Page Select	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	$V_{CC}$ <sup>(3)</sup>	High Z	Page D <sub>IN</sub>
Page Reset	X	X	X	V <sub>IL</sub>	X	$V_{CC}$ <sup>(3)</sup>	High Z	High Z
Product Identification <sup>(5)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	A <sub>9</sub> =V <sub>H</sub> <sup>(4)</sup> A <sub>0</sub> =V <sub>IH</sub> or V <sub>IL</sub> A <sub>1</sub> -A <sub>13</sub> =V <sub>IL</sub>	V <sub>CC</sub>	Identification Code	Identification Code

- Notes: 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.  
 2. Refer to Programming characteristics.  
 3. Page 0 is automatically selected at power up ( $V_{CC} < 3.8V$ ).  
 4. V<sub>H</sub> = 12.0 ± 0.5V.

5. Two identifier bytes may be selected. All A<sub>i</sub> inputs are held low (V<sub>IL</sub>), except A<sub>9</sub> which is set to V<sub>H</sub> and A<sub>0</sub> which is toggled low (V<sub>IL</sub>) to select the Manufacturer's Identification byte and high (V<sub>IH</sub>) to select the Device Code byte.

## Absolute Maximum Ratings\*

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
V <sub>PP</sub> Supply Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
Integrated UV Erase Dose.....	7258 w <sub>a</sub> sec/cm <sup>2</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Notes:

1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is V<sub>CC</sub>+0.75V dc which may overshoot to +7.0V for pulses of less than 20ns.

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## D.C. and A.C. Operating Conditions for Read and Page Select Operations

AT27C513R					
		-12	-15	-20	-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V <sub>CC</sub> Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

## D.C. and Operating Characteristics for Read and Page Select Operations

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = -0.1V to V <sub>CC</sub> + 1V		10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = -0.1V to V <sub>CC</sub> + 0.1V		10	μA
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	I <sub>SB1</sub> (CMOS)	Com.	100	μA
		CE = V <sub>CC</sub> - 0.3 to V <sub>CC</sub> + 1.0V	Ind., Mil.	200	μA
		I <sub>SB2</sub> (TTL)	Com.	2	mA
		CE = 2.0 to V <sub>CC</sub> + 1.0V	Ind., Mil.	3	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5MHz, I <sub>OUT</sub> = 0mA, CE = V <sub>IL</sub>	Com.	20	mA
			Ind., Mil.	25	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA		.45	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -100μA		V <sub>CC</sub> - 0.3	V
		I <sub>OH</sub> = -2.5mA		3.5	V
		I <sub>OH</sub> = -400μA		2.4	V
V <sub>CLR</sub>	Page Latch Clear V <sub>CC</sub> Supply Voltage			4.0	V

Notes: 1. V<sub>CC</sub> must be applied simultaneously or before  $\overline{OE}/V_{PP}$ , and removed simultaneously or after  $\overline{OE}/V_{PP}$ .

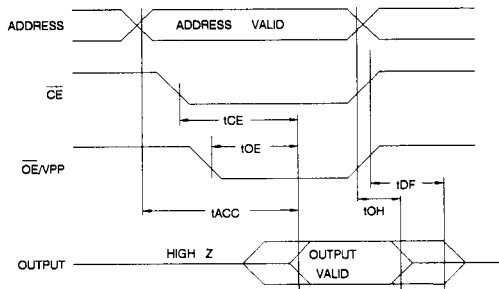




## A.C. Characteristics for Read Operation

			AT27C513R								
			-12		-15		-20		-25		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Units
$t_{ACC}^{(4)}$	Address to Output Delay	$\overline{CE} = \overline{OE}/V_{PP}$ $= V_{IL}$	Com., Ind. Mil.		120	150	200	250	ns		
$t_{CE}^{(3)}$	$\overline{CE}$ to Output Delay	$\overline{OE}/V_{PP} = V_{IL}$	120	150	200	250	ns				
$t_{OE}^{(3,4)}$	$\overline{OE}/V_{PP}$ to Output Delay	$\overline{CE} = V_{IL}$	60	60	75	100	ns				
$t_{DF}^{(2,5)}$	$\overline{OE}/V_{PP}$ or $\overline{CE}$ High to Output Float	$\overline{CE} = V_{IL}$	50	50	55	60	ns				
$t_{OH}$	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ , whichever occurred first	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$	0	0	0	0	ns				

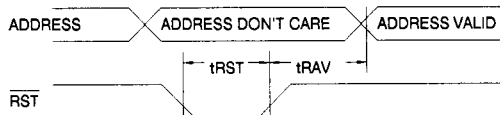
## A.C. Waveforms for Read Operation <sup>(1)</sup>



### Notes:

- Timing measurement references are 0.8V and 2.0V. Input AC driving levels are 0.45V and 2.4V, unless otherwise specified.
- $t_{DF}$  is specified from  $\overline{OE}/V_{PP}$  or  $\overline{CE}$ , whichever occurs first. Output float is defined as the point when data is no longer driven.
- $\overline{OE}/V_{PP}$  may be delayed up to  $t_{CE}-t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
- $\overline{OE}/V_{PP}$  may be delayed up to  $t_{ACC}-t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
- This parameter is only sampled and is not 100% tested.

## A.C. Waveforms for Page Reset Operation



## Pin Capacitance (f = 1MHz T = 25°C) <sup>(1)</sup>

	Typ	Max	Units	Conditions
$C_{IN}$	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

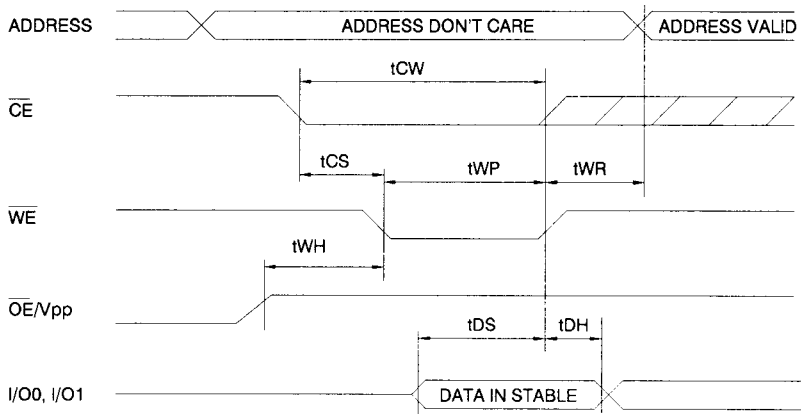
A.C. Characteristics for Page Select and Page Reset Operations

Symbol	Parameter	Condition	AT27C513R								Units
			-12		-15		-20		-25		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>CW</sub> <sup>(1)</sup>	$\overline{CE}$ to End of Write	$\overline{OE}/V_{PP} = V_{IH}$	110		110		145		180		ns
t <sub>WP</sub> <sup>(1)</sup>	Write Pulse Width	$\overline{OE}/V_{PP} = V_{IH}$	60		60		80		100		ns
t <sub>WR</sub> <sup>(3)</sup>	Write Recovery Time		20		20		20		20		ns
t <sub>DS</sub>	Data Setup Time	$\overline{OE}/V_{PP} = V_{IH}$	35		35		45		50		ns
t <sub>DH</sub>	Data Hold Time	$\overline{OE}/V_{PP} = V_{IH}$	20		20		20		20		ns
t <sub>CS</sub>	$\overline{CE}$ to Write Setup Time	$\overline{OE}/V_{PP} = V_{IH}$	0		0		0		0		ns
t <sub>WH</sub> <sup>(2,3)</sup>	$\overline{WE}$ Low from $\overline{OE}/V_{PP}$ High Delay Time		50		50		50		55		ns
t <sub>RST</sub>	Reset Low Time		120		150		200		250		ns
t <sub>RAV</sub>	Reset to Address Valid		120		150		200		250		ns

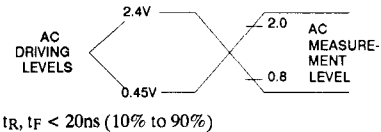
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- Notes: 1. Writing can be terminated by either  $\overline{CE}$  or  $\overline{WE}$  going high after the minimum t<sub>CW</sub> or t<sub>WP</sub> requirements have been met.  
 2.  $\overline{OE}/V_{PP}$  must be at V<sub>IH</sub> during a Page Select.  
 3. This parameter is only sampled and is not 100% tested.

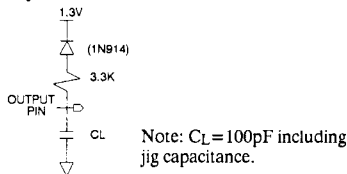
A.C. Waveforms for Page Select Operation



Input Test Waveforms and Measurement Levels



Output Test Load





## D.C. Programming Characteristics

$T_A=25\pm 5^\circ\text{C}$ ,  $V_{CC}=6.5\pm 0.25\text{V}$ ,  $\overline{\text{OE}}/V_{PP}=13.0\pm 0.25\text{V}$

Sym- bol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$I_{LI}$	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		10	$\mu\text{A}$
$V_{IL}$	Input Low Level	(All Inputs)	-0.6	0.8	V
$V_{IH}$	Input High Level		2.0	$V_{CC}+1$	V
$V_{OL}$	Output Low Volt.	$I_{OL} = 2.1\text{mA}$		.45	V
$V_{OH}$	Output High Volt.	$I_{OH} = -400\mu\text{A}$	2.4		V
$I_{CC2}$	$V_{CC}$ Supply Current (Program and Verify)			25	mA
$I_{PP2}$	$\overline{\text{OE}}/V_{PP}$ Current	$\overline{\text{CE}} = V_{IL}$		25	mA
$V_{ID}$	A9 Product Identification Voltage		11.5	12.5	V

### \*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20ns  
 Input Pulse Levels ..... 0.45V to 2.4V  
 Input Timing Reference Level ..... 0.8V to 2.0V  
 Output Timing Reference Level ..... 0.8V to 2.0V

## A.C. Programming Characteristics

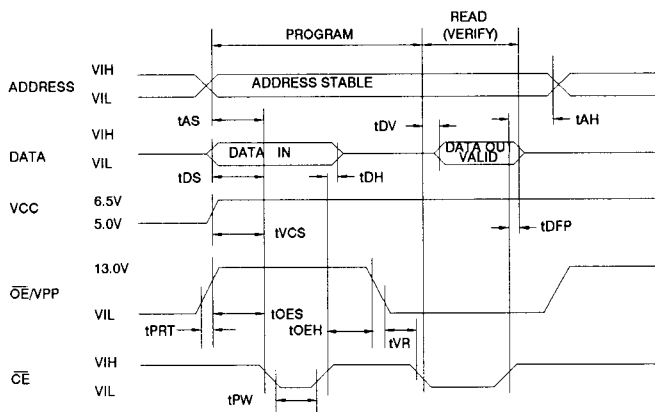
$T_A=25\pm 5^\circ\text{C}$ ,  $V_{CC}=6.5\pm 0.25\text{V}$ ,  $\overline{\text{OE}}/V_{PP}=13.0\pm 0.25\text{V}$

Sym- bol	Parameter	Test Conditions* (see Note 1)	Limits		Units
			Min	Max	
$t_{AS}$	Address Setup Time		2		$\mu\text{s}$
$t_{OES}$	$\overline{\text{OE}}/V_{PP}$ Setup Time		2		$\mu\text{s}$
$t_{OEh}$	$\overline{\text{OE}}/V_{PP}$ Hold Time		2		$\mu\text{s}$
$t_{DS}$	Data Setup Time		2		$\mu\text{s}$
$t_{AH}$	Address Hold Time		0		$\mu\text{s}$
$t_{DH}$	Data Hold Time		2		$\mu\text{s}$
$t_{DFP}$	$\overline{\text{CE}}$ High to Output Float Delay	(Note 2)	0	130	ns
$t_{VCS}$	$V_{CC}$ Setup Time		2		$\mu\text{s}$
$t_{PW}$	$\overline{\text{CE}}$ Program Pulse Width	(Note 3)	95	105	$\mu\text{s}$
$t_{DV}$	Data Valid from $\overline{\text{CE}}$	(Note 2)		1	$\mu\text{s}$
$t_{VR}$	$\overline{\text{OE}}/V_{PP}$ Recovery Time		2		$\mu\text{s}$
$t_{PRT}$	$\overline{\text{OE}}/V_{PP}$ Pulse Rise Time During Programming		50		ns

### Notes:

- $V_{CC}$  must be applied simultaneously or before  $\overline{\text{OE}}/V_{PP}$  and removed simultaneously or after  $\overline{\text{OE}}/V_{PP}$ .
- This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
- Program Pulse width tolerance is  $100\mu\text{sec}\pm 5\%$ .

## Programming Waveforms <sup>(1)</sup>



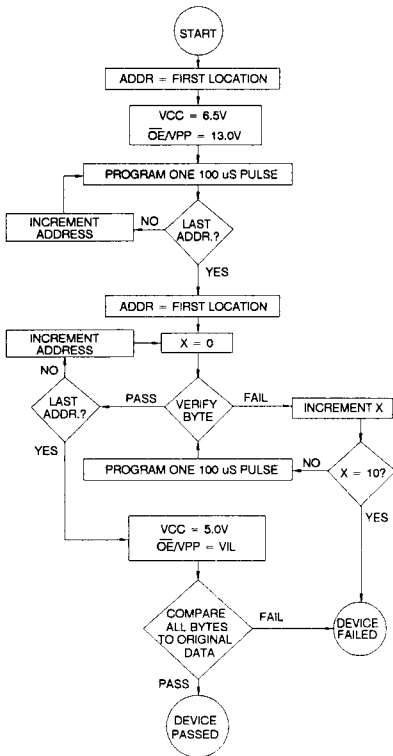
### Notes:

- The Input Timing Reference is 0.8V for  $V_{IL}$  and 2.0V for  $V_{IH}$ .
- $t_{PV}$  and  $t_{DFP}$  are characteristics of the device but must be accommodated by the programmer.
- The proper page to be programmed must be selected by a page select operation prior to programming the AT27C513R.

## Rapid Programming Algorithm <sup>(1)</sup>

A  $100\mu\text{s}$   $\overline{\text{CE}}$  pulse width is used to program. The address is set to the first location.  $V_{\text{CC}}$  is raised to 6.5V and  $\overline{\text{OE}}/V_{\text{PP}}$  is raised to 13.0V. Each address is first programmed with one  $100\mu\text{s}$   $\overline{\text{CE}}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive  $100\mu\text{s}$  pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $\overline{\text{OE}}/V_{\text{PP}}$  is then lowered to  $V_{\text{IL}}$  and  $V_{\text{CC}}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

Note: 1. The proper page to be programmed must be selected by a page select operation prior to programming the AT27C513R.



## Erasure Characteristics

The entire memory array of the AT27C513R is erased (all outputs read as  $V_{\text{OH}}$ ) after exposure to ultraviolet light at a wavelength of  $2537 \text{ \AA}$ . Complete erasure is assured after a minimum of 20 minutes exposure using  $12,000 \mu\text{W}/\text{cm}^2$  intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of  $15\text{W}\cdot\text{sec}/\text{cm}^2$ . To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

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## Identification Code:

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	1	1	0	0E



## Ordering Information

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	20	0.1	AT27C513R-12DC AT27C513R-12LC	28DW6 32LW	Commercial (0°C to 70°C)
120	25	0.2	AT27C513R-12DI AT27C513R-12LI	28DW6 32LW	Industrial (-40°C to 85°C)
150	20	0.1	AT27C513R-15DC AT27C513R-15LC AT27C513R-15PC AT27C513R-15JC AT27C513R-15RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)
150	25	0.2	AT27C513R-15DI AT27C513R-15LI AT27C513R-15PI AT27C513R-15JI AT27C513R-15RI	28DW6 32LW 28P6 32J 28R	Industrial (-40°C to 85°C)
			AT27C513R-15DM AT27C513R-15LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C513R-15DM/883 AT27C513R-15LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	20	0.1	AT27C513R-20DC AT27C513R-20LC AT27C513R-20PC AT27C513R-20JC AT27C513R-20RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)
200	25	0.2	AT27C513R-20DI AT27C513R-20LI AT27C513R-20PI AT27C513R-20JI AT27C513R-20RI	28DW6 32LW 28P6 32J 28R	Industrial (-40°C to 85°C)
			AT27C513R-20DM AT27C513R-20LM	28DW6 32LW	Military (-55°C to 125°C)
			AT27C513R-20DM/883 AT27C513R-20LM/883	28DW6 32LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	20	0.1	AT27C513R-25DC AT27C513R-25LC AT27C513R-25PC AT27C513R-25JC AT27C513R-25RC	28DW6 32LW 28P6 32J 28R	Commercial (0°C to 70°C)

## Ordering Information

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	25	0.2	AT27C513R-25DI	28DW6	Industrial (-40°C to 85°C)
			AT27C513R-25LI	32LW	
			AT27C513R-25PI	28P6	
			AT27C513R-25JI	32J	
			AT27C513R-25RI	28R	
			AT27C513R-25DM	28DW6	Military (-55°C to 125°C)
			AT27C513R-25LM	32LW	
			AT27C513R-25DM/883	28DW6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
			AT27C513R-25LM/883	32LW	

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### Package Type

<b>28DW6</b>	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
<b>32J</b>	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
<b>32LW</b>	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
<b>28P6</b>	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
<b>28R</b>	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

