

## 6805-Series Microprocessors

### General 6805 Family Features

#### Hardware

- 8-bit architecture
- Fully static operation
- Self-check mode in microcomputers
- Master Reset and Power-on Reset
- Single 3-6V power supply
- Power-saving STOP and WAIT modes

#### Software

- Software compatible with entire 6805 family
- 61 instructions and 10 addressing modes
- Indexed addressing for tables
- True bit manipulation
- Memory-mapped I/O
- Efficient use of program space
- Versatile interrupt handling

### Comparison of CMOS CD6805 Family Microprocessors

| Type                     | Memory Add. (Bytes) | On-chip RAM (Bytes) | Max. Clock Freq. (MHz) | Instruc. Time Min./Max. (µs) | Timer/Counter Bits | Prescalers | Bus Structure            | Interrupts | Latched I/O Lines | Maximum Operation Temperature (°C) | Package No. of Pins* |
|--------------------------|---------------------|---------------------|------------------------|------------------------------|--------------------|------------|--------------------------|------------|-------------------|------------------------------------|----------------------|
| CDP6805E2<br>CDP6805E2C# | 8K                  | 112                 | 5.0                    | 2.0/10.00                    | 8                  | Program    | Multiplexed Address Data | V          | 16                | 0 to +70                           | 40D, E<br>44Q        |
| CDP6805E3<br>CDP6805E3C# | 64K                 | 112                 | 5.0                    | 2.0/10.00                    | 8                  | Program    | Multiplexed Address Data | V          | 13                | 0 to +70                           | 40D, E<br>44Q        |

V = Vectored address

# 'C' Version has -40 to +85°C operating temperature range.

\* See interpretation guide and packaging section

## 1800-Series Microprocessors and Microcomputers

### General Features:

- 16 x 16 matrix of registers for use as multiple program counters, data pointers or data registers
- Single-phase clock; optional on-chip crystal-controlled oscillator
- Flexible programmed I/O mode
- Four flag inputs directly tested by branch instructions
- Programmable single-bit output port
- Static circuitry - no minimum clock frequency
- 8-bit parallel organization with bi-directional data bus and multiplexed address bus

| Type                  | Memory Add. (Bytes) | On-chip RAM (Bytes) | On-chip ROM (Bytes) | Max. Clock Freq. (MHz) | Instruc. Time Min./Max. (µs) | Timer/Counter Bits | Pre-scalers | Bus Structure             | Interrupts | Latch I/O | Max. Oper. Temp. (°C) | Pkg No. of Pin*   |
|-----------------------|---------------------|---------------------|---------------------|------------------------|------------------------------|--------------------|-------------|---------------------------|------------|-----------|-----------------------|-------------------|
| CDP1802A<br>CDP1802AC | 64K                 | -                   | -                   | 3.2                    | 5.0/7.5                      | -                  | -           | Multiplexed Address Lines | ✓          | Off-chip  | -55 to +125           | 40D<br>40E<br>40Q |
| CDP1802BC             | 64K                 | -                   | -                   | 5.0                    | 3.2/4.8                      | -                  | -           | Multiplexed Address Lines | ✓          | Off-chip  | -55 to +125           | 40D<br>40E<br>40Q |
| CDP1804AC             | 64K                 | 64                  | 2K                  | 5.0                    | 3.2/16.0                     | 8                  | +32         | Multiplexed Address Lines | ✓          | Off-chip  | -55 to +125           | 40D<br>40E        |
| CDP1805AC             | 64K                 | 64                  | -                   | 5.0                    | 3.2/16.8                     | 8                  | +32         | Multiplexed Address Lines | ✓          | Off-chip  | -55 to +125           | 40D<br>40E<br>40Q |
| CDP1806AC             | 64K                 | -                   | -                   | 5.0                    | 3.2/16.0                     | 8                  | +32         | Multiplexed Address Lines | ✓          | Off-chip  | -55 to +125           | 40D<br>40E<br>40Q |

\* See interpretation guide and packaging section