STANDARD MICROSYSTEMS CORPORATION

COM 7210

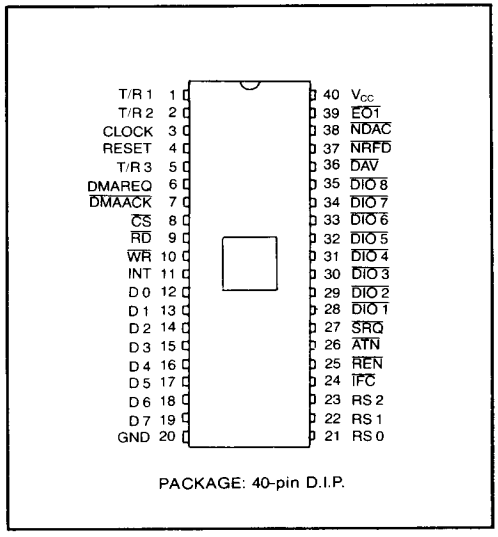
SECTION III

Intelligent GPIB Interface Controller

FEATURES

- ☐ All Functional Interface Capability Meeting IEEE Standard 488-1978
  - —SH1 (Source Handshake)
  - —AH1 (Acceptor Handshake)
  - —T5 or TE5 (Talker or Extended Talker)
  - —L3 or LE3 (Listener or Extended Listener)
  - —SR1 (Service Request)
  - —RL1 (Remote Local)
  - —PP1 or PP2 (Parallel Poll) (Remote or Local Configuration)
  - —DC1 (Device Clear)
  - —DT1 (Device Trigger)
  - —C1-5 ((Controller) (All Functions))
- ☐ Programmable Data Transfer Rate
- ☐ 16 MPU Accessible Registers—8 Read/8 Write
- ☐ 2 Address Registers
  - —Detection of MTA, MLA, MSA (My Talk/Listen/Secondary Address)
  - —2 Device Addresses
- ☐ EOS Message Automatic Detection
- ☐ Command (IEEE Standard 488-78) Automatic Processing and Undefined Command Read Capability
- ☐ DMA Capability
- ☐ Programmable Bus Transceiver I/O Specification (Works with T.I./Motorola/Intel)
- ☐ 1 to 8 MHz Clock Range
- ☐ TTL Compatible

PIN CONFIGURATION

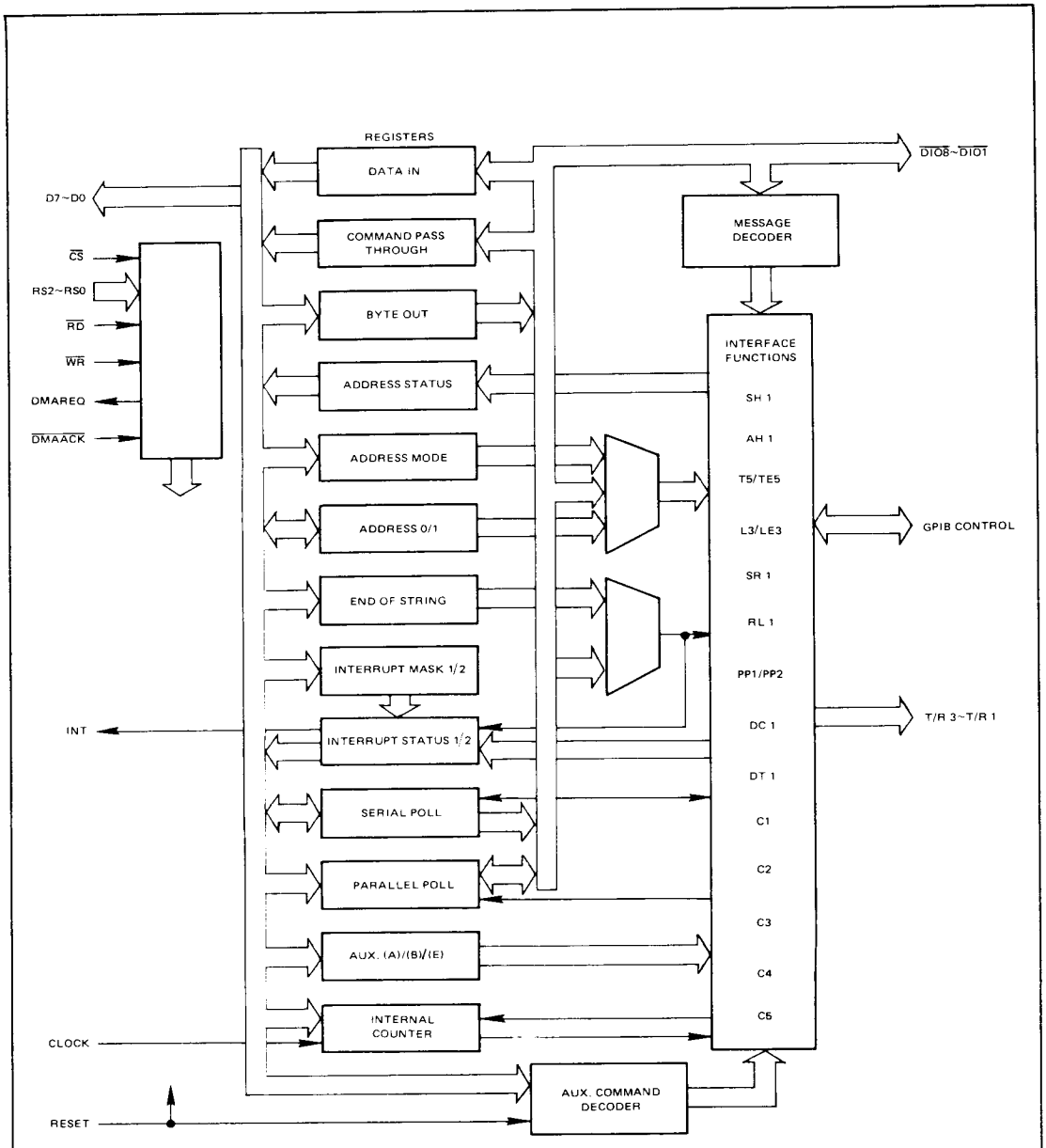


PACKAGE: 40-pin D.I.P.

- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ +5V Single Power Supply
- ☐ 40-Pin DIP
- ☐ 8080/85/86 Compatible

GENERAL DESCRIPTION

The COM7210 TLC is an intelligent GPIB Interface Controller designed to meet all of the functional requirements for Talkers, Listeners, and Controllers as specified by the IEEE Standard 488-1978. Connected between a processor bus and the GPIB, the TLC provides high level management of the GPIB to unburden the processor and to simplify both hardware and software design. Fully compatible with most processor architectures, Bus Driver/Receivers are the only additional components required to implement any type of GPIB interface.



BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN	SYMBOL	I/O	DESCRIPTION
1	T/R1	O	Transmit/Receive Control—Input/Output Control Signal for the GPIB Bus Transceivers.
2	T/R2	O	Transmit/Receive Control—The functions of T/R2, T/R3 are determined by the values of TRM1, TRM0 of the address mode register.
3	CLK	I	Clock—(1-8 MHz) Reference Clock for generating the state change prohibit times T1, T6, T7, T9 specified in IEEE Standard 488-1978.
4	RST	I	Reset—Resets 7210 to an idle state when high (active high).
5	T/R3	O	Transmit/Receive Control—Function determined by TRM1 and TRM0 of address mode register (See T/R2).
6	DMAREQ	O	DMA Request—7210 requests data transfer to the computer system. becomes low on input of DMA acknowledge signal DACK.
7	$\overline{DMAACK}$	I	DMA Acknowledge—(Active Low) Signal connects the computer system data bus to the data register of the 7210.
8	$\overline{CS}$	I	Chip Select—(Active Low) Enables access to the register selected by RS0-2 (read or write operation).
9	$\overline{RD}$	I	Read—(Active Low) Places contents of read register specified by RS0-2—on D0-7 (Computer Bus).
10	$\overline{WR}$	I	Write—(Active Low) writes data on D0-7 into the write register specified by RS0-2.
11	INT / $\overline{INT}$	O	Interrupt Request—(Active High/Low) Becomes active due to any 1 of 13 internal interrupt factors (unmasked) active state software configurable, active high on chip reset.
12-19	D0-7	I/O	Data Bus—8-bit bidirectional data bus, for interface to computer system.
20	GND		Ground.
21-23	RS0-2	I	Register Select—These lines select one of eight read (write) registers during a read (write) operation.
24	$\overline{IFC}$	I/O	Interface Clear—Control line used for clearing the interface functions.
25	$\overline{REN}$	I/O	Remote Enable—Control line used to select remote or local control of the devices.
26	$\overline{ATN}$	I/O	Attention—Control line which indicates whether data on DIO lines is an interface message or device dependent message.
27	$\overline{SRQ}$	I/O	Service Request—Control line used to request the controller for service.
28-35	$\overline{DIO1\text{-}8}$	I/O	Data Input/Output—8-bit bidirectional bus for transfer of message on the GPIB.
36	$\overline{DAV}$	I/O	Data Valid—Handshake line indicating that data on DIO lines is valid.
37	$\overline{NRFD}$	I/O	Ready for Data—Handshake line indicating that device is ready for data.
38	$\overline{NDAC}$	I/O	Data Accepted—Handshake line indicating completion of message reception.
39	$\overline{EOI}$	I/O	End or Identify—Control line used to indicate the end of multiple byte transfer sequence or to execute a parallel polling in conjunction with ATN.
40	V_{CC}		+5V DC

FUNCTIONAL DESCRIPTION

Introduction

The IEEE Standard 488 describes a "Standard Digital Interface for Programmable Instrumentation" which, since its introduction in 1975, has become the most popular means of interconnecting instruments and controllers in laboratory, automatic test and even industrial applications. Refined over several years, the 488-1978 Standard, also known as the General Purpose Interface Bus (GPIB), is a highly sophisticated standard providing a high degree of flexibility to meet virtually most all instrumentation requirements. The COM7210 TLC implements all of the functions that are required to interface to the GPIB. While it is beyond the scope of this document to provide a complete explanation of the IEEE 488 Standard, a basic description follows:

The GPIB interconnects up to 15 devices over a common set of data control lines. Three types of devices are defined by the standard: Talkers, Listeners, and Controllers, although some devices may combine functions such as Talker/Listener or Talker/Controller.

Data on the GPIB is transferred in a bit parallel, byte serial fashion over 8 Data I/O lines (D101-D108). A 3 wire handshake is used to ensure synchronization of transmission and reception. In order to permit more than one device to receive data at the same time, these control lines are "Open Collector" so that the slowest device controls the data rate. A number of other control lines perform a variety of functions such as device addressing, interrupt generation, etc.

The COM7210 TLC implements all functional aspects of Talker, Listener and Controller functions as defined by the 488-1978 Standard, and on a single chip.

The COM7210 TLC is an intelligent controller designed to provide high level protocol management of the GPIB, freeing the host processor for other tasks. Control of the TLC is accomplished via 16 internal registers. Data may be transferred either under program control or via DMA using the TLC's DMA control facilities to further reduce processor

overhead. The processor interface of the TLC is general in nature and may be readily interfaced to most processor lines.

In addition to providing all control and data lines necessary for a complete GPIB implementation, the TLC also provides a unique set of bus transceiver controls permitting the use of a variety of different transceiver configurations for maximum flexibility.

Internal Registers

The TLC has 16 registers, 8 of which are read and 8 write.

REGISTER NAME	ADDRESSING						SPECIFICATION							
	RS2	RS1	RS0	$\overline{WR}$	$\overline{RD}$	$\overline{CS}$								
Data In (0R)	0	0	0	1	0	0	D17	D16	D15	D14	D13	D12	D11	D10
Interrupt Status 1 (1R)	0	0	1	1	0	0	CPT	APT	DET	END	DEC	ERR	D0	D1
Interrupt Status 2 (2R)	0	1	0	1	0	0	INT	SRQ1	LOK	REM	CO	LOKC	REMC	ADSC
Serial Poll Status (3R)	0	1	1	1	0	0	S8	PEND	S6	S5	S4	S3	S2	S1
Address Status (4R)	1	0	0	1	0	0	CIC	ATN	SPMS	LPAS	TPAS	LA	TA	MJMN
Command Pass Through (5R)	1	0	1	1	0	0	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0
Address 0 (6R)	1	1	0	1	0	0	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
Address 1 (7R)	1	1	1	1	0	0	EO1	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
Byte Out (0W)	0	0	0	0	1	0	BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0
Interrupt Mask 1 (1W)	0	0	1	0	1	0	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Mask 2 (2W)	0	1	0	0	1	0	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC
Serial Poll Mode (3W)	0	1	1	0	1	0	S8	rsv	S6	S5	S4	S3	S2	S1
Address Mode (4W)	1	0	0	0	1	0	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0
Auxiliary Mode (5W)	1	0	1	0	1	0	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0
Address 0/1 (6W)	1	1	0	0	1	0	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
End of String (7W)	1	1	1	0	1	0	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Data Registers

The data registers are used for data and command transfers between the GPIB and the microcomputer system.

DATA IN (0R)	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Holds data sent from the GPIB to the computer

BYTE OUT (0W)	BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0

Holds information written into it for transfer to the GPIB

Interrupt Registers

The interrupt registers are composed of interrupt status bits, interrupt mask bits, and some other noninterrupt related bits.

READ

INTERRUPT STATUS 1 (1R).	CPT	APT	DET	END	DEC	ERR	DO	DI

INTERRUPT STATUS 2 (2R)	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC

WRITE

INTERRUPT MASK 1 (1W)	CPT	APT	DET	END	DEC	ERR	DO	DI

INTERRUPT MASK 2 (2W)	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC

Interrupt Status Bits

INT	OR of All Unmasked Interrupt Status Bits
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger
END	End (END or EOS Message Received)
DEC	Device Clear
ERR	Error
DO	Data Out
DI	Data In
SRQI	Service Request Input
LOKC	Lockout Change
REMC	Remote Change
ADSC	Address Status Change
CO	Command Output

There are thirteen factors which can generate an interrupt from the COM7210, each with their own status bit and mask bit.

The interrupt status bits are always set to one if the interrupt condition is met. The interrupt mask bits decide whether the INT bit and the interrupt pin will be active for that condition.

Noninterrupt Related Bits

LOK	Lockout
REM	Remote/Local
DMAO	Enable/Disable DMA Out
DMAI	Enable/Disable DMA In

Serial Poll Registers

READ

SERIAL POLL STATUS (3R)	S8	PEND	S6	S5	S4	S3	S1	S0

WRITE

SERIAL POLL MODE (3W)	S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll Mode register holds the STB (status byte: S8, S6-S1) sent over the GPIB and the local message rsv (request service). The Serial Poll Mode register may be read through the Serial Poll Status register. The PEND is set by rsv = 1, and cleared by NPRS • $\overline{rsv}$ = 1 (NPRS = Negative Poll Response State).

Address Mode/Status Registers

ADDRESS STATUS (4R)	CIC	$\overline{ATN}$	SPMS	LPAS	TPAS	LA	TA	MJMN
ADDRESS MODE (4W)	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0

The Address Mode register selects the address mode of the device and also sets the mode for T/R3 and T/R2 the transceiver control lines.

The functions of T/R2, T/R3 terminals (2 and 5) are determined as below by the TRM1, TRM0 values of the address mode register.

T/R2	T/R3	TRM1	TRM0
EOIOE	TRIG	0	0
CIC	TRIG	0	1
CIC	EOIOE	1	0
CIC	PE	1	1

EOIOE = TACS + SPAS + CIC • $\overline{CSBS}$

This denotes the input/output of $\overline{EOI}$ terminal.

When "1": Output
When "0": Input

CIC = $\overline{CIDS + CADS}$

This denotes if the controller interface function is active or not.

When "1": $\overline{ATN}$ = output, $\overline{SRQ}$ = input
When "0": $\overline{ATN}$ = input, $\overline{SRQ}$ = output

PE = CIC + $\overline{PPAS}$

This indicates the type of bus driver connected to DI08 to DI01 and DAV lines.

When "1": 3 state type
When "0": Open collector type

TRIG: When DTAS state is initiated or when a trigger auxiliary command is issued, a high pulse is generated.

Upon RESET, TRM0 and TRM1 become "0" (TRM0 = TRM1 = 0) and local message port is provided, so that T/R2 and T/R3 both become "LOW."

Address Modes

ton	lon	ADM1	ADM0	ADDRESS MODE	CONTENTS OF ADDRESS (0) REGISTER	CONTENTS OF ADDRESS (1) REGISTER
1	0	0	0	Talk only mode	Address Identification Not Necessary (No controller on the GPIB)	
0	1	0	0	Listen only mode	Not Used	
0	0	0	1	Address mode 1 (A1)	Major talk address or Major listen address	Minor talk address or Minor listen address
0	0	1	0	Address mode 2 (A2)	Primary address (talk or listen)	Secondary address (talk or listen)
0	0	1	1	Address mode 3 (A3)	Primary address (major talk or major listen)	Primary address (minor talk or minor listen)
Combinations other than above indicated Prohibited.						

Notes: (A1) —Either MTA or MLA reception is indicated by coincidence of either address with the received address. Interface function T or L.

(A2) —Address register 0 = primary, Address register 1 = secondary, interface function TE or LE.

(A3) —CPU must read secondary address via Command Pass Through Register interface function (TE or LE).

Address Status Bits

$\overline{ATN}$	Data Transfer Cycle (device in CSBS)
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
CIC	Controller Active
LA	Listener Addressed
TA	Talker Addressed
MJMN	Sets minor T/L address Reset = Major T/L address
SPMS	Serial Poll Mode State

Address Registers

ADDRESS 0 (6R)	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
ADDRESS 1 (7R)	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
ADDRESS 0/1 (6W)	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

The TLC is able to automatically detect two types of addresses which are held in address registers 0 and 1. The addressing modes are outlined below.

Address settings are made by writing into the address 0/1 register. The function of each bit is described below.

Address 0/1 Register Bit Selections

ARS —Selects which address register, 0 or 1
DT —Permits or Prohibits address to be detected as Talk
DL —Permits or Prohibits address to be detected as Listen
AD5-AD1 —Device address value
EOI —Holds the value of EOI line when data is received

Command Pass Through Register

COMMAND PASS THROUGH (5R)	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CP1	CPT0

The CPT register is used such that the CPU may read the DIO lines in the cases of undefined command, secondary address, or parallel poll response.

End of String Register

END OF STRING (7W)	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

This register holds either a 7- or 8-bit EOS message byte used in the GPIB system to detect the end of a data block. Aux Mode Register A controls the specific use of this register.

Auxiliary Mode Register

AUXILIARY MODE (5W)	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

This is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits.

CNT 2 1 0	COM 4 3 2 1 0	OPERATION
0 0 0	C_4 C_3 C_2 C_1 C_0	Issues an auxiliary command specified by C_4 to C_0.
0 0 1	0 F_3 F_2 F_1 F_0	The reference clock frequency is specified and T_1, T_6, T_7, T_9 are determined as a result.
0 1 1	U S P_3 P_2 P_1	Makes write operation to the parallel poll register.
1 0 0	A_4 A_3 A_2 A_1 A_0	Makes write operation to the aux. (A) register.
1 0 1	B_4 B_3 B_2 B_1 B_0	Makes write operation to the aux. (B) register.
1 1 0	0 0 0 E_1 E_0	Makes write operation to the aux. (E) register.

Auxiliary Commands 0 0 0 C_4 C_3 C_2 C_1 C_0

COM 43210		
00000	iepon	— Immediate Execute pon—Generate local pon Message
00010	crst	— Chip Reset—Same as External Reset
00011	rrfd	— Release RFD
00100	trig	— Trigger
00101	rtl	— Return to Local Message Generation
00110	seoi	— Send EOI Message
00111	nvid	— Non Valid (OSA reception)—Release DAC Holdoff
01111	vid	— Valid (MSA reception, CPT, DEC, DET)—Release DAC Holdoff
0X001	sppf	— Set/Reset Parallel Poll Flag
10000	gts	— Go To Standby
10001	tca	— Take Control Asynchronously
10010	tcs	— Take Control Synchronously
11010	tcse	— Take Control Synchronously on End
10011	ltn	— Listen
11011	ltnc	— Listen with Continuous Mode
11100	lun	— Local Unlisten
11101	epp	— Execute Parallel Poll
1X110	sifc	— Set/Reset IFC
1X111	sren	— Set/Reset REN
10100	dsc	— Disable System Control

Internal Counter 0 0 1 0 F_3 F_2 F_1 F_0

The internal counter generates the state change prohibit times (T_1, T_6, T_7, T_9) specified in the IEEE std 488-1978 with reference to the clock frequency.

Auxiliary A Register 1 0 0 A_4 A_3 A_2 A_1 A_0

Of the 5 bits that may be specified as part of its access word, 2 bits control the GPIB data receiving modes of the 7210 and 3 bits control how the EOS message is used.

A_1	A_0	DATA RECEIVING MODE
0	0	Normal Handshake Mode
0	1	RFD Holdoff on all Data Modes
1	0	RFD Holdoff on End Mode
1	1	Continuous Mode

BIT NAME			FUNCTION
A_2	0	Prohibit	Permits (prohibits) the setting of the END bit by reception of the EOS message.
	1	Permit	
A_3	0	Prohibit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message TACS.
	1	Permit	
A_4	0	7 bit EOS	Makes the 8 bits/7 bits of EOS register the valid EOS message.
	1	8 bit EOS	

Auxiliary B Register 1 0 1 B_4 B_3 B_2 B_1 B_0

The Auxiliary B Register is much like the A Register in that it controls the special operating features of the device.

BIT NAME			FUNCTION
B_0	1	Permit	Permits (prohibits) the detection of undefined command. In other words, it permits (prohibits) the setting of the CPT bit on reception of an undefined command.
	0	Prohibit	
B_1	1	Permit	Permits (prohibits) the transmission of the END message when in serial poll active state (SPAS).
	0	Prohibit	
B_2	1	T_1 (high-speed)	T_1 (high speed) as T_1 of handshake after transmission of 2nd byte following data transmission.
	0	T_1 (low-speed)	
B_3	1	$\overline{INT}$	Specifies the active level of $\overline{INT}$ pin.
	0	INT	
B_4	1	ist = SRQS	SRQS indicates the value of ist level local message (the value of the parallel poll flag is ignored). SRQS = 1...ist = 1. SRQS = 0...ist = 0.
	0	ist = Parallel Poll Flag	The value of the parallel poll flag is taken as the ist local message.

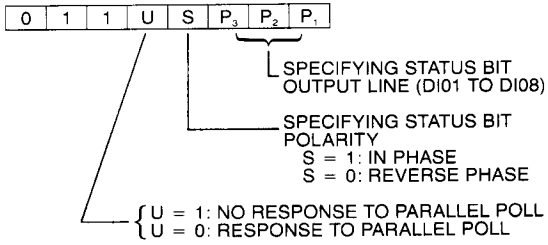
Auxiliary E Register 1 1 0 0 0 0 E_1 E_0

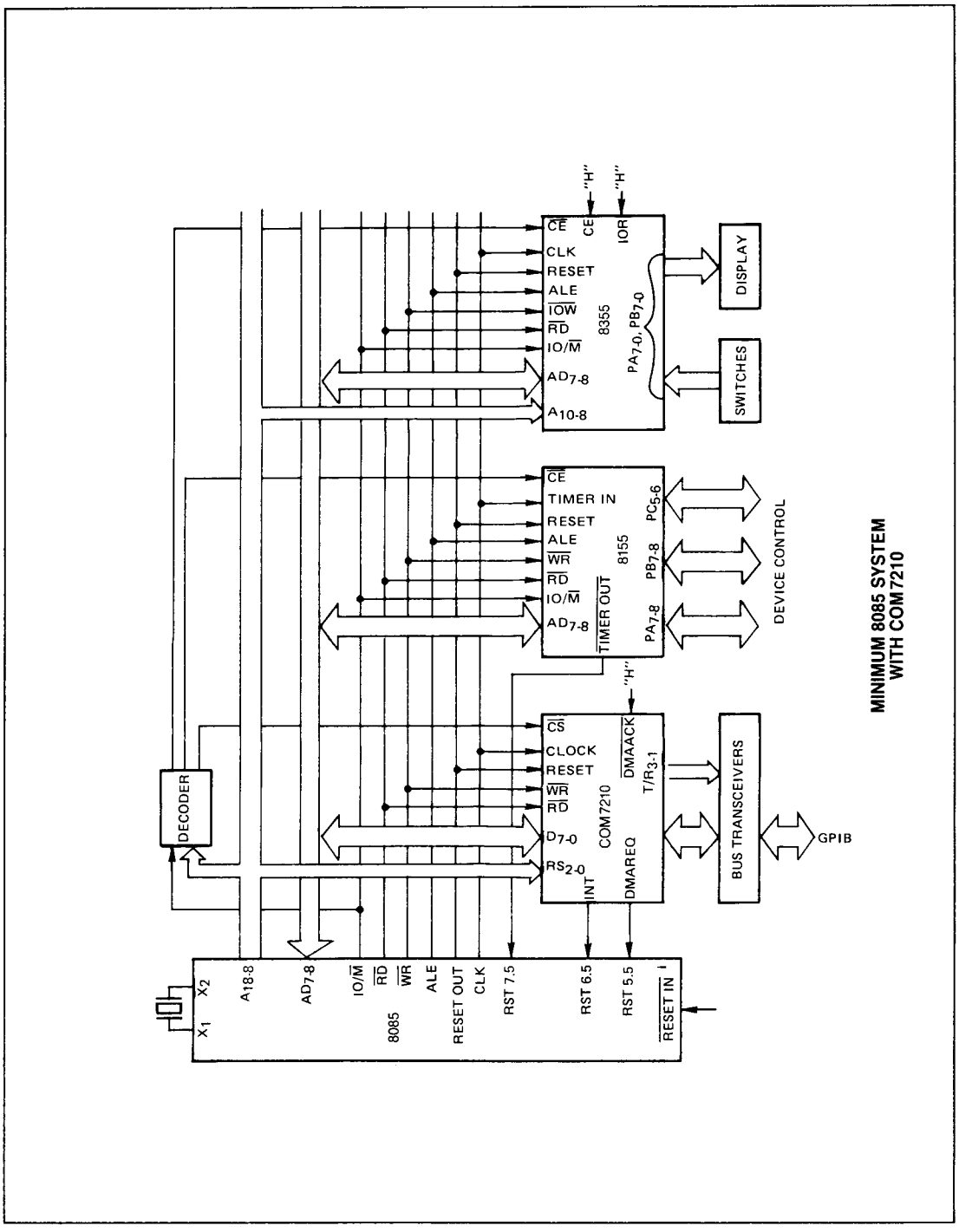
This register controls the Data Acceptance Modes of the TLC.

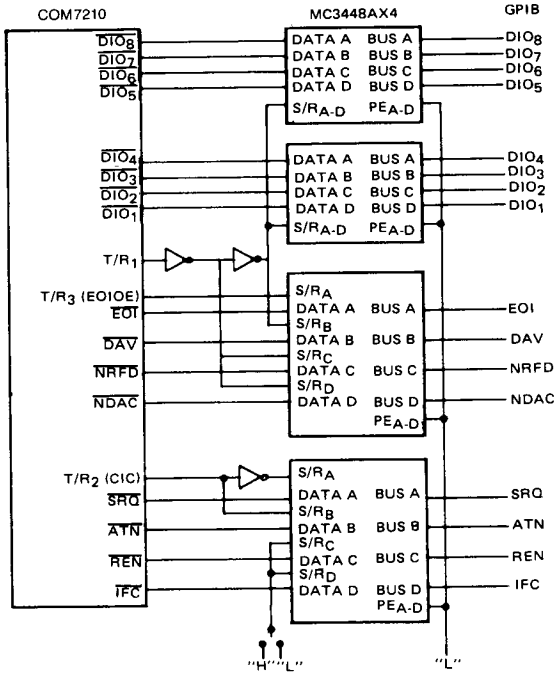
BIT			FUNCTION
E_0	1	Enable	DAC Holdoff by initiation of DCAS
	0	Disable	
E_1	1	Enable	DAC Holdoff by initiation of DTAS
	0	Disable	

Parallel Poll Register

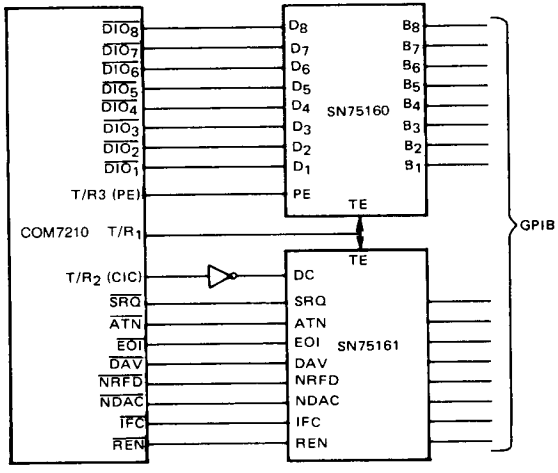
The Parallel Poll Register defines the parallel poll response of the COM7210.







Note: In this example, high-speed data transfer cannot be made since the bus transceiver is of the open collector type (Set $B_2 = 0$).



Note: In the case of low-speed data transfer ($B_2 = 0$), the T/R_3 pin can be used as a TRIG output. The PE input of SN75160 should be cleared to "0."

MINIMUM 8085 SYSTEM WITH COM7210 (CONT.)

ELECTRICAL CHARACTERISTICS

MAXIMUM GUARANTEED RATINGS (T_a = 25°C)

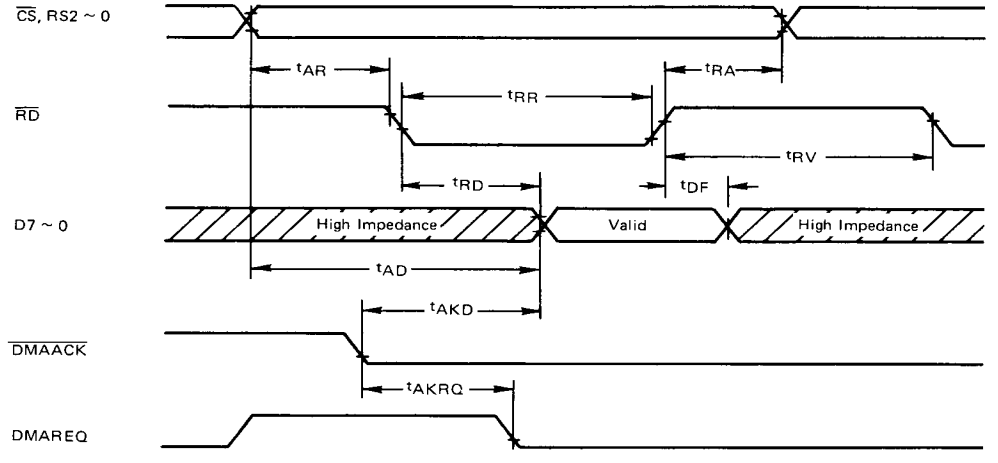
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	−0.5 ~ +7.0	V
Input Voltage	V_I	−0.5 ~ +7.0	V
Output Voltage	V_O	−0.5 ~ +7.0	V
Operating Temperature	T_{opt}	0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +125	°C

DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Input High Voltage	V_{IH}	+2.0		V_{CC} + 0.5	V	
Low Level Output Voltage	V_{OL}			+0.45	V	I_{OL} = 2 mA (4 mA: T/R1 Pin)
High Level Output Voltage	V_{OH1}	+2.4			V	I_{OH} = −400 μA (Except INT)
High Level Output Voltage (INT Pin)	V_{OH2}	+2.4 +3.5			V	I_{OH} = −400 μA I_{OH} = −50 μA
Input Leakage Current	I_{IL}	−10		+10	μA	V_{IN} = 0V ~ V_{CC}
Output Leakage Current	I_{OL}	−10		+10	μA	V_{OUT} = 0.45V ~ V_{CC}
Supply Current	I_{CC}			+180	mA	

CAPACITANCE (T_a = 25°C, V_{CC} = GND = 0V)

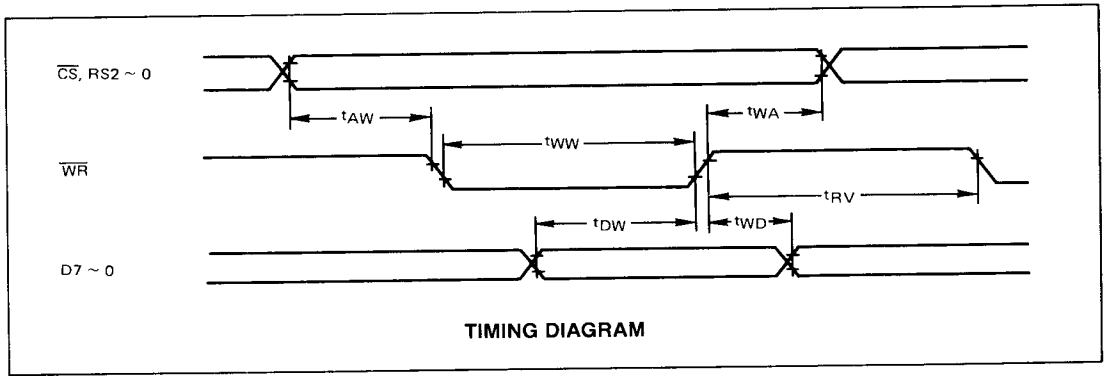
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground
I/O Capacitance	$C_{I/O}$			20	pF	



TIMING DIAGRAM

AC CHARACTERISTICS, (T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	CONDITIONS
$\overline{EOI}$ ↓ → $\overline{DIO}$	t_{EOD1}		250	ns	PPSS → PPAS, ATN = True
$\overline{EOI}$ ↓ → T/$\overline{R1}$ ↑	t_{EOT11}		155	ns	PPSS → PPAS, ATN = True
$\overline{EOI}$ ↑ → T/$\overline{R1}$↓	t_{EOT12}		200	ns	PPAS → PPSS, ATN = False
$\overline{ATN}$ ↓ → $\overline{NDAC}$ ↓	t_{ATND}		155	ns	AIDS → ANRS, LIDS
$\overline{ATN}$ ↓ → T/$\overline{R1}$ ↓	t_{ATT1}		155	ns	TACS + SPAS → TADS, CIDS
$\overline{ATN}$ ↓ → T/R2 ↓	t_{ATT2}		200	ns	TACS + SPAS → TADS, CIDS
$\overline{DAV}$ ↓ → DMAREQ	t_{DVRQ}		600	ns	ACRS → ACDS, LACS
$\overline{DAV}$ ↓ → $\overline{NFRD}$ ↓	t_{DVNR1}		350	ns	ACRS → ACDS
$\overline{DAV}$ ↓ → $\overline{NDAC}$ ↑	t_{DVND1}		650	ns	ACRS → ACDS → AWNS
$\overline{DAV}$ ↑ → $\overline{NDAC}$ ↓	t_{DVND2}		350	ns	AWNS → ANRS
$\overline{DAV}$ ↑ → $\overline{DRFD}$ ↑	t_{DVNR2}		350	ns	AWNS → ANRS → ACRS
$\overline{RD}$ ↓ → $\overline{NRFD}$ ↑	t_{RNR}		500	ns	ANRS → ACRS LACS, DI reg. selected
$\overline{NDAC}$ ↑ → DMAREQ ↑	t_{NDRQ}		400	ns	STRS → SWNS → SGNS, TACS
$\overline{NDAC}$ ↑ → $\overline{DAV}$ ↑	t_{NDDV}		350	ns	STRS → SWNS → SGNS
$\overline{WR}$ ↑ → $\overline{DIO}$	t_{WDI}		250	ns	SGNS → SDYS, BO reg. selected
$\overline{NRFD}$ ↑ → $\overline{DAV}$ ↓	t_{NRDV}		350	ns	SDYS → STRS, T_1 = True
$\overline{WR}$ ↑ → $\overline{DAV}$ ↓	t_{WDV}		830 + t_{SYNC}	ns	SGNS → SDYS → STRS BO reg. selected, RFD = True N_c = fc = 8 MHz, T_1 (High Speed)
TRIG Pulse Width	t_{TRIG}	50		ns	
Address Setup to $\overline{RD}$	t_{AR}	85		ns	RS0 ~ RS2
		0		ns	$\overline{CS}$
Address Hold from $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	170		ns	
Data Delay from Address	t_{AD}		250	ns	
Data Delay from $\overline{RD}$ ↓	t_{RD}		150	ns	
Output Float Delay from $\overline{RD}$ ↑	t_{DF}	0	80	ns	
$\overline{RD}$ Recovery Time	t_{RV}	250		ns	
Address Setup to $\overline{WR}$	t_{AW}	0		ns	
Address Hold from $\overline{WR}$	t_{WA}	0		ns	
$\overline{WR}$ Pulse Width	t_{WW}	170		ns	
Data Setup to $\overline{WR}$	t_{DW}	150		ns	
Data Hold from $\overline{WR}$	t_{WD}	0		ns	
$\overline{WR}$ Recovery Time	t_{RV}	250		ns	
DMAREQ ↓ Delay from $\overline{DMAACK}$	t_{AKRQ}		130	ns	
Data Delay from $\overline{DMAACK}$	t_{AKD}		200	ns	



TIMING DIAGRAM

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