CYPRESS SEMICONDUCTOR

Ultra High Speed State Machine EPLD

Features

- **High speed: 125 MHz conditional state control sequence generation**
  - **— Multiple, concurrent processes**
  - **— Multiway branch or join**
  - **— Full input field decode**
- **32 synchronous macrocells**
- **Skew-controlled, OR output array**
  - **— Outputs are sum of states like PLA**
  - **— 3 ns skew**
- **Metastable hardened input registers**
  - **— 10 year MTBF metastable**
  - **— Configurable as 0, 1 or 2 stages**
  - **— Clock enables on all input registers**
- **8 to 12 inputs, 10 to 14 outputs, 1 clock**
- **Programmable clock doubler and conditioner**
  - **— 'Squares up' input clock**
- **Security fuse**
- **Space saving 28 pin slim-line DIP package; also available in 28 pin PLCC**
- **Low power "L" versions**
  - **— 150 mA max at 125 MHz**
- **UV-erasable and reprogrammable**
- **Programming and operation 100% testable**

Product Characteristics

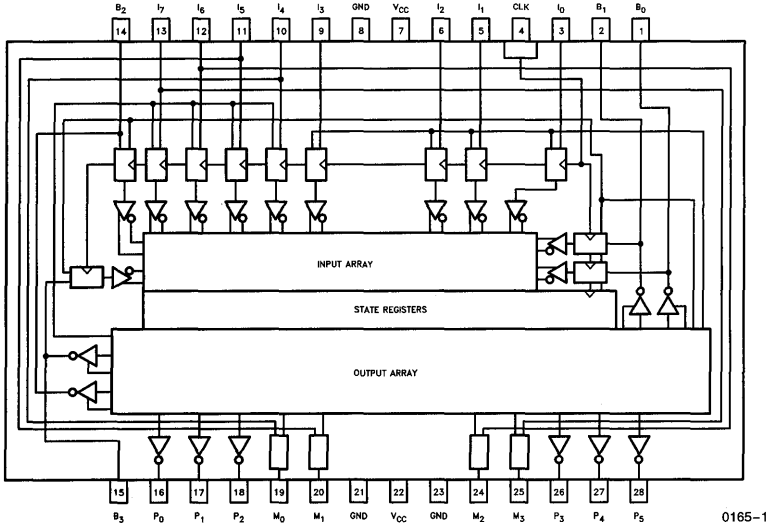
The CY7C361 is a CMOS erasable, programmable logic device (EPLD) with very high speed sequencing and arbitration capabilities.

Applications include: cache and I/O subsystem control for high speed microprocessor based systems, control of high speed numeric processors, and control of asynchronous systems including dataflow organizations.

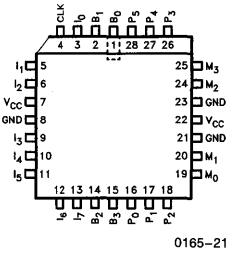
An onboard clock doubler and conditioning circuit allows the device to operate at 125 MHz based on a 62.5 MHz input reference. The same circuit guards against asymmetric clock waveforms and thus allows for the use of a clock with an imperfect duty cycle. The CY7C361 has two arrays which serve in function similar to the arrays in a PLA except that the registers are placed between the two arrays and the long feedback path of the PLA is eliminated.

4

Block Diagram



LCC, PLCC and HLCC Pinout



Selection Guide

Generic Part Number	I_{CC} mA at f_{MAX}				f_{MAX} MHz		t_{IS} ns		t_{CO} ns	
	Com	Com "L"	Mil	Mil "L"	Com	Mil	Com	Mil	Com	Mil
CY7C361-125	200	150			125.0		2		15	
CY7C361-100	200	150	200	150	100.0	100.0	3	3	19	19
CY7C361-83		150		150	83.3	83.3	5	5	23	23
CY7C361-66		150		150	66.6	66.6	5	5	25	25

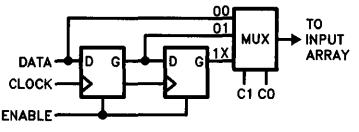
Product Characteristics (Continued)

In the CY7C361, the state information is contained in 32 macrocells sandwiched between the input and output arrays. The current state information is fed back in time to keep up with the 125 MHz operating frequency.

The output array performs an OR function over the state macrocell outputs. The signals from the output array are connected to 14 outputs; in addition they are connected to 3 groups of input macrocells to act as clock enables.

Input Macrocells

The CY7C361 has 12 input macrocells. Each macrocell can be configured to have 0, 1 or 2 registers in the path of the input data. In the configuration where there is no input register, the setup time requirement is largest. In the single register configuration, the setup time is less than half. The double register configuration is used for asynchronous inputs.



0165-3

Figure 1. Input Macrocell

Input Register Enables

The input macrocells are divided into 3 groups, each of which has a register clock enable signal coming from the output array. The purpose of the enable signal is to allow the inputs to be sampled at times controlled by the state of the device.

There is one enable signal per group of input macrocells. The assignment of enable signal node numbers to input macrocell groups is as follows:

Input Nodes	Enable Node
3, 5, 6, 9	29
10,11,12,13	30
1, 2, 14, 15	31

When the enable node is true, data is clocked into the registers of the input macrocells on the rising edge of the internal global clock.

Metastable Immunity

A high level of metastable immunity is afforded in the double register configuration. The CY7C361 input registers are of fast CMOS and resolve inputs in a minimal amount of time. With all inputs switching at the maximum frequency, one metastable event capable of violating the setup time window of the second input register occurs every 10 years. The probability of failure for the configured state machine is much lower than this calculation suggests, because there are more registers in the device and thus more decision time is allowed. No state machine failures due to metastable phenomena will be observed if the maximum frequency and double register operating mode are used.

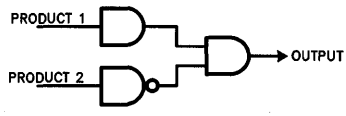
The CY7C361 is thus a superior device for constructing state machines requiring arbitration.

Input Array

The input array has 41 condition decoders: one global reset decoder, 8 local reset decoders, and 32 macrocell decoders. The array has 44 true/complement inputs or 88 inputs in total; for speed reasons, the feedback signals are folded.

Folding or partitioning of the feedback part of the array reduces the number of inputs per decoder to 56. Because of the way the feedback signals are used, this array reduction has minimal impact on utility.

The CY7C361 condition decoder is shown in *Figure 2*. In a conventional PLA or PAL device, only PRODUCT 1 would be present in the first array and the output and feedback would be encoded by a second programmable or fixed OR array. The speed of state machines made from these conventional devices is limited mainly by the feedback path.

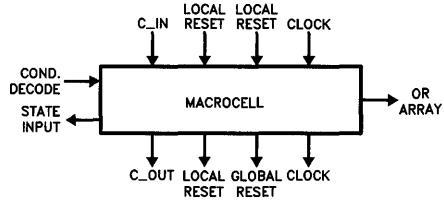


0165-4

Figure 2. Condition Decoder

The condition decoder of the CY7C361 forms a product of a product and a sum over the input field. Since there is immediate feedback information in the input field, multiway fork and join operations can be performed using this type of condition decoder. State transitions can be made in half the time because there is no "state encoding" delay.

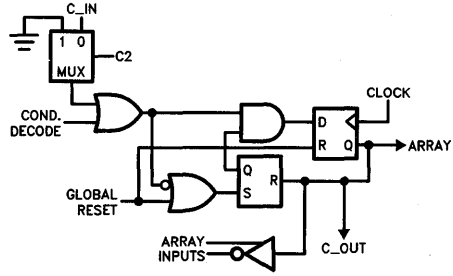
State Machine Macrocells



0165-5

Figure 3. CY7C361 Macrocell

The CY7C361 has 32 state macrocells. The state macrocells each have a single condition decode and share a common clock and global reset condition. For each 4 macrocell group there is a local reset condition.



C1,C0 = 0,1: START

0165-6

Figure 4. Start Configuration

Product Characteristics (Continued)

There are 3 macrocell configurations, named START, TERMINATE and TOGGLE. The purpose of the START configuration is to create a "token" based on a condition decode. The purpose of the TERMINATE configuration is to capture a token and maintain it until a particular condition is decoded, then terminate the token. The TOGGLE configuration is used to make counters.

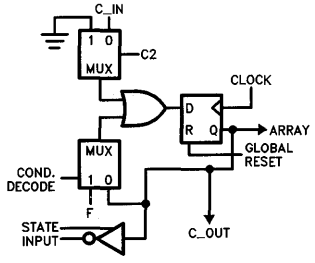
The start configuration creates a token at the leading edge of the condition decode or C_IN. The token is represented by a true output on the macrocell register going to the output array and back as feedback to the input array. The CY7C361 consists of multiple machines or processes running concurrently, each with zero, one or more tokens active at a given time. As the output field is independent, the programmed pattern in the two arrays is one to one translatable to microcode. The microcode is concurrent in operation.

In addition to the main register going to the array, there is an R-S latch in the feedback path. The purpose of the R-S latch is to convert the input condition to a pulse.

In operation, the start macrocell starts from a reset condition (array input = FALSE). When a condition decode "fires" or a token carries in (C_IN), the register output (Q going to array) goes true for exactly one cycle. The OR of the condition decode and the C_IN signal must go FALSE before the start configuration can "fire" again.

Configuration bit C2 is used in all state macrocells to select C_IN to be active (C2 = 0) or inactive (C2 = 1).

For the topmost macrocell (N32), the C2 bit is used to specify a reset option. If the bit is '0', then for the cycle immediately following a reset, the C_IN for this macrocell will be true. At all other times, or if the C2 bit is '1', the C_IN signal will remain false. Note that this option facilitates efficient startup of state machines.



0165-7

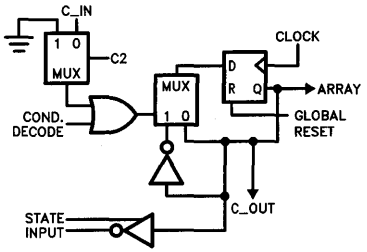
C0,C1 = 1,0: TERMINATE

Figure 5. Terminate Configuration

Figure 5 shows the terminate configuration which is used to maintain state tokens until a condition occurs.

In operation, the terminate configuration "captures" a token via C_IN and the OR gate. The condition decode is normally false or 0 so the token circulates and the register stays set. When the condition decode "fires", the register resets.

The third configuration, TOGGLE, is for counting and signalling. If the condition decode or the C_IN signal is true, then the register will toggle. The TOGGLE configuration is intended to make counters and state machines with simple control requirements.



0165-8

C0,C1 = 11: TOGGLE

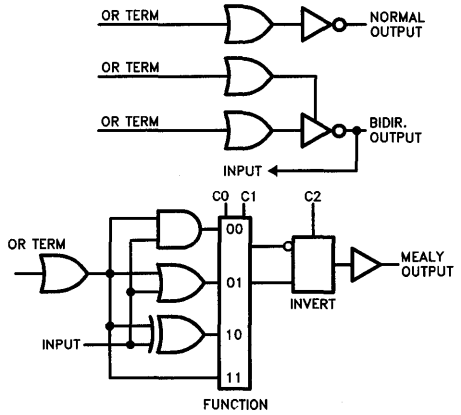
Figure 6. Toggle Configuration

There is one local reset signal for each group of 4 macrocells. The local reset condition decoders will only work with TOGGLE configurations.

The Output Section

There are 3 types of outputs: normal, bidirectional and Mealy. All 3 types can function as normal outputs, but two types—the bidirectional type and the Mealy type—can be used for other purposes. The bidirectional type can be used as an input and the Mealy type can be used as a fast combinational output.

The different types of output structures are shown in *Figure 7.* Note that the only output type that has configuration information to be programmed is the Mealy type.



0165-9

Figure 7. Output Types

A normal output signal from the device is a boolean sum of a subset of the macrocell outputs. The subset selection is programmed into the output array. The number of state machines in the device, and the output mappings of each are determined by the user. The architecture is thus "horizontally divisible" and offers advantages in coding efficiency and event response time over the non-divisible architectures found in most PLA and sequencer types.

A normal output pin is low asserted. The output gate performs an OR function over the flip-flop outputs of the state macrocells. The OR function includes only the outputs which are programmably connected to the OR line in the output array. When none of the connected state macrocell flip-flops are in the true or set condition, the output is high.

Product Characteristics (Continued)

If any connected macrocell flip-flop is asserted (or true) then the OR gate function is true and the output pin is low.

Forcing a false condition is easily accomplished by not connecting any state macrocells to the OR line. To force a true condition, line 33 (labelled V_{CC}) is included in the output array. Any OR line connected to line 33 will be permanently true which will cause a normal output to be low.

The bidirectional outputs are I/O pins which may be used as either inputs or outputs. Under state machine control, these pins may be tristated and used as inputs or outputs depending on how the OE term is programmed.

Each bidirectional output has an OE or output enable control and an associated input path to the first array. The OE control is an OR term from the output array which enables the output when the OR function is true. Thus, an OE which has its OR term connected to line 33 will turn the output on permanently.

The Mealy outputs are designed to implement the fastest possible path between an input to the device and an output. Functions are available which combine the OR term and an input signal. These functions, XOR, AND, and OR, with true or negated assertion levels, are useful for data strobes and semaphore operations where signalling occurs depending on the state, but independent of a signal transition.

The AND and OR functions can be used to gate data strobe signals by the state. The XOR function can be used to implement 2 cycle signalling, which is used in self-timed systems to minimize signalling delays. If these functions are not needed, then the Mealy outputs can be configured as normal outputs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (DIP Pins 7 or 22 to Pins 8, 21 or 23) ... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..... −0.5V to +7.0V

DC Voltage Applied to Outputs During Programming ..... 0.0V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Programming Voltage 13.0V

Output Current into Outputs (Low) ..... 8 mA

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015.2)

Latchup Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Level	Guaranteed HIGH Input, All Inputs[1]		2.2		V
V_{IL}	Input LOW Level	Guaranteed LOW Input, All Inputs[1]			0.8	V
I_{IX}	Input Leakage Current	V_{SS} < V_{IN} < V_{CC}, V_{CC} = Max.		−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{SS} < V_{OUT} < V_{CC}		−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]		−30	−110	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open, Operating at f = f_{MAX}	Commercial "L"		150	mA
			Military "L"			
			Commercial		200	mA
			Military			

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

AC Test Loads and Waveforms

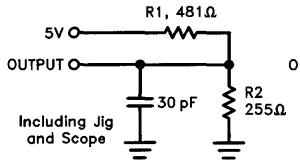


Figure 8a

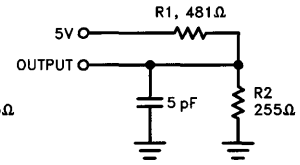
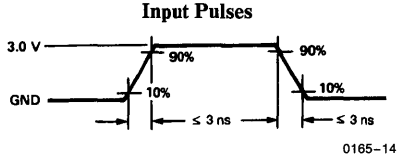


Figure 8b

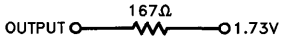
0165–13



0165–14

Figure 9

Equivalent to: THÉVENIN EQUIVALENT



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Switching Characteristics[7]

Parameters	Description	Commercial								Military						Units
		-125		-100		-83		-66		-100		-83		-66		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}[13]	Input to Mealy Output Delay	2	9	2	11	2	12	2	15	2	11	2	13	2	15	ns
t_{PD2}[14]	Input to Mealy Output Delay	2	8	2	10	2	11	2	14	2	10	2	12	2	14	ns
t_{CO1}[3, 13]	Clock to Output Delay	5	15	5	19	5	23	5	25	5	19	5	23	5	25	ns
t_{CO2}[3, 14]	Clock to Output Delay	5	14	5	18	5	22	5	24	5	18	5	22	5	24	ns
t_{CM1}[3, 13]	Clock to Mealy Output Delay	5	17	5	20	5	25	5	28	5	21	5	25	5	28	ns
t_{CM2}[3, 14]	Clock to Mealy Output Delay	5	16	5	19	5	24	5	27	5	20	5	24	5	27	ns
t_{IS}[3]	Input Register Input Set Up Time	2		3		5		5		3		5		5		ns
t_{IH}[3]	Input Register Input Hold Time	3		4		5		5		4		5		5		ns
t_{S}[3, 4]	State Register Input Set Up Time	7		9		12		14		9		12		14		ns
t_{H}[3, 4]	State Register Input Hold Time	0		0		0		0		0		0		0		ns
t_{WH}[6]	Input Clock Pulse Width HIGH	6		7		9		11		7		9		11		ns
t_{WL}[6]	Input Clock Pulse Width LOW	6		7		9		11		7		9		11		ns
t_{SO1}[3, 11]	Output Skew		4		5		6		6		5		6		6	ns
t_{SO2}[3, 12]	Output Skew		3		4		5		5		4		5		5	ns
t_{SM1}[3, 15]	Mealy Output Skew		4		5		6		6		5		6		6	ns
t_{SM2}[3, 16]	Mealy Output Skew		3		4		5		5		4		5		5	ns
f_{MAX}[5]	Output Maximum Frequency	125.0		100.0		83.3		66.6		100.0		83.3		66.6		MHz
t_{CER}[3, 7]	Clock to Output Disable Delay		16		20		22		25		20		22		25	ns
t_{CEA}[3, 8, 9]	Clock to Output Enable Delay		16		20		22		25		20		22		25	ns

Notes:

3. Minimum clock pulse width 8 ns Commercial, 10 ns Military for measurement. Periodically sampled.
4. Input register bypassed.
5. Input clock frequency is $\frac{1}{2}$ f_{MAX} when clock doubler is used.
6. The clock input is tested to accommodate a 60/40 duty cycle waveform at the maximum frequency.
7. Output reference point on AC measurements is 1.5V, except as noted in *Figure 12*:
   $t_{CER(-)}$ negative going is measured at V_{OH} −0.5V.
   $t_{CER(+)}$ positive going is measured at V_{OL} + 0.5V.
8. R1 is disconnected for $t_{CEA(+)}$ positive going (open circuited). (See *Figures 8a* and *8b*).
9. R2 is disconnected for $t_{CEA(-)}$ negative going (open circuited). (See *Figures 8a* and *8b*).
10. *Figure 8a* test load is used for all parameters except t_{CEA} and t_{CER}. *Figure 8b* test load is used for t_{CEA} and t_{CER}.
11. This parameter specifies the maximum allowable t_{CO} clock to output delay difference, or skew, between any two outputs triggered by the same clock edge with all other device outputs changing state within the same clock cycle.
12. This parameter specifies the maximum allowable t_{CO} clock to output delay difference, or skew, between any two outputs triggered by the same clock edge with only the two device outputs changing state within the same clock cycle.
13. This specification is guaranteed for the worst case programmed pattern for which all device outputs are changing state on a given access or clock cycle.
14. This specification is guaranteed for two or fewer outputs changing state in a given access or clock cycle.
15. This parameter specifies the maximum allowable t_{PD} difference between any two mealy outputs triggered by the same or simultaneous input signals with all other device outputs changing state within the same access or clock cycle.
16. This parameter specifies the maximum allowable t_{PD} difference between any two mealy outputs triggered by the same or simultaneous input signals with only the two device outputs changing state within the given access cycle.

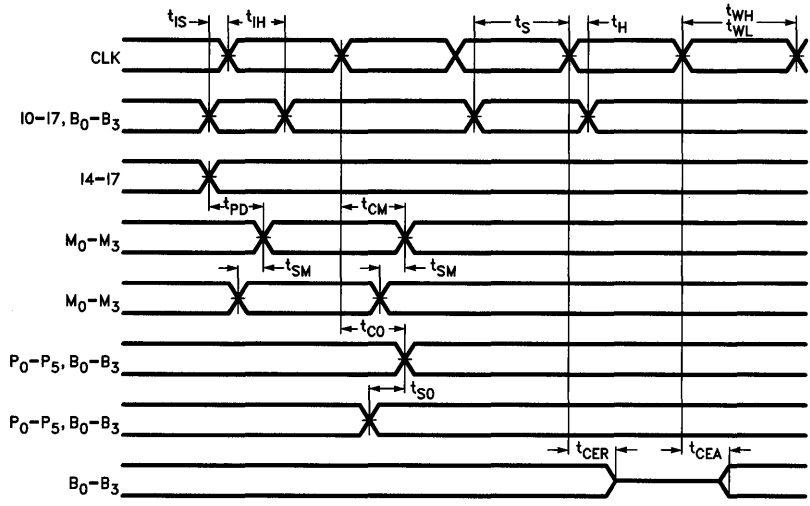


Figure 10. AC Timing Waveforms

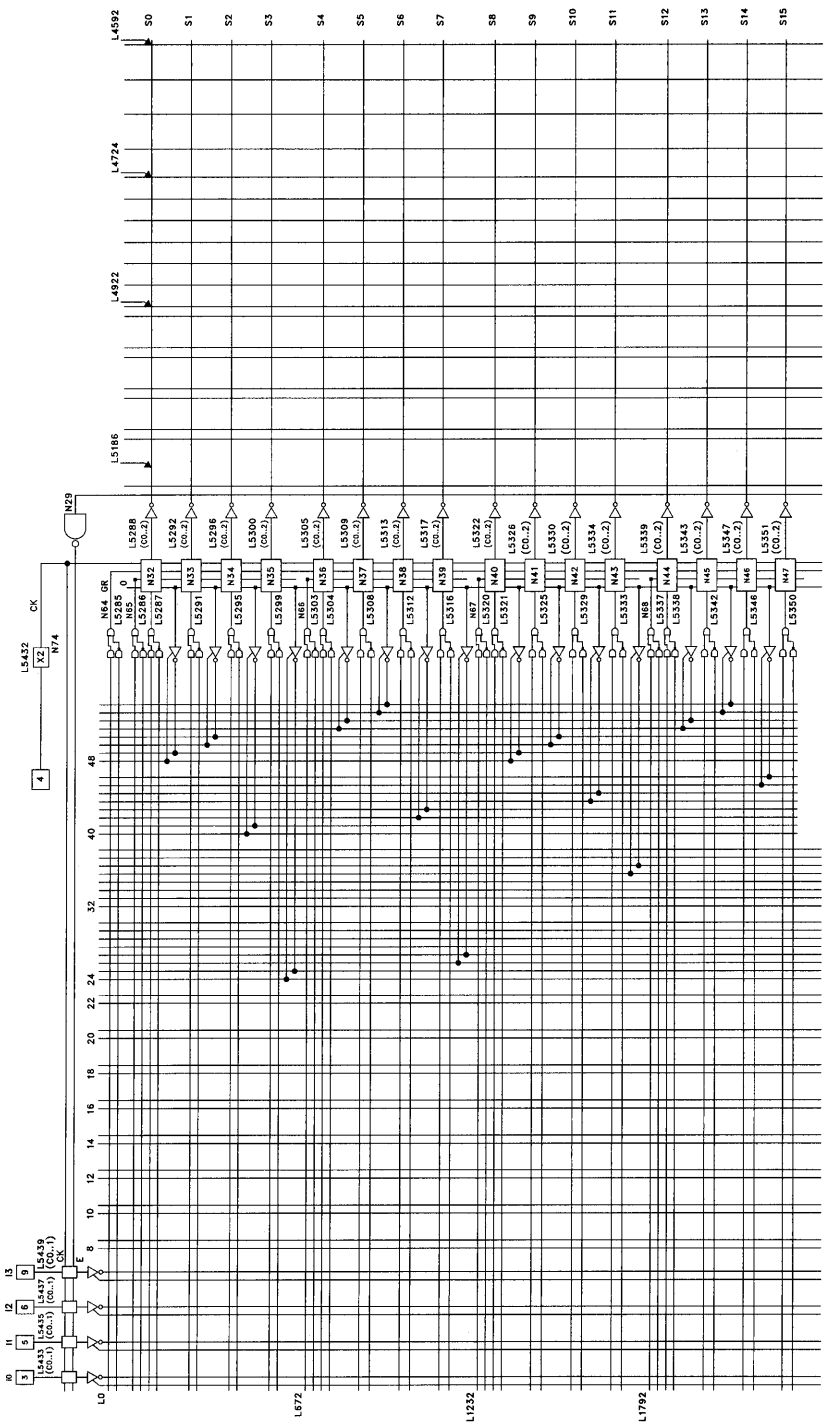
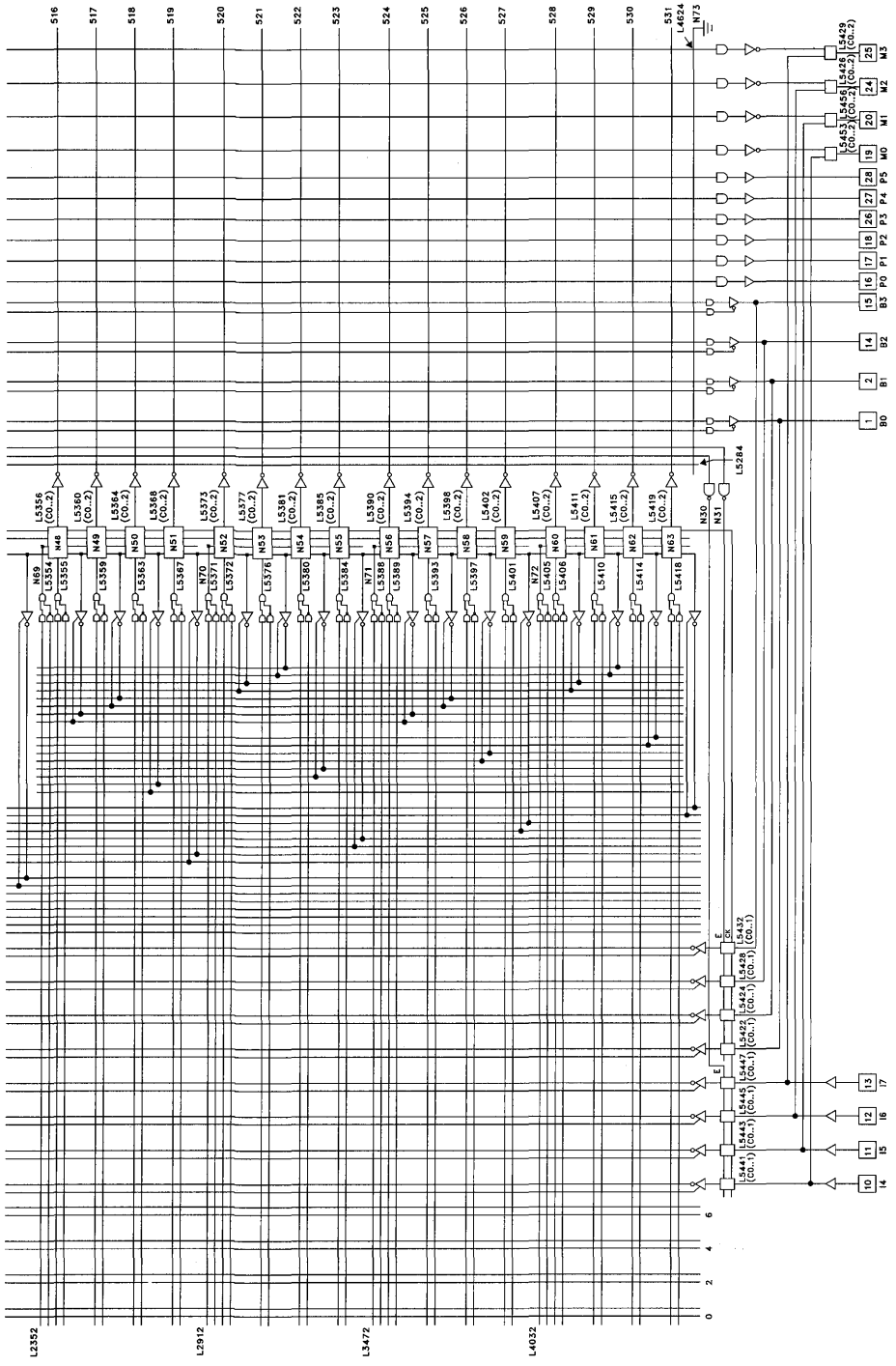


Figure 11a. CY7C361 Block Diagram (Upper Half)



0165-11

Figure 11b. CY7C361 Block Diagram (Lower Half)

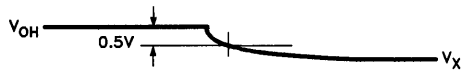
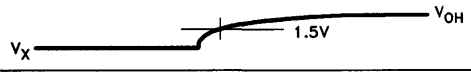
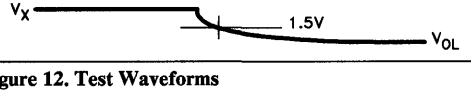
Parameters	V_X	Output Waveform—Measurement Level
$t_{CER}(-)$	0.0V	
$t_{CER}(+)$	2.6V	
$t_{CEA}(+)$	0.0V	
$t_{CEA}(-)$	2.6V	

Figure 12. Test Waveforms

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Ordering Information

I_{CC} mA	f_{MAX} MHz	Ordering Code	Package Type	Operating Range
200	125.0	CY7C361-125PC	P21	Commercial
		CY7C361-125WC	W22	
		CY7C361-125JC	J64	
		CY7C361-125HC	H64	
150	125.0	CY7C361L-125PC	P21	Commercial
		CY7C361L-125WC	W22	
		CY7C361L-125JC	J64	
		CY7C361L-125HC	H64	
200	100.0	CY7C361-100PC	P21	Commercial
		CY7C361-100WC	W22	
		CY7C361-100JC	J64	
		CY7C361-100HC	H64	
150	100.0	CY7C361L-100PC	P21	Commercial
		CY7C361L-100WC	W22	
		CY7C361L-100JC	J64	
		CY7C361L-100HC	H64	
200	100.0	CY7C361-100WMB	W22	Military
		CY7C361-100DMB	D22	
		CY7C361-100QMB	Q64	
		CY7C361-100LMB	L64	
		CY7C361-100HMB	H64	
150	100.0	CY7C361L-100WMB	W22	Military
		CY7C361L-100DMB	D22	
		CY7C361L-100QMB	Q64	
		CY7C361L-100LMB	L64	
		CY7C361L-100HMB	H64	
150	83.3	CY7C361L-83PC	P21	Commercial
		CY7C361L-83WC	W22	
		CY7C361L-83JC	J64	
		CY7C361L-83HC	H64	
150	83.3	CY7C361L-83WMB	W22	Military
		CY7C361L-83DMB	D22	
		CY7C361L-83QMB	Q64	
		CY7C361L-83LMB	L64	
		CY7C361L-83HMB	H64	
150	66.6	CY7C361L-66PC	P21	Commercial
		CY7C361L-66WC	W22	
		CY7C361L-66JC	J64	
		CY7C361L-66HC	H64	
150	66.6	CY7C361L-66WMB	W22	Military
		CY7C361L-66DMB	D22	
		CY7C361L-66QMB	Q64	
		CY7C361L-66LMB	L64	
		CY7C361L-6HMB	H64	

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