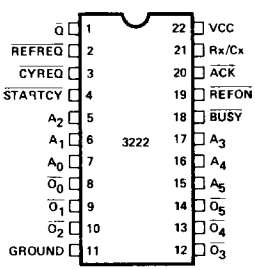
3222
REFRESH CONTROLLER FOR 4K DYNAMIC RANDOM ACCESS MEMORIES

- **Ideal for use in 2107A, 2107C Systems**
- **Simplifies System Design**
- **Reduces Package Count**
- **Standard 22-Pin DIP**
- **Adjustable Refresh Timing Oscillator**
- **6-Bit Address Multiplexer**
- **6-Bit Refresh Address Counter**
- **Refresh Cycle Controller**

The Intel® 3222 is a refresh controller for dynamic RAMs requiring refresh of up to 6 input addresses (or 4K bits for 64 x 64 organization). The device contains an accurate refresh timer (whose frequency can be set by an external resistor and capacitor), plus all necessary control and I/O circuitry to provide for the refresh requirements of dynamic RAMs. The chip's high performance makes it especially suitable for use with high speed N-channel RAMs like the Intel® 2107C. The 3222 is well suited for asynchronous dynamic memory systems.

The 3222 operates from a single +5 volt power supply and is specified for operation over a 0°C to 75°C ambient temperature range. It is fabricated by means of Intel's highly reliable Schottky bipolar process.

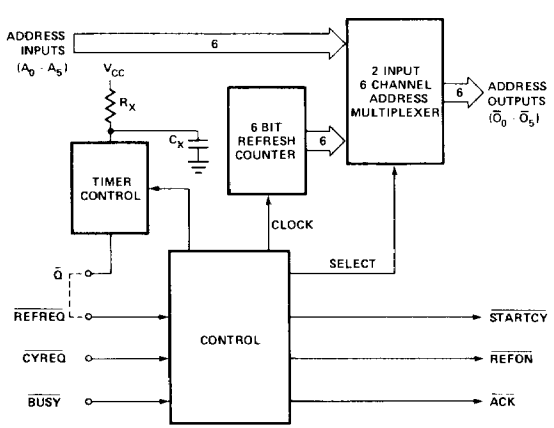
PIN CONFIGURATION



PIN NAMES

$A_0 - A_5$	ADDRESS INPUTS	$\bar{O}_0 - \bar{O}_5$	ADDRESS OUTPUTS
ACK	ACKNOWLEDGE OUTPUT	$\bar{Q}$	INTERNAL REFRESH REQUEST LATCH OUTPUT
BUSY	BUSY INPUT	REFON	REFRESH ON OUTPUT
CYREQ	CYCLE REQUEST INPUT	REFREQ	REFRESH REQUEST INPUT
		RxCx	RC TIE POINT
		STARTCY	START CYCLE OUTPUT
		V_{CC}	+5V SUPPLY

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65° to +125°C
Storage Temperature . . . . . -65° to +160°C
All Input, Output or Supply Voltages . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA
Power Dissipation . . . . . 1 W

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FB}	Input Load Current $\overline{BUSY}$		0.40	1	mA	V_{IN} = 0.45V
I_{FO}	Input Load Current All Other Inputs		0.05	0.25	mA	V_{IN} = 0.45V
I_{RB}	Input Leakage Current $\overline{BUSY}$		<1	50	μA	V_{IN} = V_{CC}
I_{RO}	Input Leakage Current All Other Inputs		<1	20	μA	V_{IN} = 5.25V
V_{CLAMP}	Input Clamp Voltage		-0.76	-1	V	I_C = -5.0mA
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{CC}	Power Supply Current		91	120	mA	V_{CC} = 5.25V
I_{SC}	Output High Short Circuit Current		-48	-70	mA	V_{OUT} = 0V V_{CC} = 5.25V
V_{OL}	Output Low Voltage		0.32	0.45	V	I_{OL} = 5mA
V_{OH}	Output High Voltage ($\overline{O}_0$-$\overline{O}_5$)	2.6	3.1		V	I_{OH} = -1mA V_{CC} = 4.75V
V_{OH1}	Output High Voltage (All Other Outputs)	2.4	3.0		V	I_{OH} = -1mA V_{CC} = 4.75V

Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

Capacitance[2], T_A = 25°C

Symbol	Test	Limits (pF)		Conditions
		Typ.	Max.	
C_{IN} (Address)	Input Capacitance	5	10	V_{bias} = 2.0V
C_{IN} ($\overline{CYREQ}$)	Input Capacitance	6	10	V_{CC} = 0V
C_{IN} ($\overline{BUSY}$)	Input Capacitance	20	30	f = 1MHz

Note 2: This parameter is periodically sampled and is not 100% tested.

A.C. Characteristics

All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C. Load = 1 TTL, C_L = 15pF.
Conditions of Test: Input pulse amplitude: 3V, Input rise and fall times: 5ns between 1V and 2V. Measurements are made at 1.5V.

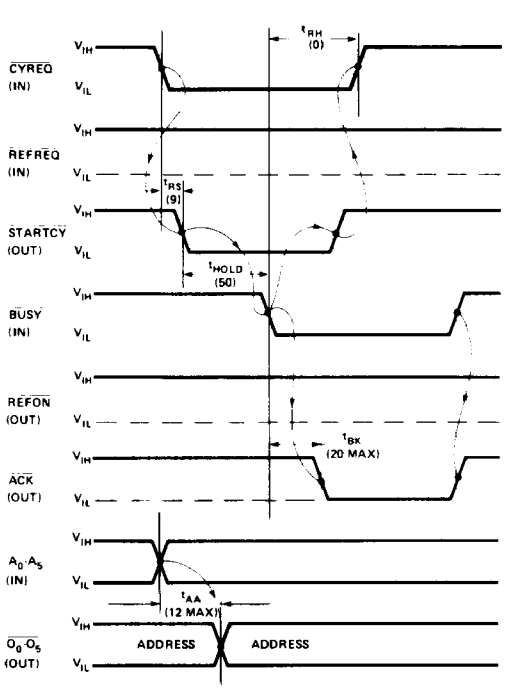
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
t_{AA}	Address In to Address Out		7	12	ns	$\overline{BUSY}$ = V_{IH}
t_{BAM}	$\overline{BUSY}$ In to Address Out		21	28	ns	
t_{BAR}	$\overline{BUSY}$ In to Counter Out		18	27	ns	
t_{BK}	$\overline{BUSY}$ In to $\overline{ACK}$ Out		14	20	ns	$\overline{REFREQ}$ = V_{IH}, $\overline{CYREQ}$ = V_{IL}
t_{BR}	$\overline{BUSY}$ In to $\overline{REFON}$ Out		15	24	ns	
t_{BS}	$\overline{BUSY}$ In to $\overline{STARTCY}$ Out	4	7	14	ns	$\overline{CYREQ}$ = V_{IL}
t_{HOLD}	$\overline{BUSY}$ Hold Time	50			ns	External Delay between $\overline{STARTCY}$ and $\overline{BUSY}$
t_{RH}	$\overline{CYREQ}$ or $\overline{REFREQ}$ Hold Time	0			ns	External Delay after $\overline{BUSY}$
t_{RR}	$\overline{REFREQ}$ to $\overline{REFON}$		18	26	ns	$\overline{CYREQ}$ and $\overline{BUSY}$ = V_{IH}, No priority contention between $\overline{REFREQ}$ and $\overline{CYREQ}$
t_{RRC}	$\overline{REFREQ}$ to $\overline{REFON}$		33	45	ns	$\overline{BUSY}$ = V_{IH}
t_{RS}	$\overline{CYREQ}$ or $\overline{REFREQ}$ In to $\overline{STARTCY}$ Out	9	14	21	ns	$\overline{BUSY}$ = V_{IH}
t_{Setup}	$\overline{BUSY}$ Setup Time	120			ns	$\overline{BUSY}$ = V_{IL} During Refresh

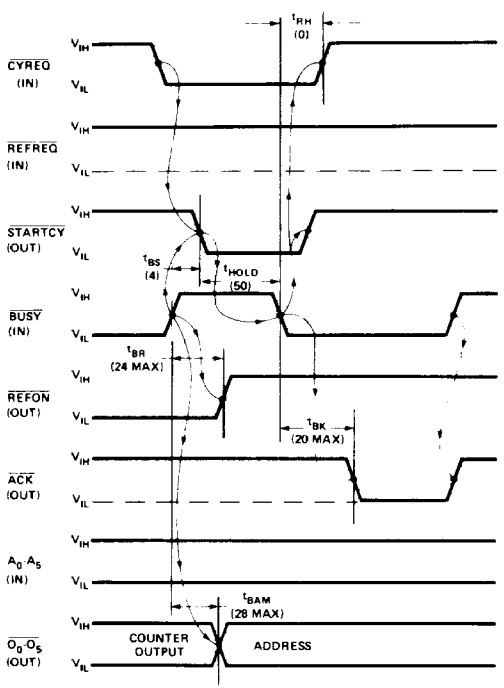
Note 1: Typical values are for T_A = 25°C and nominal power supply voltages.

A. SYSTEM MEMORY CYCLE WITH MEMORY NOT BUSY

B. SYSTEM MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING REFRESH CYCLE)

(Numbers in parentheses are minimum values in ns unless otherwise specified.)

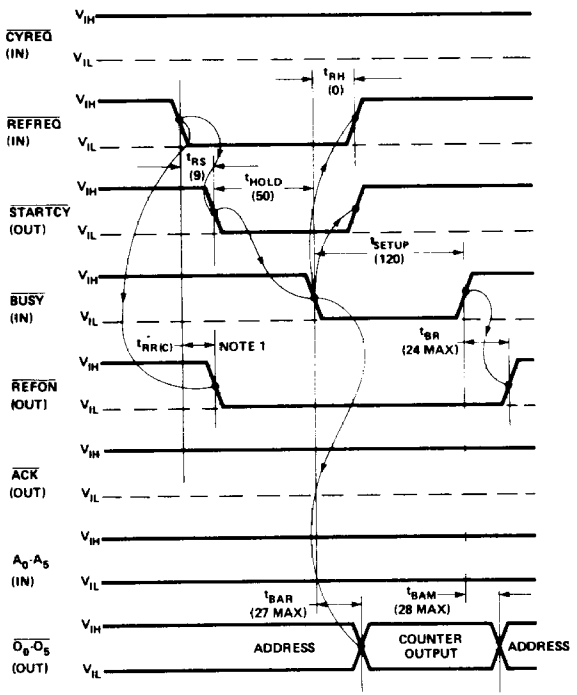




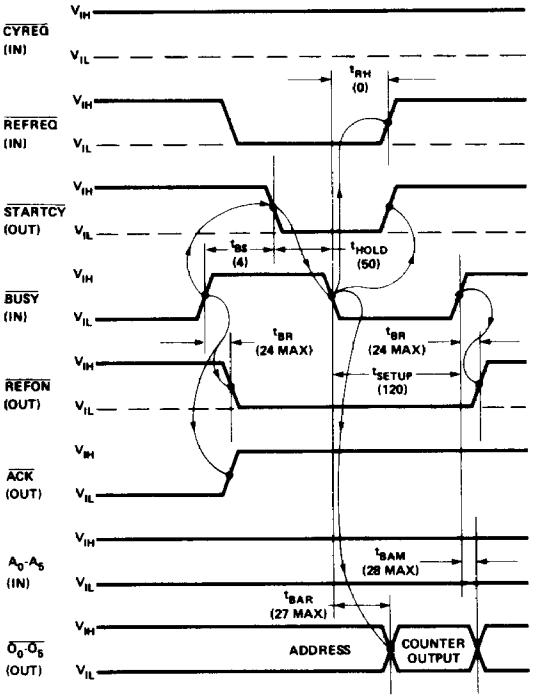
C. REFRESH MEMORY CYCLE WITH MEMORY NOT BUSY

D. REFRESH MEMORY CYCLE WITH MEMORY BUSY (FOLLOWING SYSTEM CYCLE)

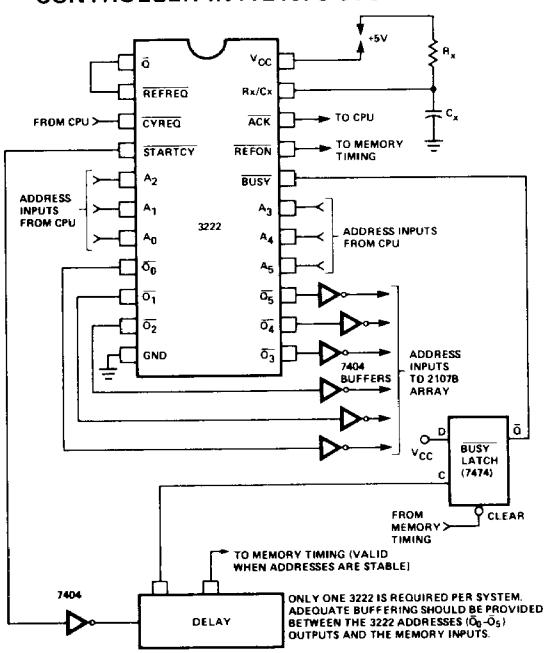
(Numbers in parentheses are minimum values in ns unless otherwise specified.)



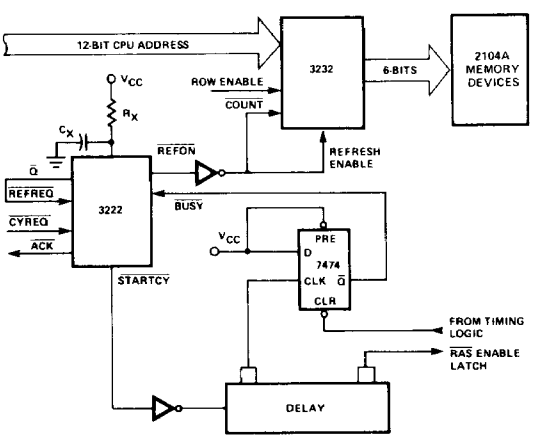
NOTE 1: t_{RR} (26ns MAX) IF PRIORITY CONTENTION IS ELIMINATED; t_{RRC}



E. TYPICAL APPLICATION OF 3222 REFRESH CONTROLLER IN A 2107C SYSTEM



F. USE OF 3222 FOR REFRESH TIMING AND CONTROL IN A 2104A SYSTEM



PIN NAMES AND FUNCTIONS

Pin No.	Pin Name	Function
1	$\overline{Q}$	Output of the internal Refresh Request latch. This pin may be connected to the Refresh Request input ($\overline{REFREQ}$) directly for asynchronous sequential mode refresh or indirectly through control logic for burst mode or synchronous mode refresh (see text).
2	$\overline{REFREQ}$	Refresh Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a system cycle request did not occur first.
3	$\overline{CYREQ}$	System Memory Cycle Request input (active when low). The request is honored only if the memory is not presently executing a cycle ($\overline{BUSY}$ high) and if a refresh request did not occur first.
4	$\overline{STARTCY}$	Output signal indicating to external circuitry that a memory cycle (system or refresh) is to begin. See text for timing considerations for a refresh cycle.
5-7 15-17	A_0-A_5	Low order system address inputs. These addresses are multiplexed to the address output pins ($\overline{O}_0$-$\overline{O}_5$) during a system cycle.
8-10	$\overline{O}_0$-$\overline{O}_5$	Low order memory address outputs. During a system cycle these outputs give the low order (A_0-A_5) address of a memory access. During a refresh cycle these outputs give the refresh address (generated internal to the 3222).
11	GROUND	Ground.
18	$\overline{BUSY}$	An externally generated signal which the 3222 monitors to determine memory system status. If $\overline{BUSY}$ is high the memory is not busy and a system or refresh cycle may begin. If $\overline{BUSY}$ is low the memory is being accessed for a data I/O or refresh cycle and no other cycle may begin.
19	$\overline{REFON}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a refresh cycle (Refresh On).
20	$\overline{ACK}$	The 3222 output which when low indicates the memory system is either ready to begin or is in a system cycle (system cycle request accepted and acknowledged).
21	RX/CX	Connection point for the RC network which determines the refresh period for sequential refresh mode. (See Refresh Control section).
22	V_{CC}	+5 volt supply.

FUNCTIONAL DESCRIPTION

The Intel® 3222 performs the four basic functions of a refresh controller by:

1. Providing a refresh timing oscillator.
2. Generating six bit refresh addresses.
3. Multiplexing refresh and system addresses to the six low order address inputs ($\overline{O}_0$-$\overline{O}_5$).
4. Providing control signals for both refresh and memory cycle accesses.

As shown in the pin configuration figure, the 3222 has as inputs the six low order (A_0-A_5) system addresses. These addresses are internally multiplexed with six internally generated refresh addresses. The output of these multiplexers provide the six low order addresses to the memory array.

The block diagram shows the four main circuit categories of the 3222. An explanation of the workings of each of these categories is given in the Device Operation section from a users point of view.

DEVICE OPERATION

Operation of the Intel® 3222 Refresh Controller is most easily explained by considering five conditions presented by the three input control lines Cycle Request ($\overline{CYREQ}$), Refresh Request ($\overline{REFREQ}$), and System Busy ($\overline{BUSY}$). These conditions are:

1. System memory cycle request — memory not busy ($\overline{BUSY}$ = High)
2. System memory cycle request — memory busy ($\overline{BUSY}$ =Low)
3. Refresh cycle request — memory not busy ($\overline{BUSY}$ = High)
4. Refresh cycle request — memory busy ($\overline{BUSY}$ =Low)
5. Simultaneous system memory cycle and refresh cycle requests.

Condition 5 is actually a subset of the four previous conditions and is included for completeness.

As is implied in the five conditions, the response of the 3222 to both refresh and memory cycles is dependent on the state of the $\overline{BUSY}$ input. The $\overline{BUSY}$ signal is generated externally to the 3222 and, when low, defines the time when the memory is performing a cycle (refresh or memory access). It is important to assure that $\overline{BUSY}$ is low for the *entire* memory cycle time. Interference may occur in asynchronous memory systems if the $\overline{BUSY}$ input goes high prematurely. (An asynchronous memory system is one in which the refresh and memory cycle requests occur independent of each other.)

System Memory Cycle Request — Memory Not Busy

This section details operation of the 3222 when the memory is not busy and a request for a system memory cycle is made (See Figure A for timing sequences). The request for a memory cycle is made by the $\overline{CYREQ}$ input going low. The Start Cycle output $\overline{STARTCY}$ goes low at t_{RS} after $\overline{CYREQ}$. $\overline{STARTCY}$ is used for two purposes:

1. To set the external $\overline{BUSY}$ latch. (See Figure E.)
2. To initiate memory system timing (after appropriate delay).

The required delay time depends on system configuration and associated delay paths for both Chip Enable (2107B input signal) and system addresses.

The low going $\overline{BUSY}$ input causes the internally generated Start Cycle output to go high and the Acknowledge output $\overline{ACK}$ to go low (after t_{BK} time). The Acknowledge output confirms that the requested system memory cycle has been accepted by the 3222. Note that the cycle request input may be returned to the high state when the $\overline{BUSY}$ input goes low. However, at the designer's discretion, the cycle request line may remain low until "just prior" to $\overline{BUSY}$ returning high. (If $\overline{BUSY}$ goes high before $\overline{CYREQ}$ goes high, another memory access may inadvertently be started.)

When the memory is not busy and a cycle request has been made, the low order system address delay through the 3222 is t_{AA} nsec. When the 3222 is not busy, the low order system addresses (A_0-A_5) are gated through to the output ($\overline{O}_0$-$\overline{O}_5$) independent of any other input.

System Memory Cycle Request — Memory Busy

The major differences between a system memory cycle request when the system is busy and when it is not busy (as previously described) are:

1. The Start Cycle output $\overline{STARTCY}$ does not go low until t_{BS} after the rising edge of the $\overline{BUSY}$ input. (Even though the $\overline{CYREQ}$ input is low.)
2. Output addresses $\overline{O}_0$-$\overline{O}_5$ change at or before t_{AA} time if the previous cycle was a system cycle request and change at or before t_{BAM} if the previous cycle was a Refresh Cycle request. (Note that the longer delay is after a refresh cycle.) See Figure B for definition of terms.

Note that for a system memory cycle following a refresh cycle, the refresh on output $\overline{REFON}$ goes high at or before t_{BR} relative to $\overline{BUSY}$ going high. Since the Acknowledge output $\overline{ACK}$ can not go low until after t_{HOLD} there is no ambiguity between $\overline{REFON}$ and $\overline{ACK}$. The memory is always defined as being in a refresh cycle, system cycle or no cycle.

Refresh Cycle — Memory Not Busy

Operation of the 3222 for a refresh request with the memory not busy (see Figure C) is similar to a system cycle request under the same condition. A refresh cycle is initiated by the Refresh Request input ($\overline{REFREQ}$) going low. This low going input causes both the Start Cycle output, $\overline{STARTCY}$, and Refresh On output, $\overline{REFON}$, to go low at t_{RS} and t_{RRC} (or t_{RR}) time respectively. The low going edge of $\overline{STARTCY}$ is used to set the external $\overline{BUSY}$ latch low. As in the previous two cases, the $\overline{BUSY}$ input must remain low for the entire cycle required by the memory. As in the previous two cases, the low going $\overline{BUSY}$ drives the $\overline{STARTCY}$ output high.

Refresh Cycle — Memory Busy

For this condition, it is assumed that the previous cycle was a system access cycle. Timing conditions for this operation are shown in Figure D. Here, the $\overline{STARTCY}$ input goes low t_{BS} after $\overline{BUSY}$ returns high from the previous cycle. As before, $\overline{REFON}$ goes low t_{BR} after $\overline{BUSY}$ goes high. After t_{HOLD}, relative to $\overline{STARTCY}$, $\overline{BUSY}$ again goes low and places the low order refresh addresses on the address outputs ($\overline{O}_0$-$\overline{O}_5$) after t_{BAR} time. Internal refresh timing is performed in a manner identical to that described in Refresh Cycle-Memory Not Busy section.

Simultaneous Refresh and Memory System Cycle Request

The simultaneous request for a refresh and memory system access is almost a certainty in asynchronous systems. It is, therefore, necessary to have circuitry in any refresh controller capable of resolving the attendent ambiguity with minimum additional delay. The Intel® 3222 Refresh Controller has just such a circuit. (All timing parameters specified for asynchronous operation assume that a refresh and memory system request can occur at the same time.) A latch internal to the 3222 decides which signal ($\overline{CYREQ}$ or $\overline{REFREQ}$) it will accept if both occur simultaneously, and conditions the other control circuits appropriately. If a refresh cycle was accepted, $\overline{REFON}$ will go low at the appropriate time. If a memory system access was accepted then $\overline{ACK}$ will go low at the appropriate time.

Refresh Control

The 3222 controls both burst and distributed refresh modes. The burst refresh mode requires that $\overline{REFREQ}$ be generated externally to the 3222 since refresh is completed in 64 consecutive cycles every 2ms. A system requiring distributed refresh timing, however can be controlled either by the 3222 or by external circuitry. If refresh timing is to be controlled by the 3222 the output $\overline{Q}$ is tied to the $\overline{REFREQ}$ input. Timing is controlled by an oscillator internal to the 3222. The desired refresh timing interval is determined by:

1. $\frac{t_{REF}}{r} = .63\ R_xC_x$

   Where:

   t_{REF} = the total time between refreshes (e.g. 2msec) in msec.

   r = the number of rows to be refreshed on the memory device (for the 2107C r = 64).

   R_x = external timing resistance in KΩ (3K to 10K)

   C_x = external timing capacitance in μf. (0.005μf to 0.02μf)

The 3222's oscillator stability is guaranteed to be ±2% for a given part and ±6% from part to part, both over the ranges $0°C \leq T_A \leq 75°C$ and $V_{CC} = 5.0V \pm 5\%$.

Figure F shows how the 3222 may be used to control refresh in a 2104A system.