

FEATURES

- Drop-in replacement for IBM AT computer clock/calendar
- Pin compatible with the MC146818B and DS1287A
- Totally nonvolatile with over 10 years of operation in the absence of power
- Self-contained subsystem includes lithium, quartz, and support circuitry
- Counts seconds, minutes, hours, days, day of the week, date, month, and year with leap-year compensation valid up to 2100
- Binary or BCD representation of time, calendar, and alarm
- 12-hour or 24-hour clock with AM and PM in 12-hour mode
- Daylight Savings Time option
- Selectable between Motorola and Intel bus timing
- Multiplex bus for pin efficiency
- Interfaced with software as 128 RAM locations
 - 14 bytes of clock and control registers
 - 114 bytes of general-purpose RAM
- Programmable square-wave output signal
- Bus-compatible interrupt signals (IRQ)
- Three interrupts are separately software-maskable and testable
 - Time-of-day alarm once/second to once/day
 - Periodic rates from 122μs to 500ms
 - End-of-clock update cycle
- Underwriters Laboratory (UL) recognized

PIN ASSIGNMENT (Top View)

MOT	1	24	V _{CC}
N.C.	2	23	SQW
N.C.	3	22	NC
AD0	4	21	RCLR
AD1	5	20	N.C.
AD2	6	19	IRQ
AD3	7	18	RESET
AD4	8	17	DS
AD5	9	16	N.C.
AD6	10	15	R/W
AD7	11	14	AS
GND	12	13	CS

[DS12887A](#)

[24 PDIP Module \(700mil\)](#)

Package Dimension Information

<http://www.maxim-ic.com/TechSupport/DallasPackInfo.htm>

PIN DESCRIPTION

AD0–AD7	-	Multiplexed Address/Data Bus
N.C.	-	No Connect
MOT	-	Bus Type Selection
CS	-	RTC Chip-Select Input
AS	-	Address Strobe
R/W	-	Read/Write Input
DS	-	Data Strobe
RESET	-	Reset Input
IRQ	-	Interrupt Request Output
SQW	-	Square-Wave Output
V _{CC}	-	+5V Main Supply
RCLR	-	RAM Clear
GND	-	Ground

ORDERING INFORMATION

PART	PIN-PACKAGE	TOP MARK	TEMP RANGE
DS12887A	24 PDIP Module	DS12887A	0°C to +70°C

DESCRIPTION

The DS12887A real-time clock plus RAM is designed to be a direct replacement for the DS1287A. The DS12887A is identical in form, fit, and function to the DS1287A, and includes additional 64 bytes of general-purpose RAM. Access to this additional RAM space is determined by the logic level presented on AD6 during the address portion of an access cycle. The $\overline{\text{RCLR}}$ pin is used to clear (set to logic 1) all 114 bytes of general-purpose RAM but does not affect the RAM associated with the real-time clock. In order to clear the RAM, $\overline{\text{RCLR}}$ must be forced to an input logic 0 (-0.3V to $+0.8\text{V}$) during battery-backup mode when V_{CC} is not applied. The $\overline{\text{RCLR}}$ function is designed to be used by human interface (shorting to ground manually or by switch) and not to be driven with external buffers.

For a complete description of operating conditions, electrical characteristics, bus timing and pin descriptions other than $\overline{\text{RCLR}}$, refer to the DS12887 data sheet.

Note: Pins 2, 3, 16, 20, and 22 are missing by design. This device cannot be stored or shipped in conductive material that will give a continuity path between the RAM clear pin and ground.

TYPICAL OPERATING CIRCUIT

