HUGHES MICROELECTRONICS LIMITED
Subsidiary of Hughes Aircraft Company

H3300

32 x 8 CMOS EEPROM

DESCRIPTION

Hughes H3300 is a CMOS Electrically Erasable Programmable ROM (EEPROM), organised as 32 x 8. Read and Write operations are performed with a single 5V power supply using simple TTL level control signals.

Writing data into nonvolatile storage is performed in a manner similar to the write control of a static RAM. A short logic low pulse to the $\overline{WE}$ pin (Write Enable) initiates the Byte Write operation which is completed with on-chip timing (a separate Erase operation is not required). Addresses and data are internally latched to free the system bus for other tasks during the Write period.

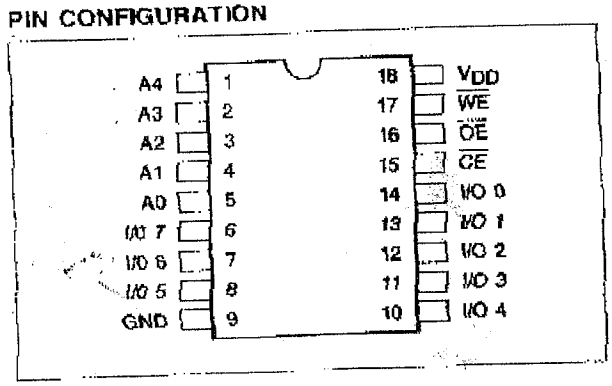
A Read operation is performed by presenting the byte address and enabling the chip with $\overline{CE}$ (Chip-Enable) low. The device uses a two-line control architecture, $\overline{CE}$ and $\overline{OE}$ (Output Enable), to eliminate bus-contention in a system environment.

Hughes H3300 is available in an 18 lead hermetic dual-in-line ceramic package (D suffix) and plastic package (P suffix). Devices in chip form (H suffix) are available upon request. Commercial (HC3300), Industrial (HI3300), and Military (HB3300) versions are available.

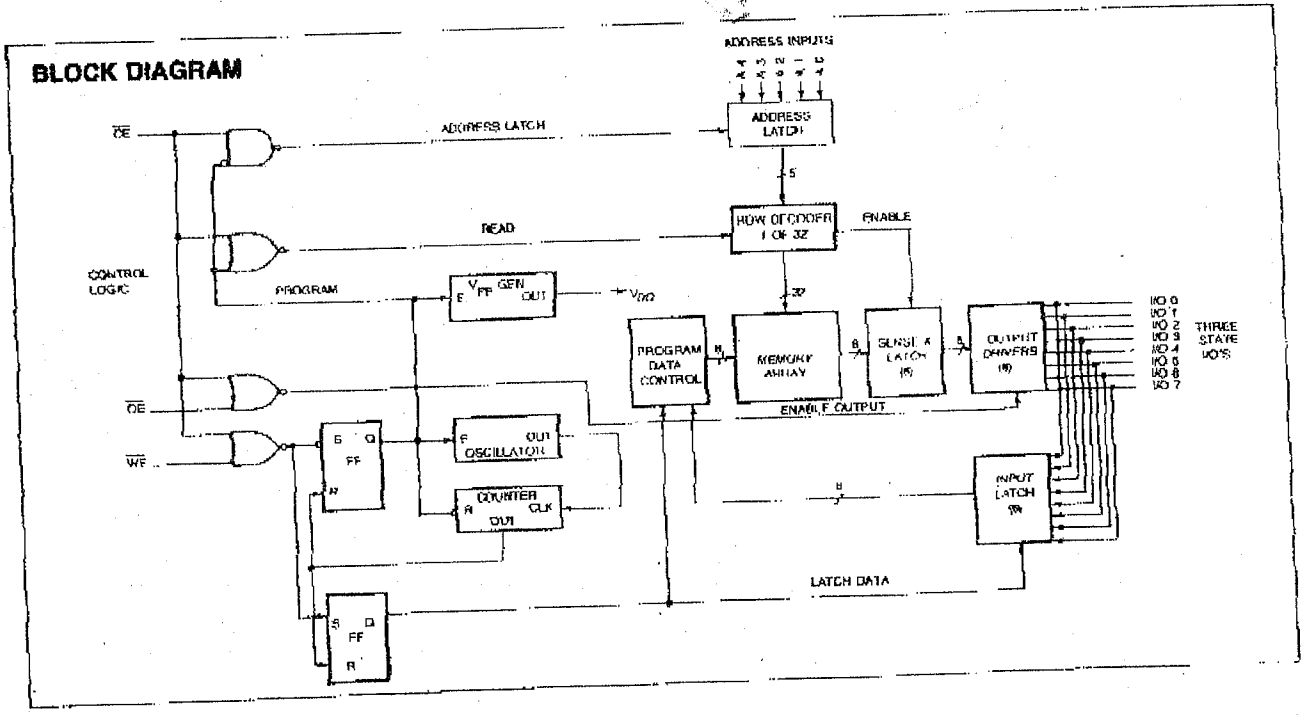
FEATURES

- Byte wide organisation — 32 x 8 bit
- Single 5V power supply — Read and Write
- Very low power dissipation — CMOS
- Byte programmable with No Erase required
- On chip timing for Byte Write
- On chip Address & Data latches
- Simple and efficient 3-line control ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$)
- 10 Year Data Retention[3]
- 10,000 Byte Write Cycles (Endurance)[3]

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range ..... −0.3 to +6V
(All voltages referenced to GND Pin)
Input Voltage Range ..... −0.3 to V_{DD} +0.3V
Storage Temperature Range .. −65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage		5V ± 5%	5V ± 5%
Temperature Range	Plastic Package	−40°C to +85°C	−40°C to +85°C
	Ceramic Package	−55°C to +125°C	−55°C to 125°C

DC OPERATING CHARACTERISTICS

Read: V_{DD} = 5V ± 5% Unless Otherwise Specified

		−40°C to +85°C			−55°C to +125°C				
		Min	Typ	Max	Min	Typ	Max		
I_{DDS}	V_{DD} Standby Current	—	25	100	—	200	—	200	µA	$\overline{CE}$ = $\overline{WE}$ = 5V, OE = O All I/O's = open
I_{DDA}	V_{DD} Active Current[1]	—	25	100	—	200	—	200	µA	$\overline{CE}$ = $\overline{OE}$ = O, WE = 5V All I/O's = open
V_{OL}	Output Low Voltage	—	0.25	0.45	—	0.45	—	0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	3.0	4.5	—	3.0	—	3.0	—	V	I_{OH} = − 400 µ A
V_{IL}	Input Low Voltage	—	—	0.8	—	0.8	—	0.8	V	—
V_{IH}	Input High Voltage	3.2	—	—	3.2	—	3.2	—	V	—
I_{LI}	Input Leakage Current	—	±0.1	±10	—	±10	—	± 10	µA	V_{IN} = 0 or 5V
I_{LO}	Output Leakage Current	—	±0.3	±10	—	±10	—	±10	µA	V_{OUT} = 0 or 5V

Notes
(1) This parameter is sampled only and is not 100% tested.
(2) Endurance is the number of possible Write cycles per Syte.
(3) Retention is the amount by time data is retained in memory without power applied.

AC OPERATING CHARACTERISTICS

Read: V_{DD} = 5V ± 5% Unless Otherwise Specified

t_{CEH}	$\overline{CE}$ High Time	350	200	—	450	—	600	—	ns	$\overline{WE}$ = V_{IH}, CE low time = $t_{ACE(Max)}$
t_{ACE}	Chip Enable Access Time	—	400	500	—	650	—	700	ns	$\overline{WE}$ = V_{IH}
t_{OE}	Output Enable Access Time	—	225	275	—	350	—	375	ns	$\overline{WE}$ = V_{IH}
t_{ASU}	Address Set Up Time	100	25	—	165	—	250	—	ns	$\overline{WE}$ = V_{IH}
t_{AH}	Address Hold Time	50	25	—	50	—	50	—	ns	$\overline{WE}$ = V_{IH}
t_{OH}	Output Hold from $\overline{OE}$ or $\overline{CE}$ High	0	—	—	0	—	0	—	ns	$\overline{WE}$ = V_{IH}
t_{DF}	Output Float from $\overline{OE}$ or $\overline{CE}$ High	—	—	400	—	475	—	525	ns	$\overline{WE}$ = V_{IH}
t_{DDR}	Dynamic Read Current	—	0.3	.5	—	.5	—	.5	mA	f = 100 KHz

Write V_{DD} = 5V ± 5% Unless Otherwise Specified

t_{CES}	$\overline{CE}$ Set Up Time	0	—	—	0	—	0	—	ns	$\overline{OE}$ = V_{IH}
t_{CEH}	$\overline{CE}$ Hold Time	0	—	—	0	—	0	—	ns	$\overline{OE}$ = V_{IH}
t_{WP}	Write Pulse Width	500	350	—	650	—	700	—	ns	$\overline{OE}$ = V_{IH}
t_{ASP}	Address Set Up Time	100	25	—	165	—	250	—	ns	$\overline{OE}$ = V_{IH}
t_{AHP}	Address Hold Time	50	25	—	50	—	50	—	ns	$\overline{OE}$ = V_{IH}
t_{DS}	Data Set Up Time	0	−200	—	0	—	0	—	ns	$\overline{OE}$ = V_{IH}
t_{DH}	Data Hold Time	325	240	—	400	—	450	—	ns	$\overline{OE}$ = V_{IH}
t_{WES}	$\overline{WE}$ Set Up Time	0	—	—	0	—	0	—	ns	$\overline{OE}$ = V_{IH}
t_{WEH}	$\overline{WE}$ Hold Time	0	—	—	0	—	0	—	ns	$\overline{OE}$ = V_{IH}
t_P	Program Cycle Time	—	5	10	—	10	—	10	ms	$\overline{OE}$ = V_{IH}, $\overline{CE}$ = V_{IL}
I_{DDW}	Dynamic Write Current	—	.3	.8	—	1.0	—	1.0	mA	f = 100 Hz, V_{DD} = 5.25V

AC TEST CONDITIONS

Output Load: C_L = 50 pF

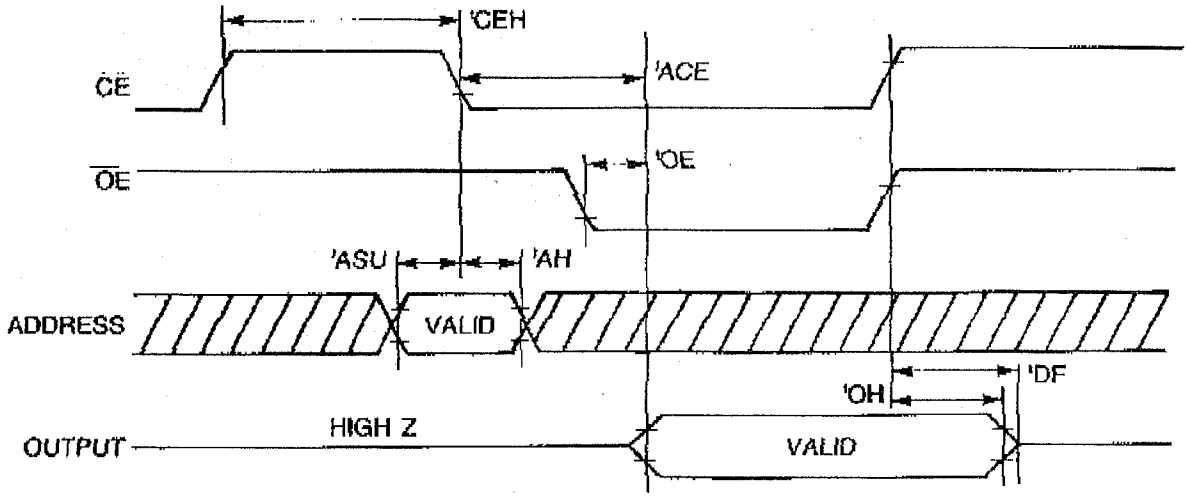
Input Levels: V_H = 3.2 V, V_L = 0.4V

Timing Measurement Reference Level: Input = Output = 50% V_{DD}

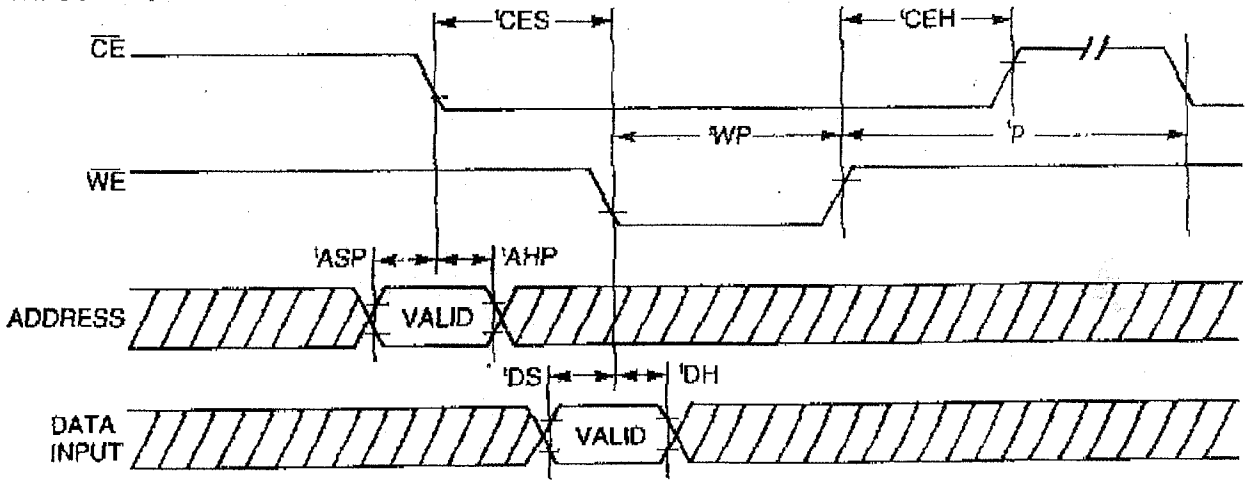
Input Rise and Fall Time: t_r = t_f = 10 ns

TIMING DIAGRAM

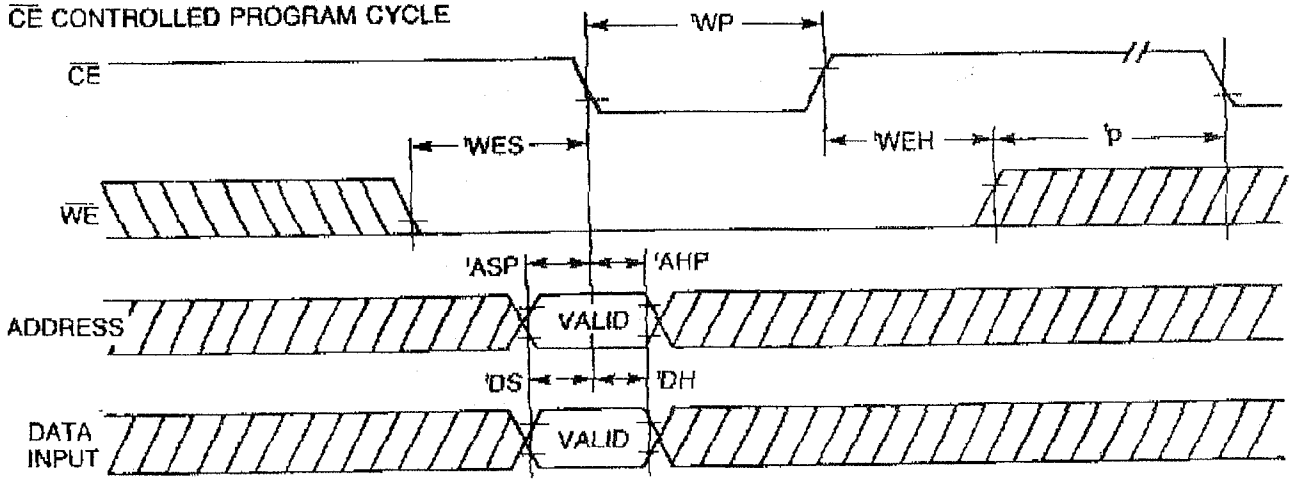
READ



WE CONTROLLED PROGRAM CYCLE



CE CONTROLLED PROGRAM CYCLE



OPERATING MODES
Logic 1 = High, Logic 0 = Low, X = Do Not Care

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	1	X	X	Floating
Read	0	1	1	Floating
Read	0	0	1	Data Output
Write	0	1	0	Data Input
Prohibited	0	0	0	Active

STANDBY MODE: With $\overline{CE}$ high the circuit is inactive, independent of the state of any other input.

READ MODE: The falling edge of $\overline{CE}$ latches the input address and initiates a Read cycle. When $\overline{CE}$ is low, a low input to $\overline{OE}$ turns on the three-state output bus drivers.

WRITE MODE: Two Write control modes are made possible:

(1) With a $\overline{WE}$ controlled mode, the cycle is initiated with $\overline{CE}$ going low which latches the input address. When $\overline{WE}$ is taken low the input data is latched and the self timed program cycle beings when $\overline{WE}$ returns high.

(2) With a $\overline{CE}$ controlled mode, the cycle is initiated with $\overline{WE}$ going low. Both input address and data are latched when $\overline{CE}$ goes low and the self timed program cycle begins when $\overline{WE}$ returns high.

PROHIBITED MODE: A Write Cycle will occur in this mode and the three-state output drives will be turned on, creating a bus contention problem for normal writes.

PIN DESCRIPTION:

A0 – A4: Address inputs which select one of 32 bytes of memory for either Read or Write.

I/O0 – I/O7: Bidirectional three-state data lines that are data outputs during Read and data inputs during Writes.

GND: Negative supply terminal and V = 0 reference

V_{DD}: Positive supply terminal.

$\overline{CE}$: Chip Enable: This input causes the circuit to latch the input address and initiate a Read cycle when taken low. Read data remains valid while $\overline{CE}$ is held low. It also enables the $\overline{WE}$ input when low.

$\overline{OE}$: Output Enable. This input turns on the three-state output bus drivers when $\overline{CE}$ is low.

$\overline{WE}$: Write Enable. This input latches the data input when taken low if $\overline{CE}$ is low. A self timed Write cycle begins when $\overline{WE}$ is returned high.