

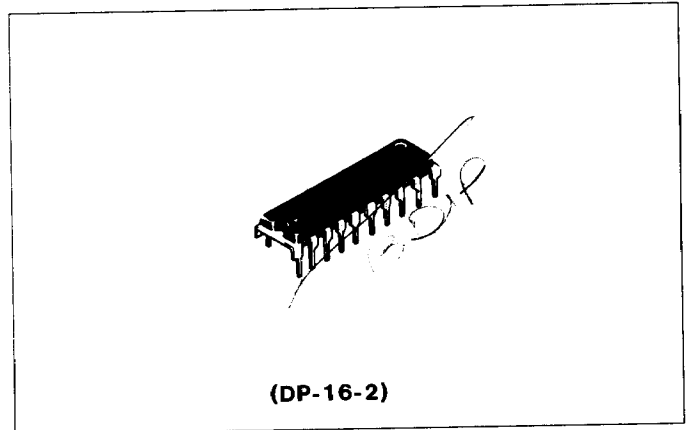
HA12006

Electronic Controller for Cassette Tape Deck

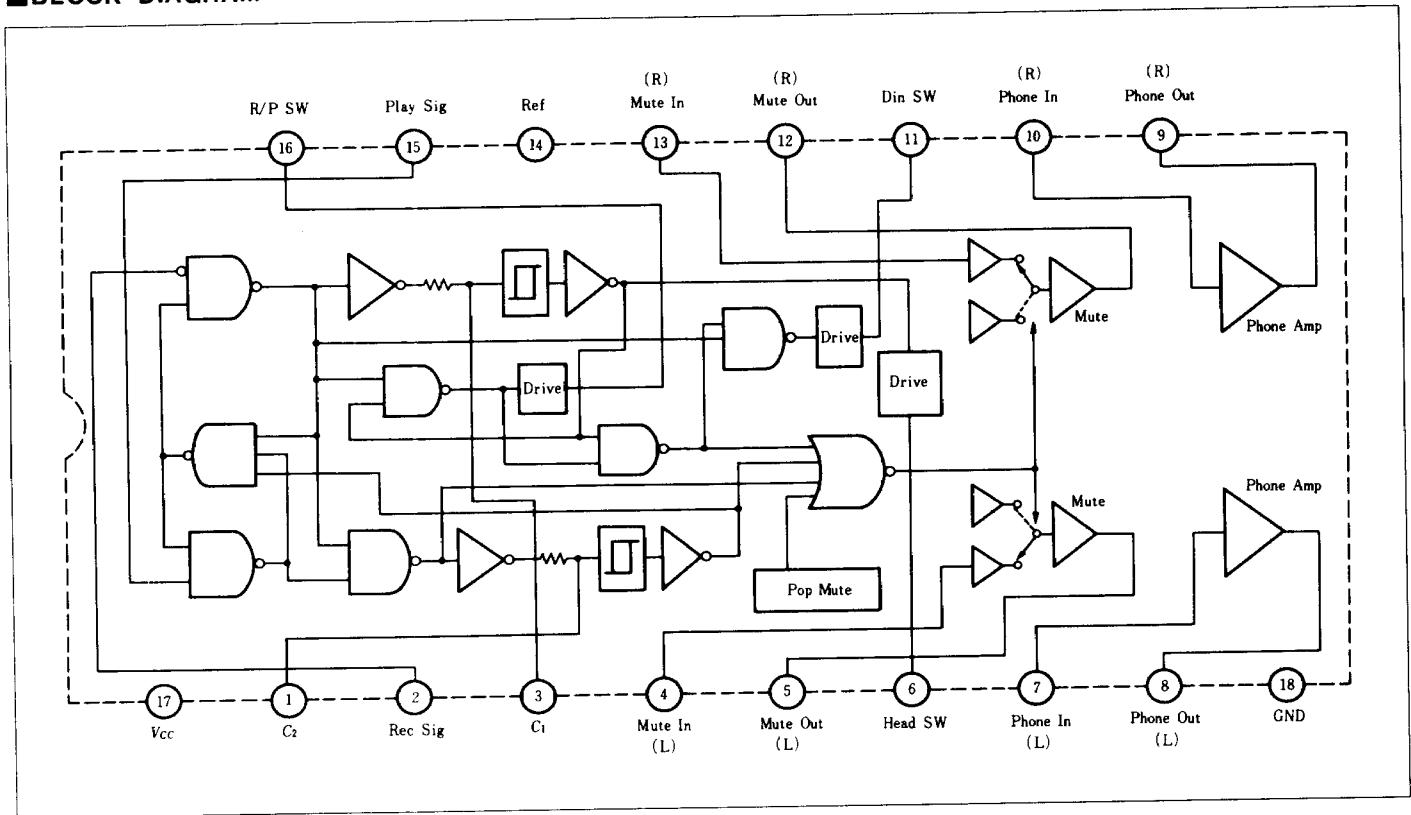
The HA12006 is designed for an electronic-controlled cassette deck system, providing Mute Amp., Phone Amp. and Switch-Control functions.

FEATURES

- Electronic controlled system provides cassette deck switches with feather-touch.
- Mute- and Phone-Amps built-in for two channels.
- Logic Control Circuit prevents, by timing delay, shock-noise caused by mode- or power source-turning.



BLOCK DIAGRAM



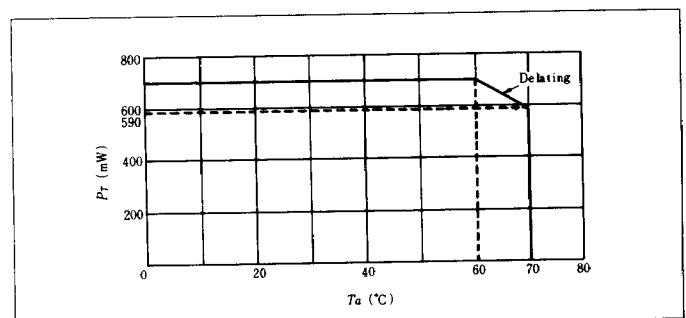
ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, $T_a = 25^\circ\text{C}$)

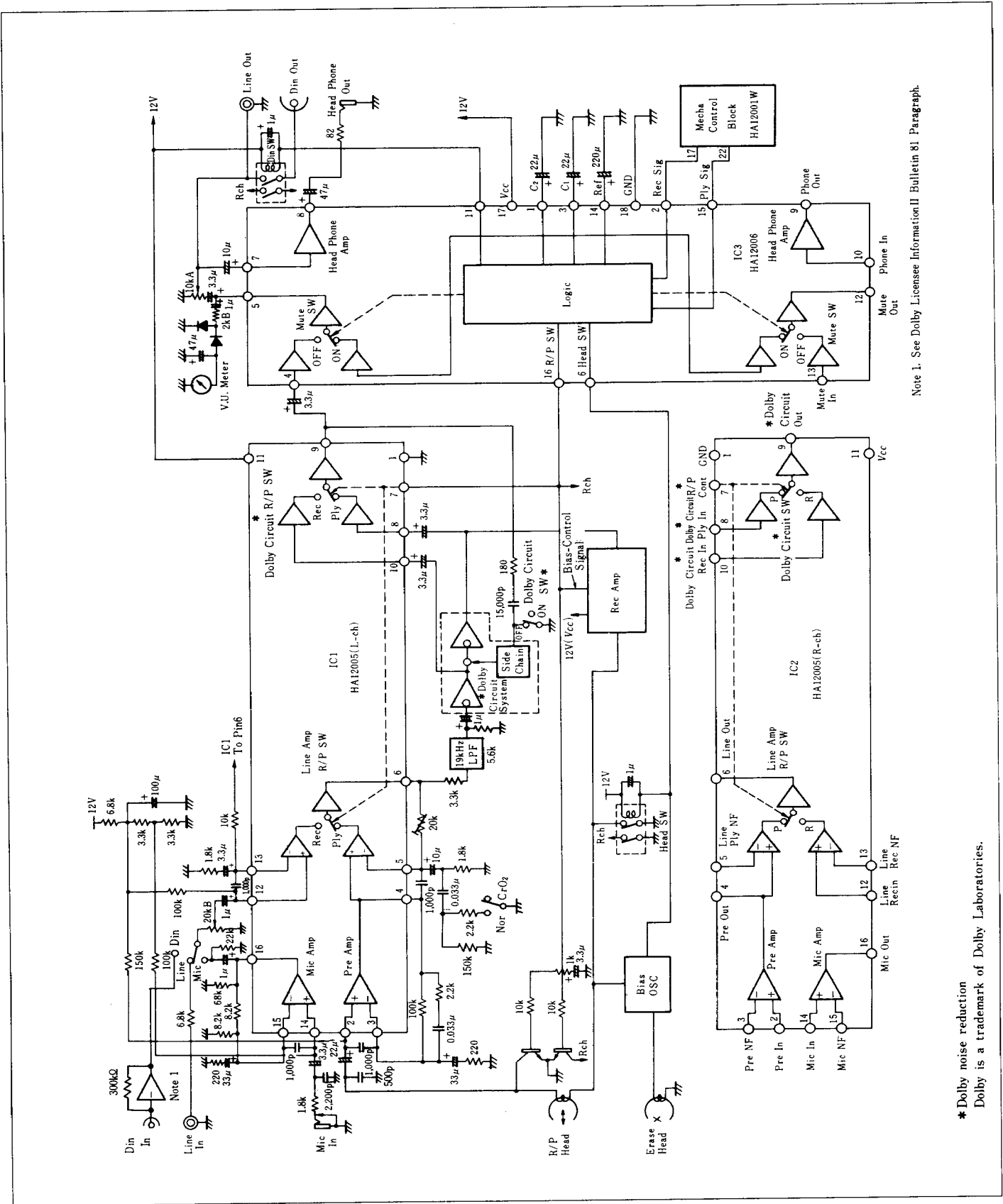
Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	15.0	V
Power Dissipation	P_T	700*	mW
Operating Temperature Range	T_{op}	-30 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +125	$^\circ\text{C}$

* Value at $T_a = 60^\circ\text{C}$

DELATING CURVE



■ BLOCK DIAGRAM FOR ELECTRONIC-CONTROLLED CASSETTE DECK SYSTEM



Note 1. See Dolby Licensee Information II Bulletin 81 Paragraph.

* Dolby noise reduction
Dolby is a trademark of Dolby Laboratories.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=12\text{V}$, and $f_i=1\text{kHz}$)

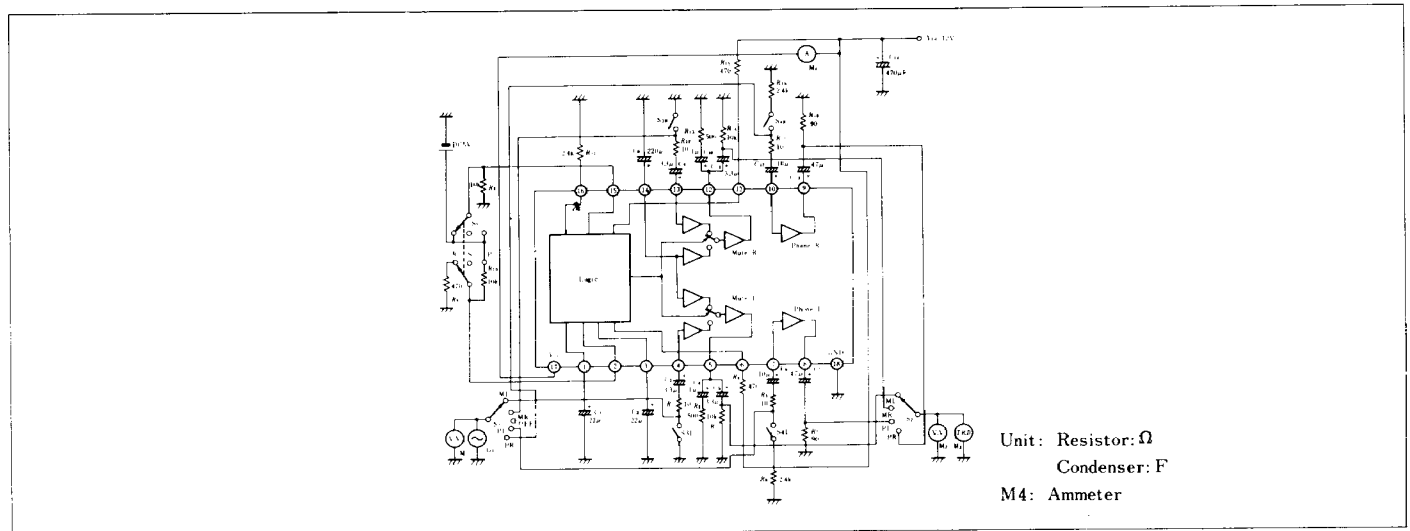
Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Operating Current	I_Q	No signal input. (PLY-mode)	—	19.1	31	mA
Mute Amp Max Output Voltage	$(e_{OMAX})_M$	$THD=1\%$, $R_L=500\Omega$	2.6	3.2	—	Vrms
Phone Amp Max Output Voltage	$(e_{OMAX})_P$	$THD=2\%$, $R_L=90\Omega$	1.4	2.2	—	Vrms
Mute Amp Hum Rejection	$(H.R)_M$	$f_i=100\text{Hz}$, $R_g=10\Omega+3.3\mu\text{F}$	—	58	—	dB
Phone Amp Hum Rejection	$(H.R)_P$	$f_i=100\text{Hz}$, $R_g=2.5\text{k}\Omega$	—	7.8	—	dB
Rated THD at Mute Amp	THD_M	$e_{OM}=550\text{mV}$	—	0.1	0.5	%
Muting Attenuation	$M.ATT$	$e_{IM}=3\text{V}$	70	76	—	dB

The above items all applicable to both R- and L-channels.

REC/PLY SW High Level Output Voltage	$V_{R/P(H)}$	$R_L=2.4\text{k}\Omega$, Pin-16 measured. $V_{(2)}=1.0\text{V}$, $V_{(15)}=1.3\text{V}$	10.0	10.5	—	V
REC/PLY SW Low Level Output Voltage	$V_{R/P(L)}$	$R_L=2.4\text{k}\Omega$, Pin-16 measured. $V_{(2)}=4.3\text{V}$, $V_{(15)}=1.3\text{V}$	—	0	0.25	V
HEAD SW High Level Output Voltage	$V_{HS(H)}$	$R_L=470\Omega$, Pin-6 measured. $V_{(2)}=1.0\text{V}$, $V_{(15)}=1.3\text{V}$	11.5	12.0	—	V
HEAD SW Level Output Voltage	$V_{HS(L)}$	$R_L=470\Omega$, Pin-6 measured. $V_{(2)}=4.3\text{V}$, $V_{(15)}=1.3\text{V}$	—	0.2	0.5	V
DIN SW High Level Output Voltage	$V_{DS(H)}$	$R_L=470\Omega$, Pin-11 measured. $V_{(2)}=1.0\text{V}$, $V_{(15)}=1.3\text{V}$	11.5	12.0	—	V
DIN SW Low Level Output Voltage	$V_{DS(L)}$	$R_L=470\Omega$, Pin-11 measured. $V_{(2)}=4.3\text{V}$, $V_{(15)}=1.3\text{V}$	—	0.2	0.5	V

Note: $V_{(2)}$ means the voltage at pin-2, and $V_{(15)}$ the voltage at pin-15.

TEST CIRCUIT



SWITCH POSITIONS FOR TEST CIRCUIT

Item	SW Position							Instrument
	S1	S2	S3L	S3R	S4L	S4R	S5	
$(e_{OMAX})_{M(L)}$	ML	ML	OFF	ON	ON	ON	P/R	M 2
$(e_{OMAX})_{M(R)}$	MR	MR	ON	OFF	ON	ON	P/R	M 2
$(e_{OMAX})_{P(L)}$	PL	PL	ON	ON	OFF	ON	*	M 2
$(e_{OMAX})_{P(R)}$	PR	PR	ON	ON	ON	OFF	*	M 2
$THD_{M(L)}$	ML	ML	OFF	ON	ON	ON	P/R	M 3
$THD_{M(R)}$	MR	MR	ON	OFF	ON	ON	P/R	M 3
$M.ATT_{(L)}$	ML	ML	OFF	ON	ON	ON	P/R→S	M 3
$M.ATT_{(R)}$	MR	MR	ON	OFF	ON	ON	P/R→S	M 3

* Any Position Applicable (P. R. S)

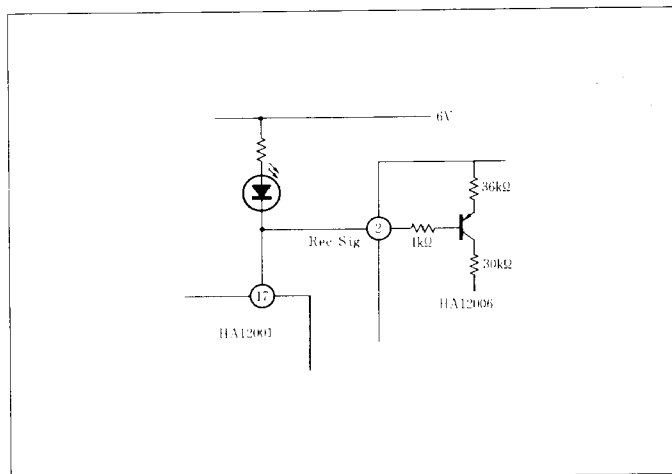
- Note: 1) Accuracy: Resistor Error: $\pm 1\%$ or less
 2) Withstand Voltage: Chemical Condensers: 16V
 The Other Condenser: 50V
 3) M1 & M2: The HP400E Type recommended
 4) G1 & M3: The Shibaden 870 Type recommended

■ LOGIC CIRCUIT FUNCTIONS

● INPUT SIGNAL (Pins 2 and 15)

REC SIG IN (pin-2) and PLY SIG IN (Pin-15) are supplied from the HA12001W, the Mechanical Controller. HA12006 pin-2 is connected to HA12001W pin-17, and HA12006 pin-12 to HA12001W pin-22.

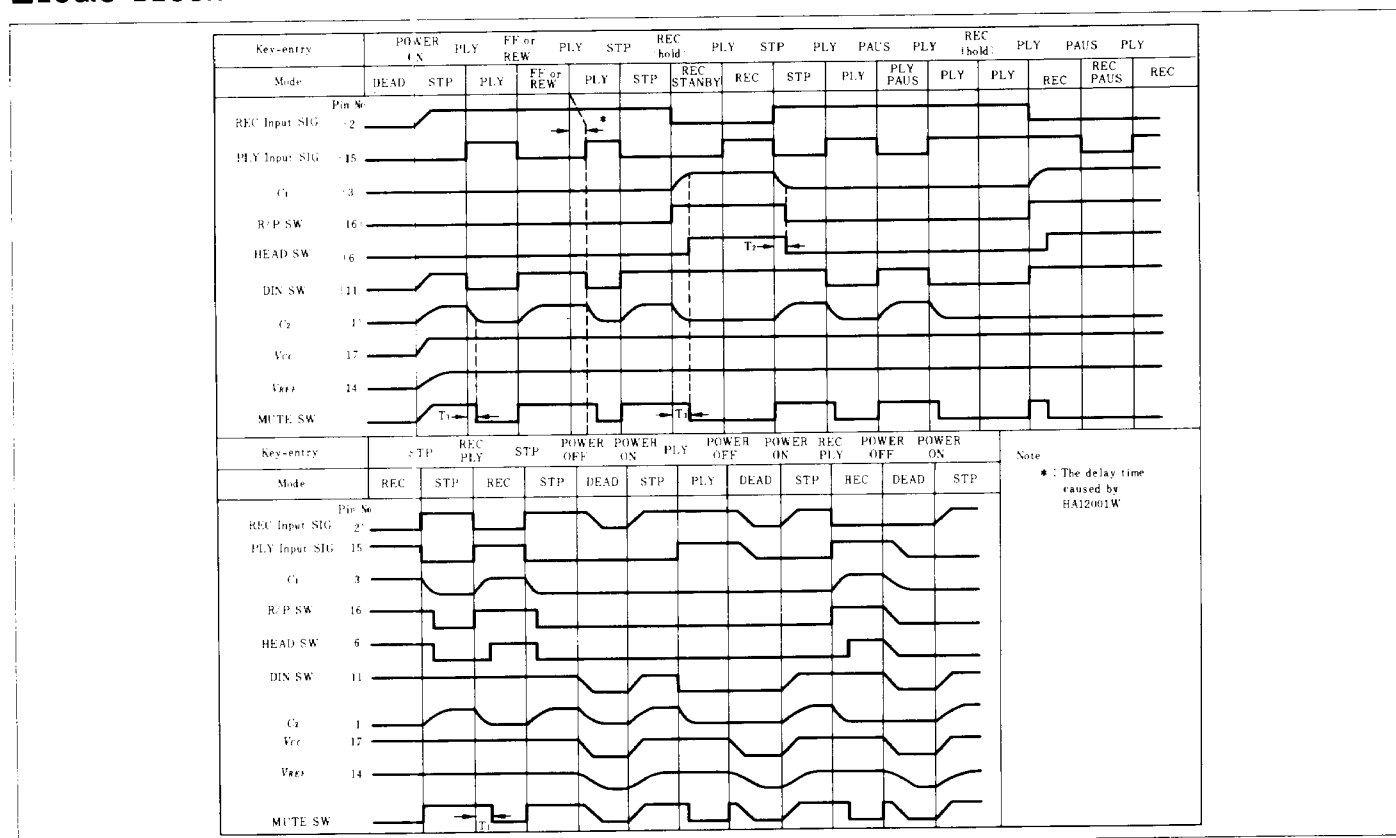
Pin No.	Name	Input Signal	Signal Level (typ)
2	REC SIG	HA12001W pin-17 REC Indicator	STP REC 5V 0.2V
15	PLY SIG	HA12001W pin-22 Head Plunger	STP/PAUS PLY/REC 4.5V 0.1V



REC SIG Terminal (pin-2) is connected to a 6V-supply via REC indicator lamp or LED.

A PNP Transistor is built-in, to prevent fine luminescence caused by over-10μA current through LED.

■ LOGIC BLOCK TIMING CHART



● TIMING CIRCUIT

(See TIMING BLOCK DIAGRAM)

Connecting pin-3 to C₁, and pin-1 to C₂, provides the following timings.

T₁: Prevent REC/PLY switching shock noise; charging C₁ generates an approx. 200ms delay of HEAD SW STP/REC-switching and MUTE SW ON/OFF-switching after REC goes to ON.

T₂: Prevents REC/STP switching shock noise; discharging C₁ generates an approx. 150ms delay of HEAD SW REC/

STP-switching after REC turns to OFF.

T₃; Prevents STP/PLY switching hock noise; discharging C₂ generates an approx. 100ms delay of MUTE SW ON/OFF-switching after REC goes to ON.

T₄: Prevents shock noise caused by abnormal key-entries; REC SIG and PLY SIG input-gates remain OFF during C₂ charging time of approx. 400ms, after REC turns to OFF.



■ OUTPUT SIGNAL

REC/PLY SW (Pin 16)

Goes to high level just following REC SIG ON, turning Rec-Amp Base-Bias and Pre-Amp SW to REC. After REC SIG turns to OFF, switches them back to PLY with a delay of T_2 .

- High Level: 10.5V typ.
- Low Level: 0V typ.
- Load Resistance: 2.4k Ω min.

MUTE SW

Supplies MUTE to the monitor output signal, using one form or more of the following three.

MUTE ON at high level.

- a) Stop MUTE: MUTE ON at STOP mode or at PLY PAUS
- b) Timing MUTE: MUTE ON during the time of T_1 or T_3 .
- c) Off-Supply MUTE: MUTE ON during a given timewhile supply is off.

DIN SW (Pin-11)

Goes to low level at PLY (except PLY PAUS) and supplies output signal into DIN Terminal.

Output signal control is provided only or PLY SIG under MUTE OFF.

Pin-6 is connected to an open-collector; when supplying 12V of external supply voltage,

- High Level: 12V typ.
- Low Level: 0.2V typ.
- Load Resistance: 470 Ω min.

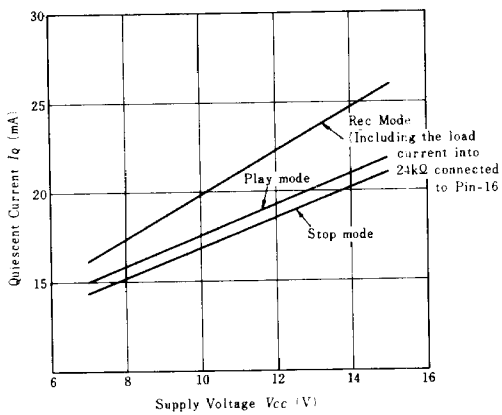
- High Level: 12V typ.
- Low Level: 0.2V typ.
- Load Resistance: 470 Ω min.

HEAD SW (Pin 6)

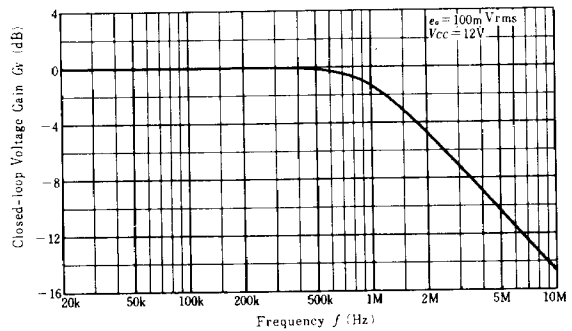
Goes to high level with a delay of T_1 after REC SIGN turns to ON, turning HEAD SW to REC. After REC SIG turns to OFF, switches head SW to PLY with a delay of T_2 .

Pin-6 is connected to an open-collector; when supplying 12V of external supply voltage,

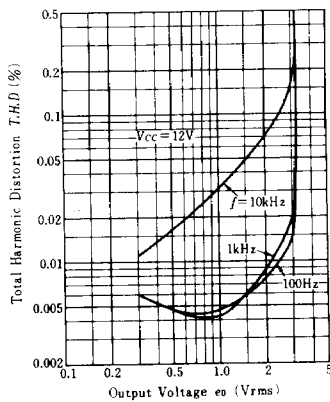
QUIESCENT CURRENT VS. SUPPLY VOLTAGE



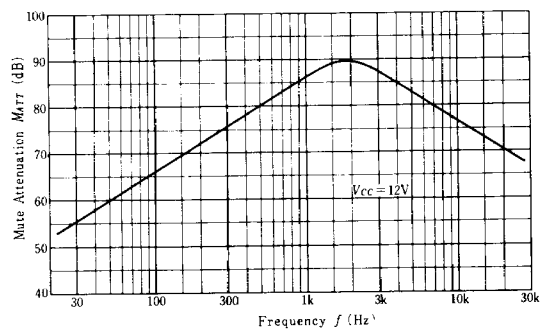
CLOSED LOOP VOLTAGE GAIN VS. FREQUENCY (MUTE AMP)



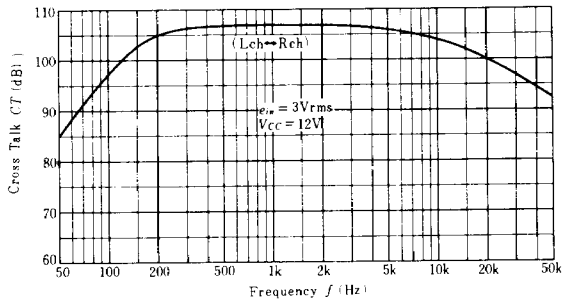
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE (MUTE AMP)



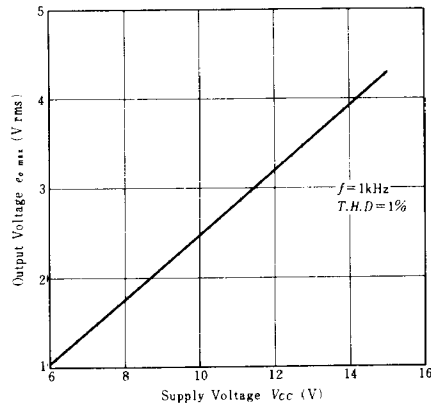
MUTE ATTENUATION VS. FREQUENCY (MUTE AMP)



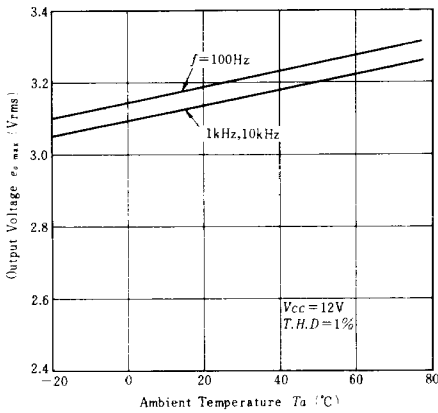
CROSS TALK VS. FREQUENCY (MUTE AMP)



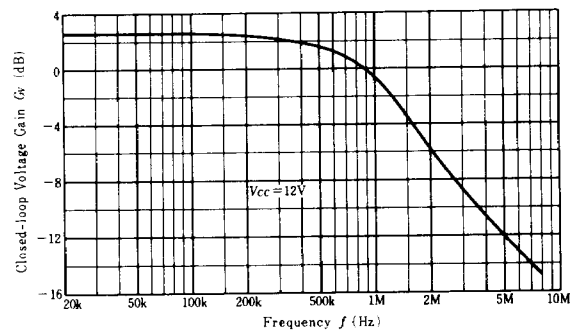
OUTPUT VOLTAGE VS. SUPPLY VOLTAGE (MUTE AMP)



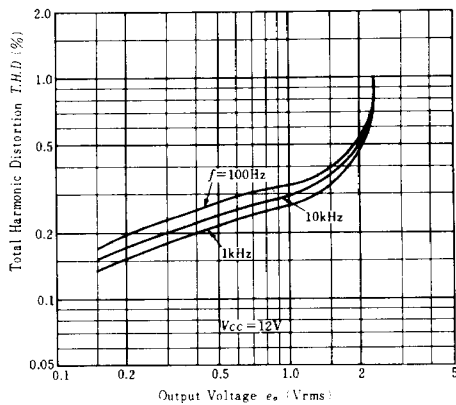
OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE (MUTE AMP)



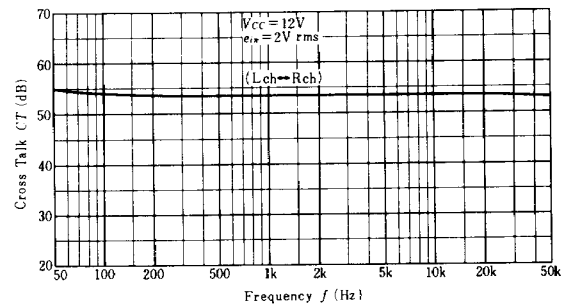
CLOSED LOOP VOLTAGE GAIN VS. FREQUENCY (HEAD PHONE AMP)



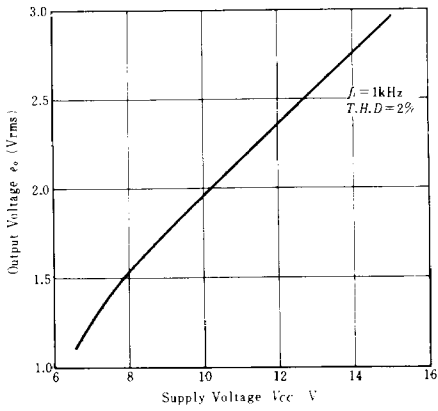
TOTAL HARMONIC DISTORTION VS. OUTPUT VOLTAGE (HEAD PHONE AMP)



CROSS TALK VS. FREQUENCY (HEAD PHONE AMP)



OUTPUT VOLTAGE VS. SUPPLY VOLTAGE (HEAD PHONE AMP)



OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE (HEAD PHONE AMP)

