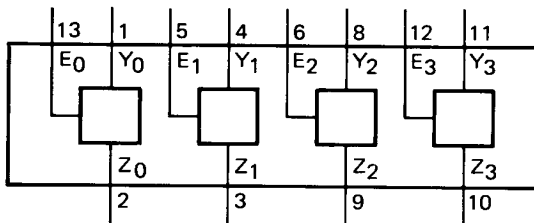


QUADRUPLE BILATERAL SWITCHES



The HEF4066B has four independent bilateral analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to V_{DD} a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to V_{SS} the switch is disabled and a high impedance between Y and Z is established (OFF condition).

The HEF4066B is pin compatible with the HEF4016B but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.



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Fig. 1 Functional diagram.

PINNING

E_0 to E_3 enable inputs

Y_0 to Y_3 input/output terminals

Z_0 to Z_3 input/output terminals

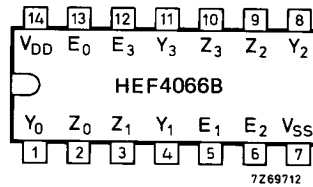


Fig. 2 Pinning diagram.

- HEF4066BP : 14-lead DIL; plastic (SOT-27).
- HEF4066BD : 14-lead DIL; ceramic (cerdip) (SOT-73).
- HEF4066BT : 14-lead mini-pack; plastic (SO-14; SOT-108A).

APPLICATION INFORMATION

An example of application for the HEF4066B is:

- Analogue and digital switching

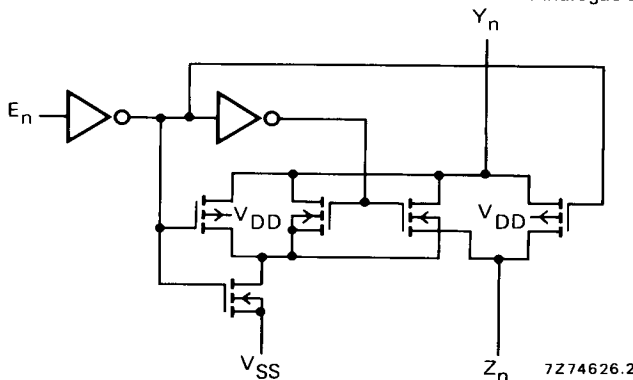


Fig. 3 Schematic diagram (one switch).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch

P max. 100 mW

For other RATINGS see Family Specifications

D.C. CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$

	V_{DD} V	symbol	min.	typ.	max.	conditions
ON resistance	5	R_{ON}	—	350	2500	} E_n at V_{DD} $V_{is} = V_{SS}$ to V_{DD} see Fig. 4
	10		—	80	245	
	15		—	60	175	
ON resistance	5	R_{ON}	—	115	340	} E_n at V_{DD} $V_{is} = V_{SS}$ see Fig. 4
	10		—	50	160	
	15		—	40	115	
ON resistance	5	R_{ON}	—	120	365	} E_n at V_{DD} $V_{is} = V_{DD}$ see Fig. 4
	10		—	65	200	
	15		—	50	155	
' Δ ' ON resistance between any two channels	5	ΔR_{ON}	—	25	—	} E_n at V_{DD} $V_{is} = V_{SS}$ to V_{DD} see Fig. 4
	10		—	10	—	
	15		—	5	—	
OFF state leakage current, any channel OFF	5	I_{OZ}	—	—	—	} E_n at V_{SS}
	10		—	—	nA	
	15		—	—	200	
E_n input voltage LOW	5	V_{IL}	—	2,25	1	} $I_{is} = 10\text{ }\mu\text{A}$ see Fig. 9
	10		—	4,50	2	
	15		—	6,75	2	

	V_{DD} V	symbol	T_{amb} ($^{\circ}\text{C}$)			conditions
			−40 max.	+25 max.	+85 max.	
Quiescent device current	5	I_{DD}	1,0	1,0	7,5	} $V_{SS} = 0$; all valid input combinations; $V_I = V_{SS}$ or V_{DD}
	10		2,0	2,0	15,0	
	15		4,0	4,0	30,0	
Input leakage current at E_n	15	$\pm I_{IN}$	—	300	1000	E_n at V_{SS} or V_{DD}

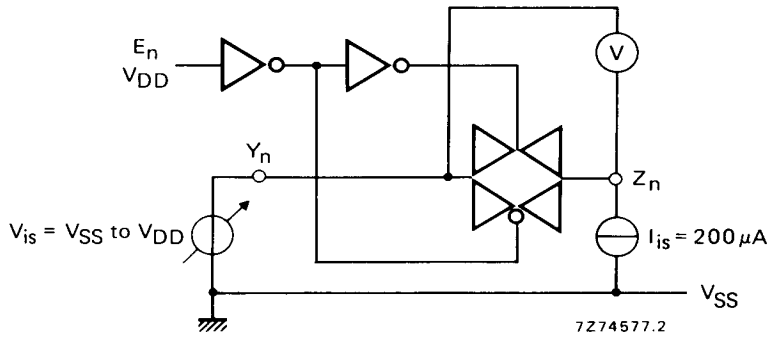


Fig. 4 Test set-up for measuring R_{ON} .

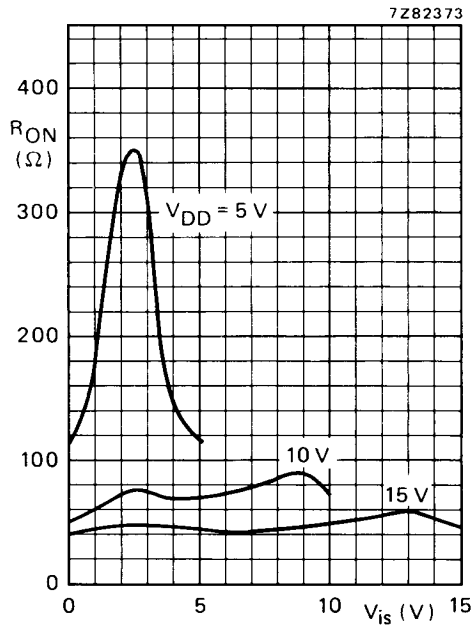


Fig. 5 Typical R_{ON} as a function of input voltage.

E_n at V_{DD}
 $I_{is} = 200 \mu A$
 $V_{SS} = 0 V$

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS} .

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	typ.	max.		
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5	tPHL	10	20	ns	} note 1
	10		5	10		
	15		5	10		
LOW to HIGH	5	tPLH	10	20	ns	} note 1
	10		5	10		
	15		5	10		
Output disable times $E_n \rightarrow V_{os}$ HIGH	5	tPHZ	80	160	ns	} note 2
	10		65	130		
	15		60	120		
LOW	5	tPLZ	80	160	ns	} note 2
	10		70	140		
	15		70	140		
Output enable times $E_n \rightarrow V_{os}$ HIGH	5	tPZH	40	80	ns	} note 2
	10		20	40		
	15		15	30		
LOW	5	tPZL	45	90	ns	} note 2
	10		20	40		
	15		15	30		
Distortion, sine-wave response	5		0,25		%	} note 3
	10		0,04			
	15		0,04			
Crosstalk between any two channels	5		—		MHz	} note 4
	10		1			
	15		—			
Crosstalk; enable input to output	5		—		mV	} note 5
	10		50			
	15		—			
OFF-state feed-through	5		—		MHz	} note 6
	10		1			
	15		—			
ON-state frequency response	5		—		MHz	} note 7
	10		90			
	15		—			
	V_{DD} V	typical formula for P (μW)			where	
Dynamic power dissipation per package (P)	5	800 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$			f_i = input freq. (MHz)	
	10	3 500 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$			f_o = output freq. (MHz)	
	15	10 100 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$			C_L = load capacitance (pF)	
					$\Sigma(f_o C_L)$ = sum of outputs	
					V_{DD} = supply voltage (V)	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.

V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 50\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$; $V_{is} = V_{DD}$ (square-wave); see Figs 6 and 10.

2. $R_L = 10\text{ k}\Omega$; $C_L = 50\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$ (square-wave);

$V_{is} = V_{DD}$ and R_L to V_{SS} for t_{pHZ} and t_{pZH} ;

$V_{is} = V_{SS}$ and R_L to V_{DD} for t_{pLZ} and t_{pZL} ; see Figs 6 and 11.

3. $R_L = 10\text{ k}\Omega$; $C_L = 15\text{ pF}$; $E_n = V_{DD}$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $f_{is} = 1\text{ kHz}$; see Fig. 7.

4. $R_L = 1\text{ k}\Omega$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);

$20 \log \frac{V_{os(B)}}{V_{is(A)}} = -50\text{ dB}$; $E_n(A) = V_{SS}$; $E_n(B) = V_{DD}$; see Fig. 8.

5. $R_L = 10\text{ k}\Omega$ to V_{SS} ; $C_L = 15\text{ pF}$ to V_{SS} ; $E_n = V_{DD}$ (square-wave); crosstalk is $\{V_{os}\}$ (peak value); see Fig. 6.

6. $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; $E_n = V_{SS}$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);

$20 \log \frac{V_{os}}{V_{is}} = -50\text{ dB}$; see Fig. 7.

7. $R_L = 1\text{ k}\Omega$; $C_L = 5\text{ pF}$; $E_n = V_{DD}$; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);

$20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$; see Fig. 7.

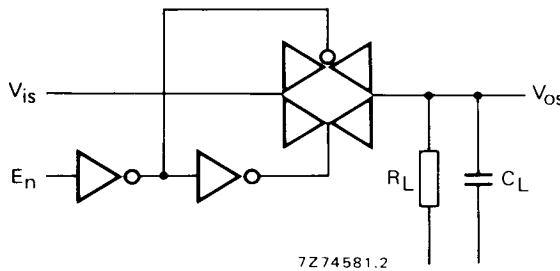


Fig. 6.

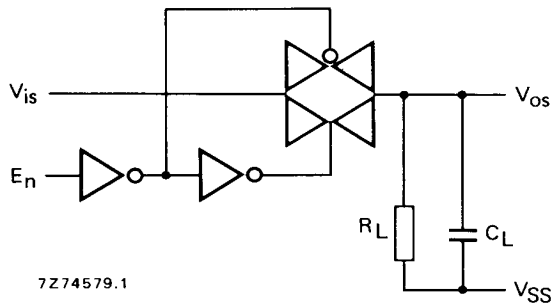


Fig. 7.

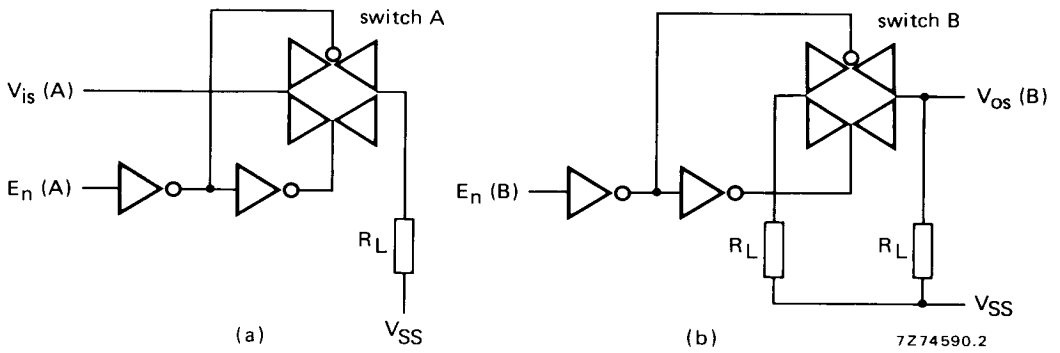


Fig. 8.

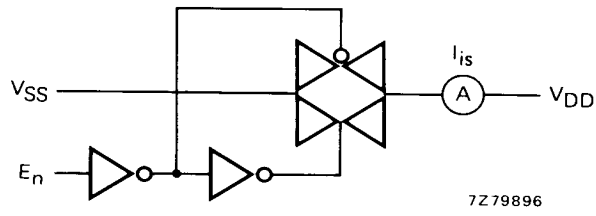


Fig. 9.

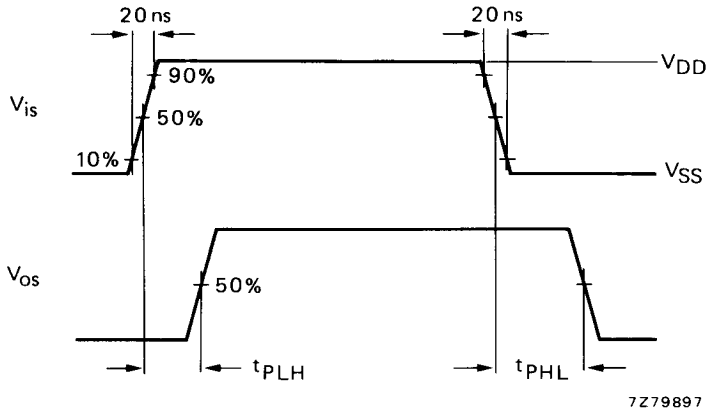
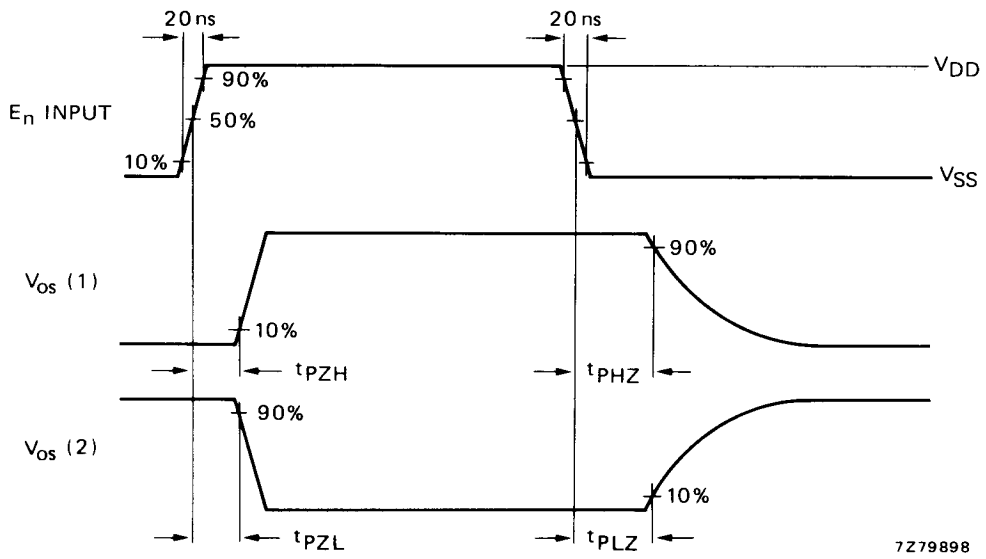


Fig. 10 Waveforms showing propagation delays from V_{is} to V_{os} .



(1) V_{is} at V_{DD} ; (2) V_{is} at V_{SS} .

Fig. 11 Waveforms showing output disable and enable times.