

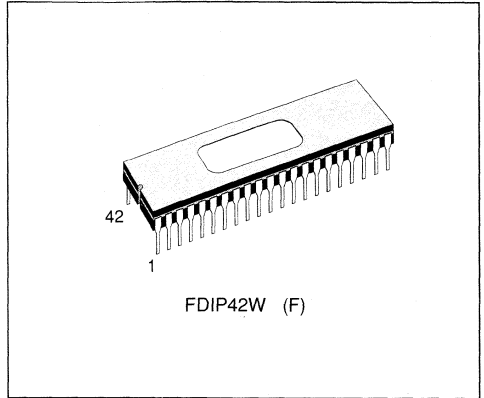
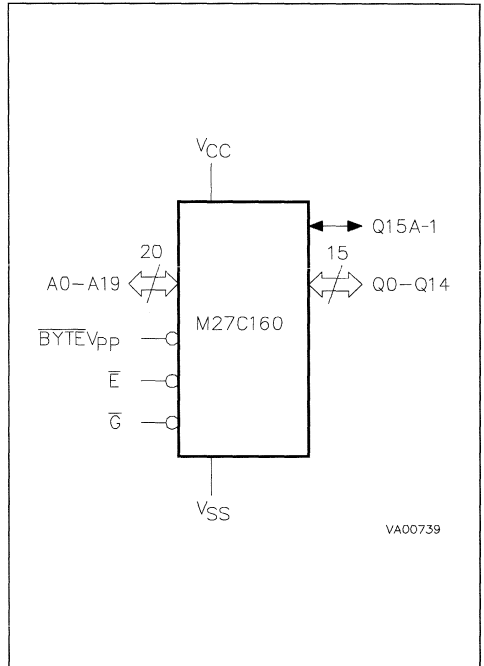
CMOS 16 Megabit (2M x 8 or 1M x 16) UV EPROM
ADVANCE DATA

- FAST ACCESS TIME: 150ns
- WORD-WIDE or BYTE-WIDE CONFIGURABLE
- 16 Megabit, 42 Pin, MASK ROM COMPATIBLE
- LOW POWER CONSUMPTION
 - Active Current 70mA at 8MHz
 - Standby Current 100µA
- PROGRAMMING VOLTAGE $12.5V \pm 0.3V$
- PROGRAMMING TIME OF AROUND 10sec. (PRESTO III ALGORITHM)

DESCRIPTION

The M27C160 is a 16 Megabit UV erasable and programmable memory (EPROM) ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 2M words of 8 bit or 1M words of 16 bit. The pin-out is compatible with a 16 Megabit Mask ROM.

The 42 pin Window Ceramic Frit-Seal package has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.


Figure 1. Logic Diagram

Table 1. Signal Names

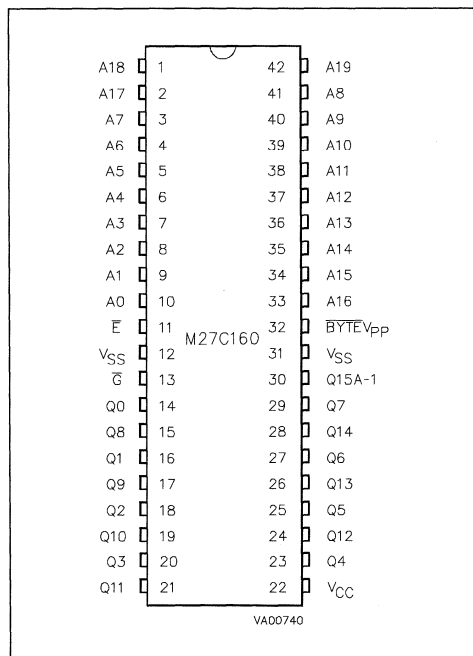
A0 - A19	Address Inputs
Q0 - Q7	Data Outputs
Q8 - Q14	Data Outputs
Q15A-1	Data Output / Address Input
\bar{E}	Chip Enable
\bar{G}	Output Enable
$\overline{BYTEV_{PP}}$	Byte Mode / Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature grade 1	0 to 70	°C
T _{BIAS}	Temperature Under Bias	-10 to 80	°C
T _{STG}	Storage Temperature	-65 to 150	°C
V _{IO}	Input or Output Voltages	-0.6 to 7	V
V _{CC}	Supply Voltage	-0.6 to 7	V
V _{A9}	A9 Voltage	-0.6 to 13.5	V
V _{PP}	Program Supply Voltage	-0.6 to 14	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DEVICE OPERATION

The operating modes of the M27C160 are listed in the Operating Modes Table. A single 5V supply is required in the read mode. All inputs are TTL compatible except for V_{PP} and 12V on A9 for the Electronic Signature.

Read Mode

The M27C160 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the BYTEV_{PP} pin. When BYTEV_{PP} is at V_{IH} the Word-wide organisation is selected and the Q15A-1 pin is used for Q15 Data Output. When the BYTEV_{PP} pin is at V_{IL} the Byte-wide organisation is selected and the Q15A-1 pin is used for the Address Input A-1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A-1 at V_{IL} the lower 8 bits of the 16 bit data are selected and with A-1 at V_{IH} the upper 8 bits of the 16 bit data are selected.

The M27C160 has two control inputs, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte-wide organisation must be selected. The E signal is the power control and should be used for device selection. The G signal is the output control and should be used to gate data to the output pins. With E=V_{IL} and G=V_{IL} the output data will be valid in a time t_{AVQV} after the all address lines are valid and stable. The Chip Enable to Output Valid time t_{ELQV} is equal to the Address Valid to output Valid time t_{AVQV}. When the Addresses are valid and E=V_{IL}, the output data is valid after a time of t_{GLQV} from the falling edge of the Output Enable signal.

Standby Mode

The M27C160 has a standby mode which reduces the active current from 50mA (f = 5MHz) to 100µA. The standby mode is entered by applying a CMOS high level V_{CC} -0.2V to E. When in the standby mode the outputs are in an high impedance state, independant of the G input level.

Table 3. Operating Modes

Mode	\bar{E}	\bar{G}	$\overline{\text{BYTEV}}_{PP}$	A9	Q0 - Q7	Q8 - Q14	Q15A-1
Read Word-wide	V_{IL}	V_{IL}	V_{IH}	X	Data Out	Data Out	Data Out
Read Byte-wide Upper	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IH}
Read Byte-wide Lower	V_{IL}	V_{IL}	V_{IL}	X	Data Out	Hi-Z	V_{IL}
Output Disable	V_{IL}	V_{IH}	X	X	Hi-Z	Hi-Z	Hi-Z
Program	V_{IL} Pulse	V_{IH}	V_{PP}	X	Data In	Data In	Data In
Verify	X	V_{IL}	V_{PP}	X	Data Out	Data Out	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	X	Hi-Z	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	Codes	Codes	Code

Notes: X = V_{IH} or V_{IL} , $V_{ID} = 12V \pm 0.5V$

Table 4. Electronic Signature

Identifier	A0	Q7 or Q15	Q6 or Q14	Q5 or Q13	Q4 or Q12	Q3 or Q11	Q2 or Q10	Q1 or Q9	Q0 or Q8	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	1	0	1	1	0	0	0	1	B1h

Table 5. Read Mode DC Characteristics ⁽¹⁾

($T_A = 0$ to 70°C ; $V_{CC} = 5V \pm 5\%$ or $5V \pm 10\%$; $V_{PP} = V_{CC}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		± 1	μA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		± 10	μA
I_{CC}	Supply Current	$\bar{E} = V_{IL}, \bar{G} = V_{IL}, f = 8\text{Mhz}$		70	mA
I_{CC}	Supply Current	$\bar{E} = V_{IL}, \bar{G} = V_{IL}, f = 5\text{MHz}$		50	mA
I_{CC1}	Supply Current (Standby) TTL	$\bar{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\bar{E} > V_{CC} - 0.2V$		100	μA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		10	μA
I_{OS}	Output Short Circuit Current	Note 2 and 3		100	mA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$		0.4	V
V_{OH}	Output High Voltage TTL	$I_{OH} = -400\mu\text{A}$	2.4		V

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP} .

2. This parameter is sampled only and not tested 100%.

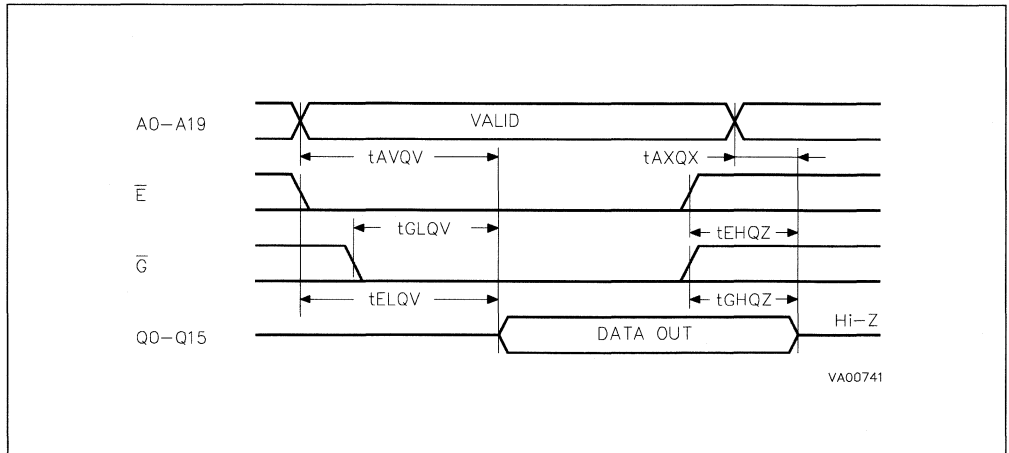
3. Output shortcircuited for no more than one second. No more than one output shorted at a time.

Table 6. Read Mode AC Characteristics (1)
 (TA = 0 to 70 °C; VCC = 5V ± 5% or 5V ± 10%; VPP = VCC)

Symbol	Alt	Parameter	Test Condition	M27C160				Unit
				-150		-200		
				Min	Max	Min	Max	
tAVQV	tACC	Address Valid to Output Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		150		200	ns
tBHQV	tST	BYTE High to Output Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		150		200	ns
tELQV	tCE	Chip Enable Low to Output Valid	$\bar{G} = V_{IL}$		150		200	ns
tGLQV	tOE	Output Enable Low to Output Valid	$\bar{E} = V_{IL}$		60		70	ns
tBLQZ (2)	tSTD	BYTE Low to Output Hi-Z	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		50		60	ns
tEHQZ (2)	tDF	Chip Enable High to Output Hi-Z	$\bar{G} = V_{IL}$	0	50	0	60	ns
tGHQZ (2)	tDF	Output Enable High to Output Hi-Z	$\bar{E} = V_{IL}$	0	50	0	60	ns
tAXQX	tOH	Address Transition to Output Transition	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$	5		5		ns
tBLQX	tOH	BYTE Low to Output Transition	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$	5		5		ns

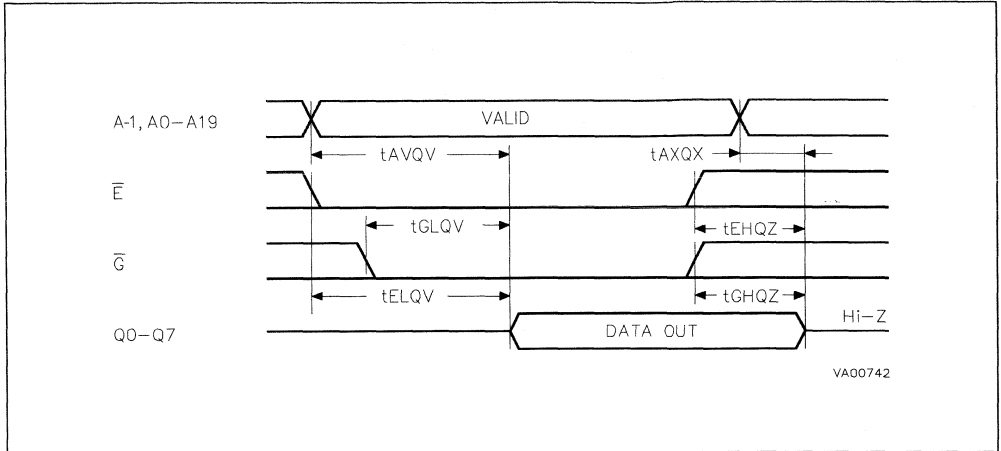
Notes: 1. VCC must be applied simultaneously with or before VPP and removed simultaneously or after VPP.
 2. This parameter is sampled only and not 100% tested.

Figure 3. Word-Wide Read Mode AC Waveforms



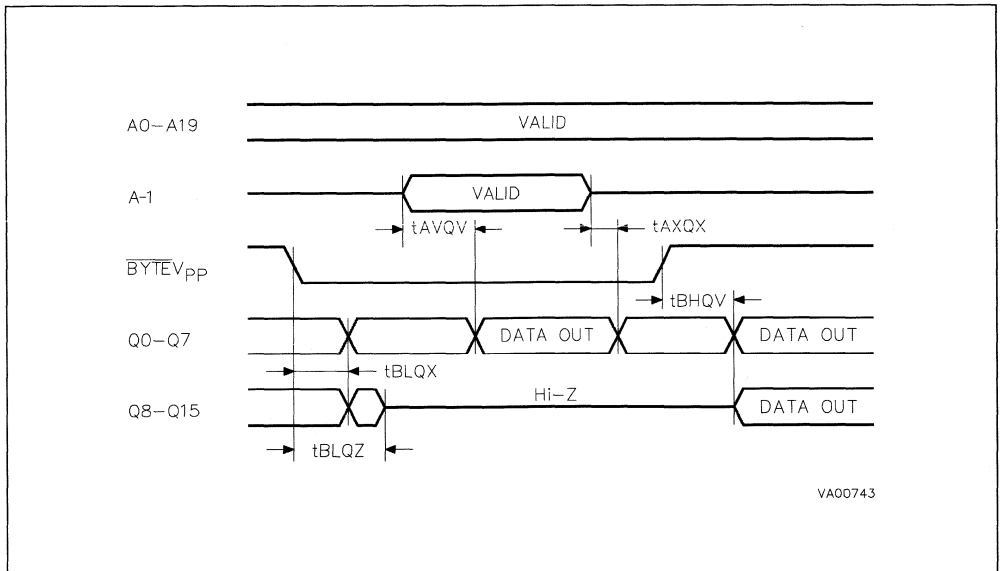
Note: BYTEVPP = VIH

Figure 4. Byte-Wide Read Mode AC Waveforms



Note: $\overline{BYTEV_{PP}} = V_{IL}$

Figure 5. \overline{BYTE} Transition AC Waveforms



Note: \overline{E} and $\overline{G} = V_{IL}$

AC Measurement Conditions

Input Rise and Fall Times < 20ns
 Input Pulse Voltages 0.4V to 2.4V
 Input and Output Timing Ref. Voltages 0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 6. AC Testing Input Output Waveforms

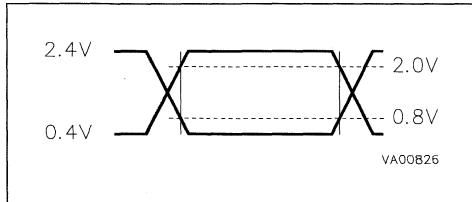


Figure 7. AC Testing Load Circuit

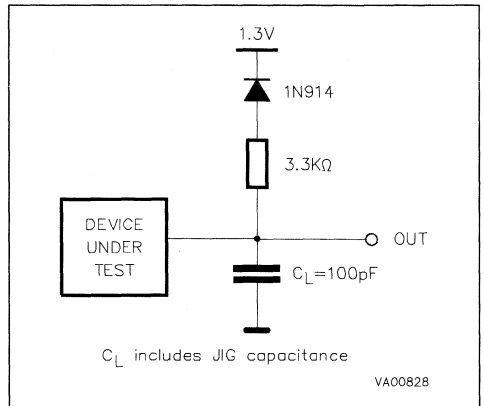


Table 7. Capacitance ($T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (except \overline{BYTEV}_{PP})	$V_{IN} = 0V$		10	pF
	Input Capacitance (\overline{BYTEV}_{PP})	$V_{IN} = 0V$		120	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		12	pF

Note: This parameter is sampled only and not tested 100%.

Table 8. Programming Mode DC Characteristics ⁽¹⁾

($T_A = 25\text{ }^\circ\text{C}$; $V_{CC} = 6.25V \pm 0.25V$; $V_{PP} = 12.5V \pm 0.3V$)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$		± 1	μA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2.4	$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$		0.4	V
V_{OH}	Output High Voltage TTL	$I_{OH} = -2.5mA$	3.5		V
V_{ID}	A9 Voltage		11.5	12.5	V

Note: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

Table 9. Programming Mode AC Characteristics ⁽¹⁾
 ($T_A = 25\text{ }^\circ\text{C}$; $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$; $V_{PP} = 12.5\text{V} \pm 0.3\text{V}$)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
$t_{A\text{VEL}}$	t_{AS}	Address Valid to Chip Enable Low		2		μs
$t_{Q\text{VEL}}$	t_{DS}	Input Valid to Chip Enable Low		2		μs
$t_{V\text{PHAV}}$	t_{VPS}	V_{PP} High to Address Valid		2		μs
$t_{V\text{CHAV}}$	t_{VCS}	V_{CC} High to Address Valid		2		μs
$t_{E\text{LEH}}$	t_{PW}	Chip Enable Program Pulse Width		9.5	10.5	μs
$t_{E\text{HQX}}$	t_{DH}	Chip Enable High to Input Transition		2		μs
$t_{Q\text{XGL}}$	t_{OES}	Input Transition to Output Enable Low		2		μs
$t_{G\text{LQV}}$	t_{OE}	Output Enable Low to Output Valid			120	ns
$t_{G\text{HQZ}}^{(2)}$	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
$t_{G\text{HAX}}$	t_{AH}	Output Enable High to Address Transition		0		ns

Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

2. This parameter is sampled only and not 100% tested.

Figure 8. Programming and Verify Modes AC Waveforms

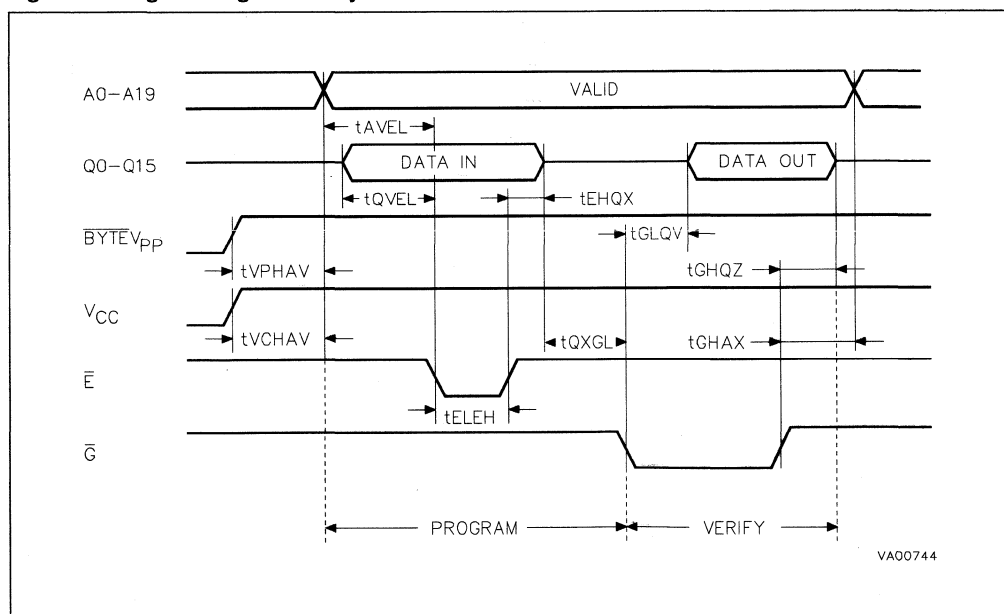
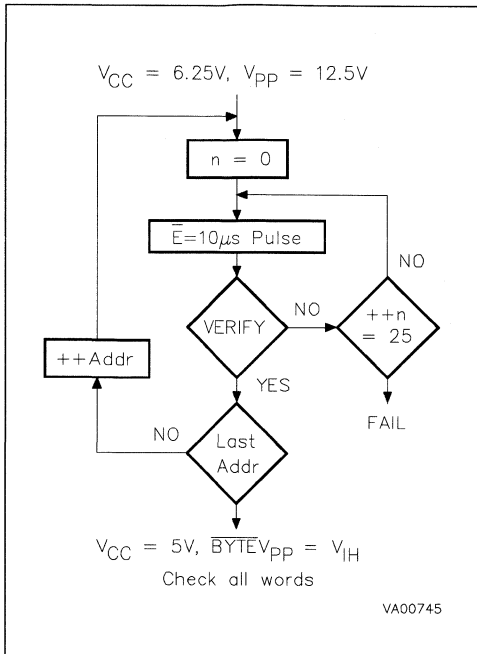


Figure 9. Programming Flowchart



Output Disable Mode

When EPROMs are used in memory arrays two line output control should be used. This function uses the output disable mode which allows:

- the lowest possible power consumption
- complete assurance that output bus contention will not occur

For the best use of the two control lines \bar{E} and \bar{G} , the input \bar{E} should be decoded and used as the primary selection, while \bar{G} should be made a common connection to all memories in the array. \bar{G} should be connected to the \bar{READ} signal of the system bus. This will ensure that all deselected devices are in the low power standby mode and that the output lines are only active when data is required from a particular memory device.

System Considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the supplies to the devices. The supply current I_{CC} has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of \bar{E} .

The magnitude of the transient current peaks is dependant on the capacitive and inductive loading of the device outputs. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a $1\mu\text{F}$ ceramic capacitor is used on every device between V_{CC} and V_{SS} . This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a $4.7\mu\text{F}$ electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. This capacitor should be mounted near the power supply connection point. The purpose of this capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Programming

When first delivered, and after erasure for UV EPROMs, all bits are in the "1" logic state (Output High). Data with both "1's" and "0's" is applied and the "0s" are programmed into the memory array. For programming V_{CC} is raised to 6.25V. The M27C160 is in the Program Mode when V_{PP} is at 12.75V, \bar{G} is at V_{IH} and \bar{E} is pulsed to V_{IL} . Data to be programmed is applied 16 bits in parallel to the data output pins Q0 - Q15.

PRESTO III Algorithm

The PRESTO III Algorithm allows the whole 16 Megabit array to be programmed with a guaranteed margin in a typical time of less than 10 seconds. The algorithm applies a series of $10\mu\text{s}$ program pulses to each word until a correct verify is made. During programming and verify a MARGIN MODE circuit is automatically activated to guarantee that each cell is programmed with an adequate margin. No overprogram pulse is applied since the verify in MARGIN MODE provides the necessary threshold margin for each cell.

Program Inhibit

Multiple M27C160s may be programmed in parallel with different data. This is done by putting in parallel all inputs except \bar{E} and \bar{G} . With V_{CC} at 6.25V and V_{PP} at 12.5V, data should be applied to all devices and \bar{G} placed at V_{IH} . Low level pulses on the \bar{E} of one device will program that device.

Program Verify

After each program pulse a verify read is made by reading the data output with V_{CC} at 6.25V, V_{PP} at 12.5V and \bar{G} placed at V_{IL} .

Electronic Signature

The Electronic Signature Mode allows a binary code to be read from the EPROM which identifies the Manufacturer and Device Type. These codes are intended to be used to match the programming

equipment to the device being programmed and its corresponding algorithm.

The Electronic Signature Mode is activated by applying a voltage V_{ID} of 12V to the Address line A9 and V_{IL} to all other Address lines, with \bar{E} and \bar{G} at V_{IL} and BYTE at V_{IH} . The identifier bytes may be read from either Q0-Q7 or Q8-Q15. With Address line A0 at V_{IL} the byte output is the Manufacturer's code, with A0 at V_{IH} the byte identifies the Device Type. The codes for the SGS-THOMSON M27C160 are shown in the table.

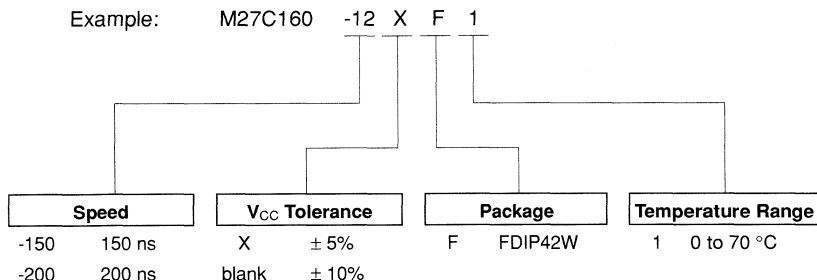
Erasure

The erasure of the M27C160 begins when the cells are exposed to light of wavelengths shorter than approximately 4000 Å. Sunlight and some types of fluorescent lamps have wavelengths in the 3000 -

4000 Å range. Constant exposure to room level fluorescent lighting could erase a typical EPROM in about 3 years, while it takes approximately 170 hours to cause erasure when exposed to direct sunlight. To prevent accidental erasure it is recommended that opaque labels be placed over the M27C160 window.

The erase procedure for the M27C160 is exposure to UV light with a wavelength of 2537 Å. The integrated dose (UV intensity x time) for erasure should be a minimum of 15 W-sec/cm². The erase time with this dosage is 15 to 20 minutes using an UV lamp with 12,000 μW/cm² rating. The M27C160 should be placed within 2.5cm of the lamp tube during erasure. No filter should be used on the lamp.

ORDERING INFORMATION



For a list of available options of Speed, V_{CC} Tolerance, Package and Temperature Range refer to the Selector Guide in this Data Book or the current Memory Shortform that will be periodically up-dated.

For further information on any aspect of this device, please contact our Sales Office nearest to you.