FUJITSU

NMOS INPUT/OUTPUT EXPANDER

MBL 8243

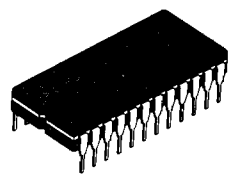
April 1986
Edition 2.1

NMOS INPUT/OUTPUT EXPANDER

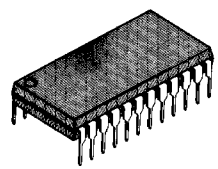
The Fujitsu MBL 8243 is an input/output expander designed specifically to provide a low cost means of I/O expansion for the MBL 8048 series of single-chip microcomputers. Fabricated in 5 volts NMOS, the MBL 8243 combines low cost single supply voltage and high drive current capability. Also, the MBL 8243 is packaged in a 24-pin cerdip or plastic DIP package.

The MBL 8243 consists of four 4-bit bidirectional static I/O ports and one 4-bit port which serves as an interface to the MBL 8048 series microcomputers. The 4-bit interface requires that only 4 I/O lines of the MBL 8048/8049/80C49/8749 be used for I/O expansion, and also allows multiple MBL 8243's to be added to the same bus.

The I/O ports of the MBL 8243 serve as a direct extension of the resident I/O facilities of the MBL 8048 series microcomputers and are accessed by their own MOVD, ANLD, and ORLD instructions.



CERAMIC DIP
DIP-24C-C01

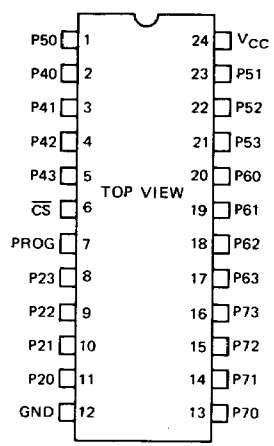


PLASTIC DIP
DIP-24P-M01

FEATURES

- Simple Interface to Fujitsu MBL 8048 Series and Intel MCS-48*
- Four 4-Bit I/O Ports.
- AND and OR Directly to Ports.
- High Current Drive: 5 mA at 0.45 V
  20 mA at 1.0 V
- On-Chip Power-On Reset Circuit.
- Single +5 V Power Supply.
- N-Channel Silicon-Gate E/D MOS Process.
- Two Package Options:
  —Standard 24-pin Cerdip (Suffix: Z)
  —Standard 24-pin Plastic DIP (Suffix: M)
- Pin-Compatible with Intel 8243 and Fujitsu MBL 82C43.

Fig. 1 – PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 2 – LOGIC SYMBOL

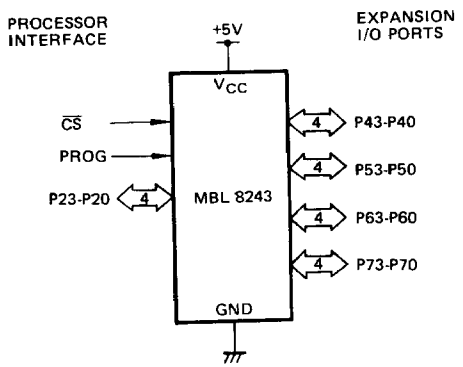
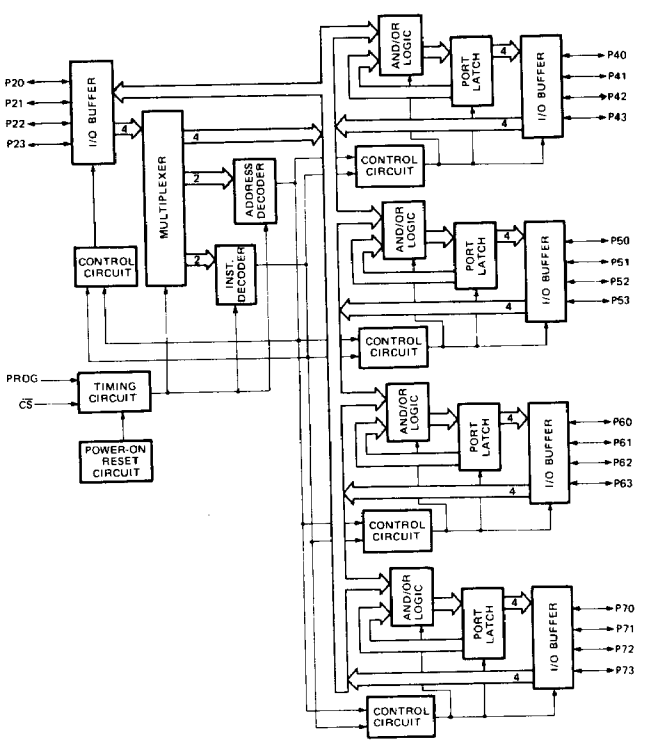


Fig. 3 – BLOCK DIAGRAM



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PIN DESCRIPTION

The MBL 8243 has two interfaces: One is the processor interface; $\overline{CS}$, PROG, and Port 2, which are used for the processor to communicate with the MBL 8243 device. Another is the expansion I/O ports; Ports 4, 5, 6, and 7, which serve as an expansion of the processor's I/O.

Table 1—Pin Description

Symbol	Pin No.	Type	Function
V_{CC}	24	–	+5 V supply.
GND	12	–	0 V supply.
$\overline{CS}$	6	I	Chip Select input: A high on $\overline{CS}$ inhibits any change of output or internal status.
PROG	7	I	Clock input: A high-to-low transition on PROG signifies that address and control are available on P20–P23, and a low-to-high transition signifies that data is available on P20–P23.
P20 – P23	11 to 8	I/O	Port 2: Four (4) bit bi-directional port contains the address and control bits on a high-to-low transition of PROG. During a low-to-high transition contains the data for a selected output port if a write operation, or the data from a selected port before the low-to-high transition if a read operation.
P40 – P43 P50 – P53 P60 – P63 P70 – P73	2 to 5 1, 23 to 21 20 to 17 13 to 16	I/O	Ports 4, 5, 6, and 7: Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write), or a tri-state (after read). Data on pins P20–P23 may be directly written, ANDed or ORed with previous data.

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The MBL 8243 contains four 4-bit I/O ports which serve as an extension of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

- Transfer Accumulator to Port.
- Transfer Port to Accumulator.
- AND Accumulator to Port.
- OR Accumulator to Port.

All communication between the MBL 8048 series and the MBL 8243 occurs over Port 2 (P20—P23) with timing provided by an output pulse on the PROG pin of the processor. Each transfer consists of two 4-bit nibbles:

The first containing the "op code" and port address and the second containing the actual 4-bits of data. A high-to-low transition of the PROG line indicates that address is present while a low-to-high transition indicates the presence of data. Additional MBL 8243's may be added to the 4-bit bus and chip selected using additional output lines from the MBL 8048 series microcomputers.

POWER ON INITIALIZATION

Initial application of power to the device forces input/output ports 4, 5, 6, and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high-to-low transition of PROG causes device to exit power on mode. The power on sequence is initiated if V_{CC} drops below 1 V.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

WRITE MODES

The device has three write modes. MOVD Pi, A directly writes new data into the selected port and old data is lost. ORLD Pi, A takes new data, OR's it with the old data and then writes it to the port. ANLD Pi, A takes new data, AND's it with the old data and then writes it to the port. Operation code and port address are latched from the input port 2 on the high-to-low transition of the PROG pin. On the low-to-high transition of PROG data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulation is performed, the data is latched and outputed. The old data remains latched until new valid outputs are entered.

READ MODE

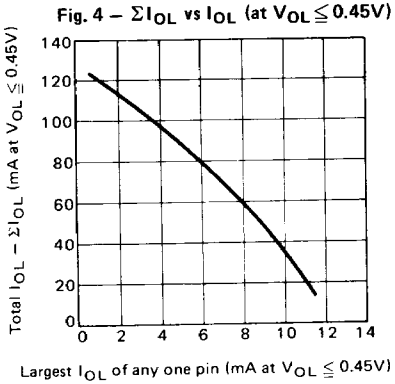
The device has one read mode. The operation code and port address are latched from the input port 2 on the high-to-low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated, and the input buffers switched on. The read operation is terminated by a low-to-high transition of the PROG pin. The port (4, 5, 6 or 7) that was selected is switched to the tri-stated mode while port 2 is returned to the input mode.

Normally, a port will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the MBL 8243 output. A read of any port will leave that port in a high impedance state.

SINK CAPABILITY

The MBL 8243 can sink 5 mA at 0.45 V on each of its 16 I/O lines simultaneously. If, however, all lines are not sinking simultaneously or all lines are not fully loaded, the drive capability of any individual line increases as is shown by the accompanying curve.

Fig. 4 – ΣI_{OL} vs I_{OL} (at $V_{OL} \leq 0.45V$)



For example, if only 5 of the 16 lines are to sink current at one time, the curve shows that each of those 5 lines is capable of sinking 9 mA at 0.45 V (if any lines are to sink 9 mA the total I_{OL} must not exceed 45 mA or five 9 mA loads).

Example: How many pins can drive 5 TTL loads (1.6 mA) assuming remaining pins are unloaded?

I_{OL} = 5 x 1.6 mA = 8 mA
ΣI_{OL} = 60 mA from curve
pins = 60 mA ÷ 8 mA/pin = 7.5 = 7

In this case, 7 lines can sink 8 mA for a total of 56 mA. This leaves 4 mA sink current capability which can be divided in any way among the remaining 8 I/O lines of the MBL 8243.

Example: This example shows how the use of the 20 mA sink capability of Port 7 affects the sinking capability of the other I/O lines.

An MBL 8243 will drive the following loads simultaneously.

2 loads – 20 mA at 1 V (port 7 only)
8 loads – 4 mA at 0.45 V
6 loads – 3.2 mA at 0.45 V
Is this within the specified limits?

ΣI_{OL} = (2 x 20) + (8 x 4) + (6 x 3.2) = 91.2 mA. From the curve: for I_{OL} = 4 mA. $\Sigma I_{OL} \approx$ 93 mA. since 91.2 mA < 93 mA the loads are within specified limits.

Although the 20 mA at 1 V loads are used in calculating ΣI_{OL}, it is the largest current required at 0.45 V which determines the maximum allowable ΣI_{OL}.

TYPICAL APPLICATION

Fig. 5 – I/O EXPANDER INTERFACE

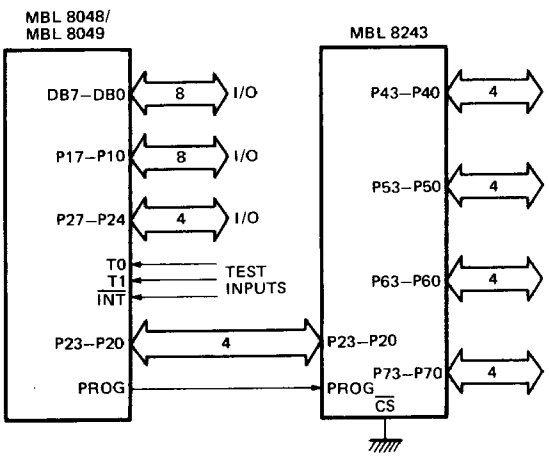
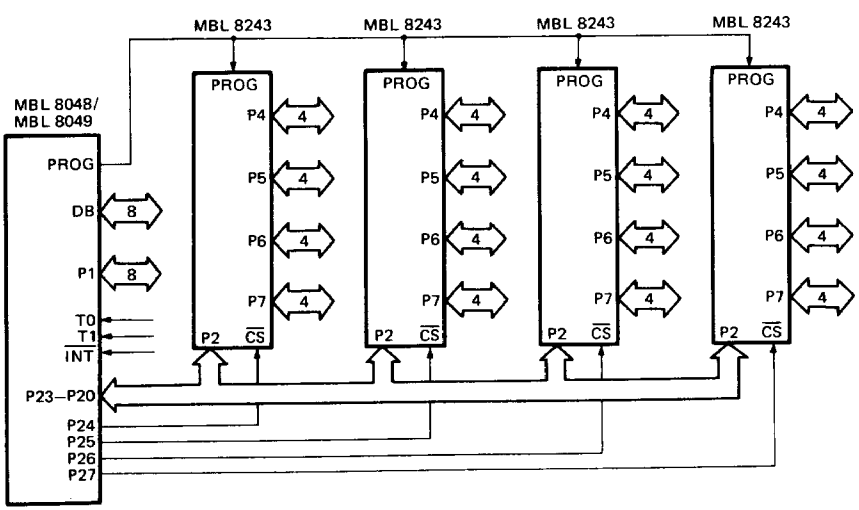


Fig. 6 – MULTIPLE I/O EXPANDER INTERFACE



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	GND−0.3 to GND+7.0	V
Input Voltage	V_{IN}	GND−0.3 to GND+7.0	
Ambient Temperature under Bias	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	
Power Dissipation	P_D	1	W

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+5 ± 10%	V
	GND	0	
Operating Temperature	T_A	0 to +70	°C

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, GND = 0V, T_A = 0°C to +70°C)

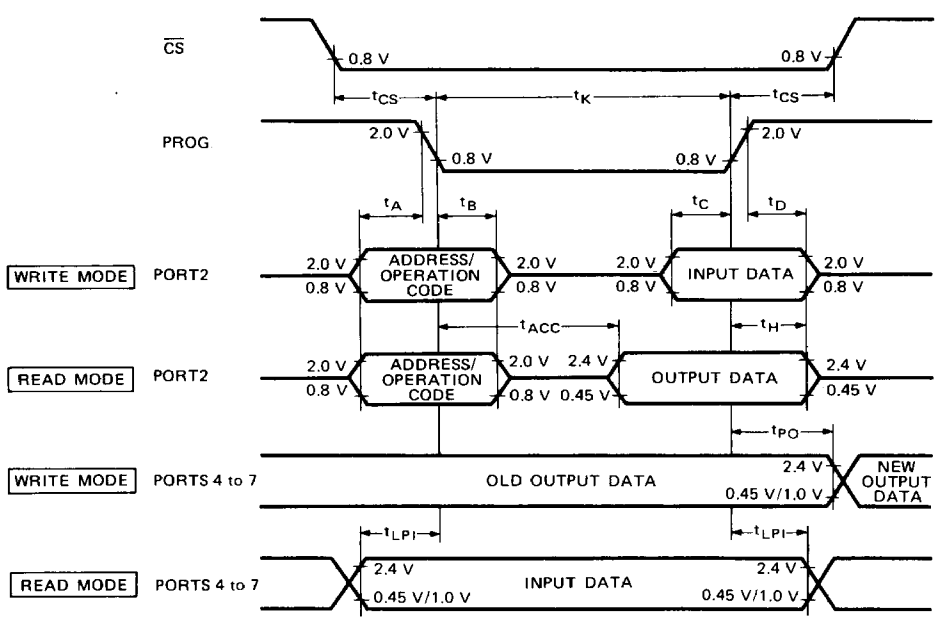
Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Input Low Voltage	V_{IL}		GND−0.3		0.8	V
Input High Voltage	V_{IH}		2.0		V_{CC}+0.3	V
Output Low Voltage	V_{OL1}	Ports 4 to 7 I_{OL} = 5mA			0.45	V
	V_{OL2}	Ports 4 to 7 I_{OL} = 20mA			1.0	V
	V_{OL3}	Port 2 I_{OL} = 0.6mA			0.45	V
Output High Voltage	V_{OH1}	Ports 4 to 7 I_{OH} = −240μA	2.4			V
	V_{OH2}	Port 2 I_{OH} = −100μA	2.4			V
Input Leakage Current	I_{IL1}	Ports 4 to 7 GND≦ V_{IN} ≦ V_{CC}	-10		20	μA
	I_{IL2}	Port 2, $\overline{CS}$, PROG GND≦ V_{IN} ≦ V_{CC}	-10		10	μA
Total I_{OL} of 16 Output	ΣI_{OL}	I_{OUT}=5mA at each pin of Ports 4 to 7			80	mA
Supply Current	I_{CC}			10	20	mA

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, GND = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Address/Operation Code Setup Time	t_A	C_L = 80pF	100			ns
Address/Operation Code Hold Time	t_B	C_L = 20pF	60			ns
Data Setup Time	t_C	C_L = 80pF	200			ns
Data Hold Time	t_D	C_L = 20pF	20			ns
Port 2 Floating Time	t_H	C_L = 20pF	0		150	ns
PROG Pulse Width	t_K		700			ns
$\overline{CS}$ Setup/Hold Times	t_{CS}		50			ns
Ports 4 to 7 Output Delay Time	t_{PO}	C_L = 100pF			700	ns
Ports 4 to 7 Setup/Hold Times	t_{LPI}		100			ns
Port 2 Output Delay Time	t_{ACC}	C_L = 80pF			650	ns

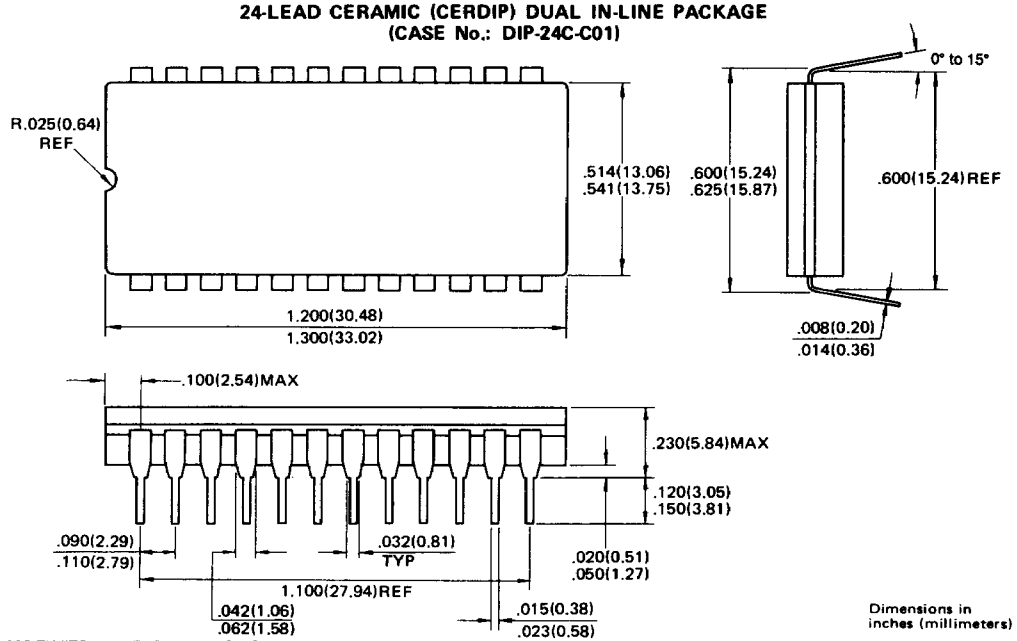
Fig. 7 – TIMING DIAGRAM



PACKAGE DIMENSIONS

CERAMIC DIP (Suffix: Z)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C01)



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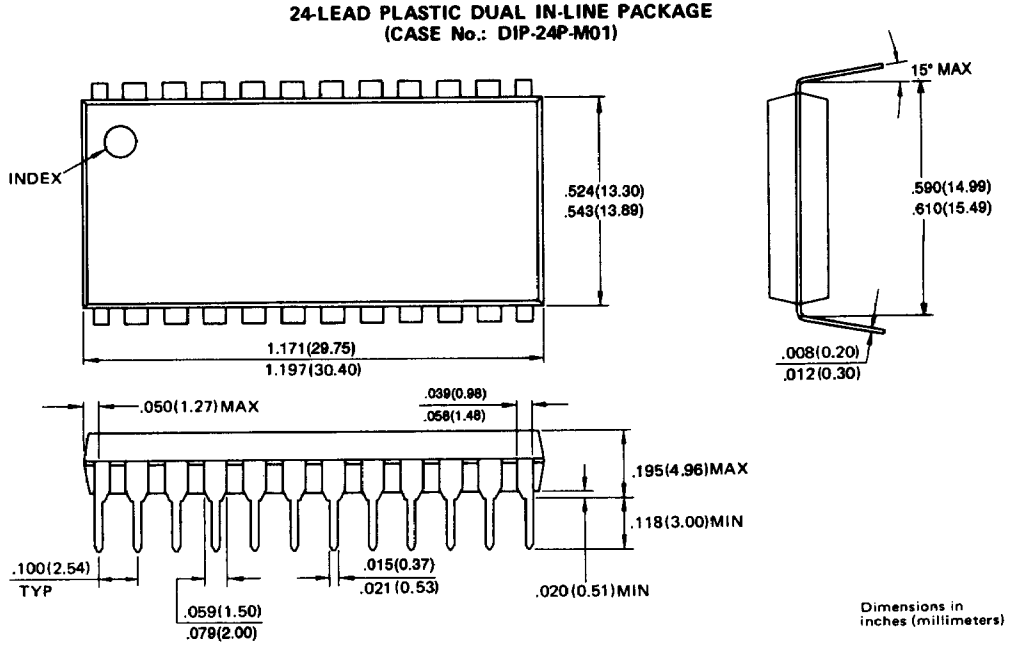
PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: M)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M01)



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