



**MOTOROLA**

# Quad Line Receivers

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

- Input Resistance – 3.0 k to 7.0 k $\Omega$
- Input Signal Range –  $\pm 30$  V
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

### ORDERING INFORMATION

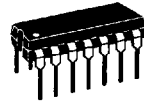
Device	Operating Temperature Range	Package
MC1489P, AP	$T_A = 0$ to $+75^\circ\text{C}$	Plastic
MC1489D, AD		SO-14

## MC1489, A

### QUAD MDTL LINE RECEIVERS EIA-232D

#### SEMICONDUCTOR TECHNICAL DATA

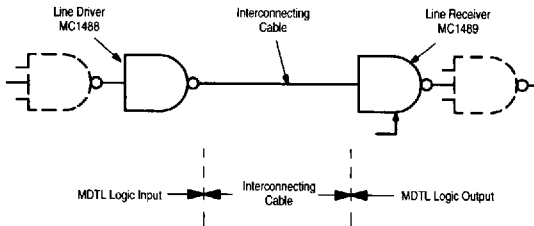
**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646



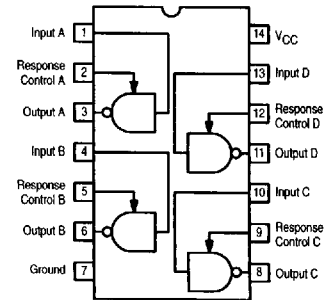
**D SUFFIX**  
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CASE 751A  
(SO-14)

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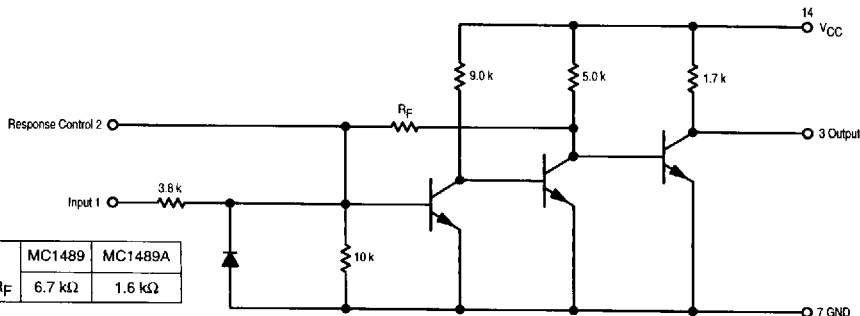
### Simplified Application



### PIN CONNECTIONS



### Representative Schematic Diagram (1/4 of Circuit Shown)





# MC1489, A

## TYPICAL CHARACTERISTICS

( $V_{CC} = 5.0$  Vdc,  $T_A = +25^\circ\text{C}$ , unless otherwise noted)

Figure 3. Input Current

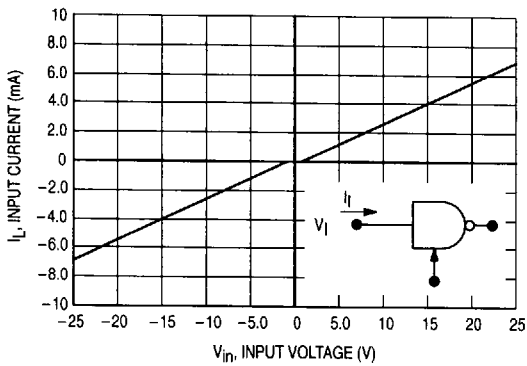


Figure 4. MC1489 Input Threshold Voltage Adjustment

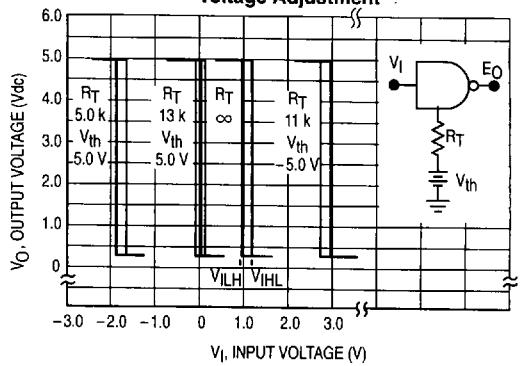


Figure 5. MC1489A Input Threshold Voltage Adjustment

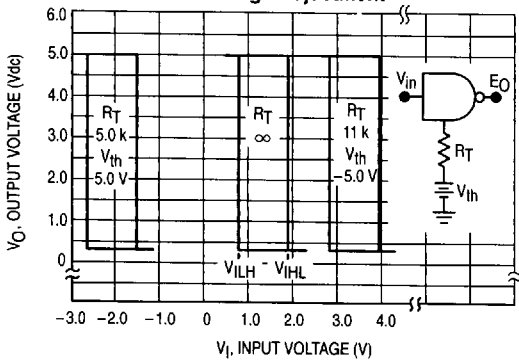


Figure 6. Input Threshold Voltage versus Temperature

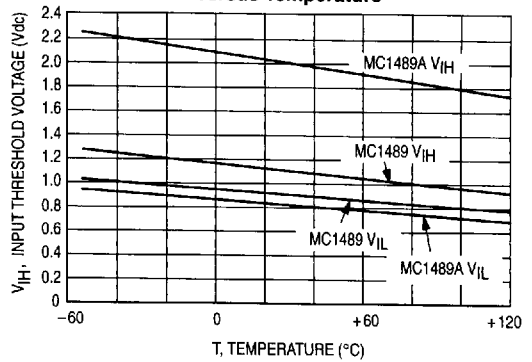
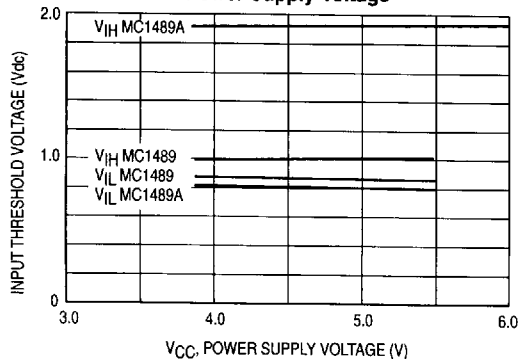


Figure 7. Input Threshold versus Power Supply Voltage



# MC1489, A

## APPLICATIONS INFORMATION

### General Information

The Electronic Industries Association (EIA) has released the EIA-232D specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232D defined levels. The EIA-232D requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000  $\Omega$  and 7000  $\Omega$  for input voltages between 3.0 and 25 V in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one  $V_{BE}$ .

The receiver shall detect a voltage between - 3.0 and - 25 V as a Logic "1" and inputs between 3.0 and 25 V as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300  $\Omega$  or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

### Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical

turn-on voltage of 1.25 V and turn-off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 V and turn-off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high frequency, high energy noise pulses. Figures 8 and 9 show typical noise pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels (see Figure 10).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the EIA-232D impedance requirement.

Figure 8. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

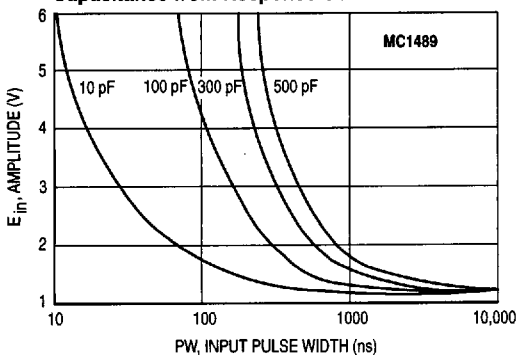
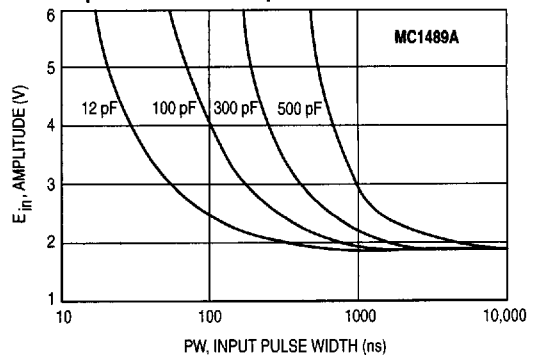


Figure 9. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND



# MC1489, A

Figure 10. Typical Translator Application – MOS to DTL or TTL

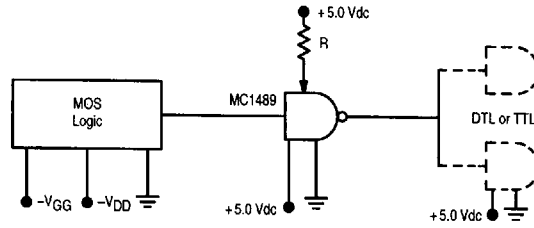
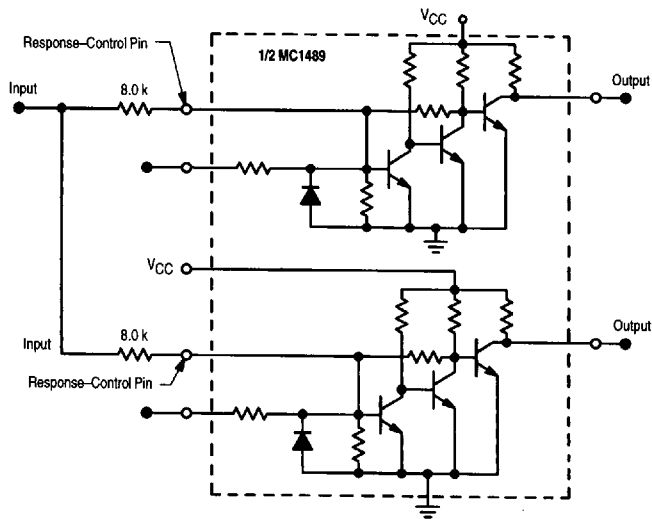


Figure 11. Typical Paralleling of Two MC1489, A Receivers to Meet EIA-232D



7