MOTOROLA

MC54/74HC160
MC54/74HC161
MC54/74HC162
MC54/74HC163

Advance Information

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

PRESETTABLE COUNTERS

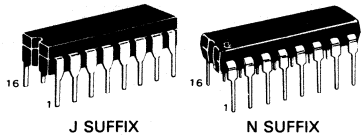
2

PRESETTABLE COUNTERS

The MC54/74HC160 through HC163 are identical in pinout to the LS160 through LS163, respectively. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC160 and HC162 are programmable BCD counters with asynchronous and synchronous Reset inputs, respectively. The HC161 and HC163 are programmable 4-bit binary counters with asynchronous and synchronous Reset, respectively.

- Synchronous or Asynchronous Reset
- Synchronous Counting and Loading
- Two Count-Enable Inputs for High-Speed Synchronous Cascading
- Rising-Edge-Triggered Operation
- Low Power Consumption Characteristic of CMOS Devices
- Output Drive Capability: 10 LSTTL Loads Minimum
- Operating Speeds Similar to LSTTL
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum (74HC Series)
- High Noise Immunity Characteristic of CMOS Devices
- Diode Protection on All Inputs



J SUFFIX
CERAMIC PACKAGE
CASE 620

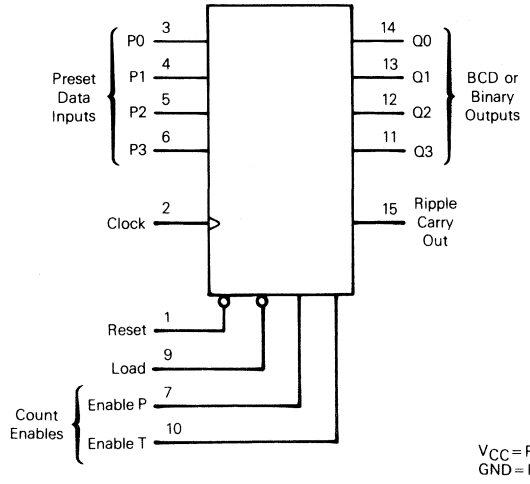
N SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

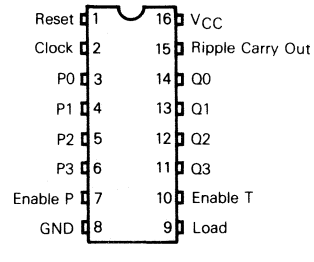
54 Series: −55°C to +125°C
MC54HCXXXJ (Ceramic Package Only)

74 Series: −40°C to +85°C
MC74HCXXXN (Plastic Package)
MC74HCXXXJ (Ceramic Package)

BLOCK DIAGRAM



PIN ASSIGNMENT



Device	Count Mode	Reset Mode
HC160	BCD	Asynchronous
HC161	Binary	Asynchronous
HC162	BCD	Synchronous
HC163	Binary	Synchronous

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating:
Plastic "N" Package: −12mW/°C from 65°C to 85°C
Ceramic "J" Package: −12mW/°C from 100°C to 125°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range GND≤(V_{in} or V_{out})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature — 74HC Series 54HC Series	−40 −55	+85 +125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	—	500	ns

ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC}	25°C 54HC and 74HC	85°C 74HC	125°C 54HC	Unit
				Typical	Guaranteed		
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	1.2 2.4 3.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$=20 μA	2.0 4.5 6.0	0.6 1.8 2.4	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=−20 μA	2.0 4.5 6.0	1.998 4.499 5.999	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in}=V_{IH} or V_{IL} I_{out}=−4.0 mA I_{out}=−5.2 mA	4.5 6.0	4.20 5.80	3.98 5.48	3.84 5.34	3.70 5.20	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} I_{out}=20 μA	2.0 4.5 6.0	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in}=V_{IH} or V_{IL} I_{out}=4.0 mA I_{out}=5.2 mA	4.5 6.0	0.22 0.18	0.26 0.26	0.33 0.33	0.40 0.40	V
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	0.00001	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	—	8	80	160	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	54HC and 74HC Typical	54HC and 74HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)**	43	30	MHz
t_{PLH}	Maximum Propagation Delay, Clock to Q	21	28	ns
t_{PHL}	(Figures 1 and 7)	29	34	
t_{PHL}	Maximum Propagation Delay, Reset to Q (HC160 and HC161 only) (Figure 2 and 7)	27	36	ns
t_{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out	15	26	ns
t_{PHL}	(Figures 3 and 7)	18	32	
t_{PLH}	Maximum Propagation Delay, Clock to Ripple Carry Out	20	30	ns
t_{PHL}	(Figures 1 and 7)	24	36	
t_{PHL}	Maximum Propagation Delay, Reset to Ripple Carry Out (HC160 and HC161 only) (Figures 2 and 7)	29	38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 7)	5	10	ns

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC Typical	85°C 74HC Guaranteed Limit	125°C 54HC Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 7)**	2.0	14	5	4	MHz
		4.5	40	27	21	18
		6.0	44	32	25	21
t_{PLH}	Maximum Propagation Delay, Clock to Q (Figures 1 and 7)	2.0	85	170	214	253	ns
		4.5	17	34	43	51	
		6.0	14	29	36	43	
t_{PHL}		2.0	103	205	258	305	ns
		4.5	21	41	52	61	
		6.0	17	35	44	52	
t_{PHL}	Maximum Propagation Delay, Reset to Q (HC160 and HC161 only) (Figures 2 and 7)	2.0	105	210	265	313	ns
		4.5	21	42	53	63	
		6.0	18	36	45	53	
t_{PLH}	Maximum Propagation Delay, Enable T to Ripple Carry Out (Figures 3 and 7)	2.0	80	160	202	238	ns
		4.5	16	32	40	48	
		6.0	14	27	34	41	
t_{PHL}		2.0	98	195	246	291	ns
		4.5	20	39	49	58	
		6.0	17	33	42	49	
t_{PLH}	Maximum Propagation Delay, Clock to Ripple Carry Out (Figures 1 and 7)	2.0	88	175	221	261	ns
		4.5	18	35	44	52	
		6.0	15	30	37	44	
t_{PHL}		2.0	108	215	271	320	ns
		4.5	22	43	54	64	
		6.0	18	37	46	54	
t_{PHL}	Maximum Propagation Delay, Reset to Ripple Carry Out (HC160 and HC161 only) (Figures 2 and 7)	2.0	110	220	277	328	ns
		4.5	22	44	55	66	
		6.0	19	37	47	55	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 7)	2.0	38	75	95	110	ns
		4.5	8	15	19	22	
		6.0	6	13	16	19	
C_{in}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance*		57	–	–	–	pF

* C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

** Applies to noncascaded configuration, only. With cascaded counters, (1) Clock to Ripple Carry Out Propagation Delays, (2) Enable T or Enable P to Clock Setup Times, and (3) Clock to Enable T or Enable P Hold Times determine f_{max}.

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC}	25°C 54HC and 74HC		85°C 74HC	125°C 54HC	Unit
			Typical	Guaranteed Limit			
t_{su}	Minimum Setup Time, Preset Data Inputs to Clock (Figure 5)	2.0	75	150	189	224	ns
		4.5	15	30	38	45	
		6.0	13	26	32	38	
t_{su}	Minimum Setup Time, Load to Clock (Figure 5)	2.0	68	135	170	201	ns
		4.5	14	27	34	40	
		6.0	11	23	29	34	
t_{su}	Minimum Setup Time, Reset to Clock (HC162 and HC163 only) (Figure 4)	2.0	80	160	202	238	ns
		4.5	16	32	40	48	
		6.0	14	27	34	41	
t_{su}	Minimum Setup Time, Enable T or Enable P to Clock (Figure 6)	2.0					ns
		4.5					
		6.0					
t_h	Minimum Hold Time, Clock to Preset Data Inputs (Figure 5)	2.0	25	50	63	75	ns
		4.5	5	10	13	15	
		6.0	4	9	11	13	
t_h	Minimum Hold Time, Clock to Load (Figure 5)	2.0					ns
		4.5					
		6.0					
t_h	Minimum Hold Time, Clock to Reset (HC162 and HC163 only) (Figure 4)	2.0					ns
		4.5					
		6.0					
t_h	Minimum Hold Time, Clock to Enable T or Enable P (Figure 6)	2.0					ns
		4.5					
		6.0					
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_{rec}	Minimum Recovery Time, Load Inactive to Clock (Figure 5)	2.0	63	125	158	186	ns
		4.5	13	25	32	37	
		6.0	11	21	27	32	
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_w	Minimum Pulse Width, Reset (HC160 and HC161 only) (Figure 2)	2.0	40	80	101	119	ns
		4.5	8	16	20	24	
		6.0	7	14	17	20	
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	–	1000	500	500	500	ns

FUNCTION TABLE

Inputs					Outputs
Clock	Reset*	Load	Enable P	Enable T	Q
↗	L	X	X	X	Reset
↗	H	L	X	X	Load Preset Data
↗	H	H	H	H	Count
↗	H	H	L	X	No Count
↗	H	H	X	L	No Count

*HC162 and HC163 only. HC160 and HC161 are Asynchronous-Reset Devices

H = high level
L = low level
X = don't care

FUNCTION DESCRIPTION

The HC160/161/162/163 are programmable 4-bit synchronous counters that feature parallel Load, synchronous or asynchronous Reset, a Carry Output for cascading, and count-enable controls.

The HC160 and HC162 are BCD counters with asynchronous Reset, and synchronous Reset, respectively. The HC161 and HC163 are binary counters with asynchronous Reset and synchronous Reset, respectively.

INPUTS

Clock (Pin 2) — The internal flip-flops toggle and the output count advances with the rising edge of the Clock input. In addition, control functions, such as Resetting (HC162 and HC163) and loading occur with the rising edge of the Clock input.

Preset Data Inputs P0, P1, P2, P3 (Pins 3, 4, 5, 6) — These are the data inputs for programmable counting. Data on these pins may be synchronously loaded into the internal flip-flops and appear at the counter outputs. P0 (pin 3) is the least-significant bit and P3 (pin 6) is the most-significant bit.

OUTPUTS

Q0, Q1, Q2, Q3 (Pins 14, 13, 12, 11) — These are the counter outputs (BCD or binary). Q0 (pin 14) is the least-significant bit and Q3 (pin 11) is the most-significant bit.

Ripple Carry Out (Pin 15) — When the counter is in its maximum state (1001 for the BCD counters or 1111 for the binary counters), this output goes high, providing an external look-ahead carry pulse that may be used to enable successive cascaded counters. Ripple Carry Out remains high only during the maximum count state. The logic equations for this output are:

Ripple Carry Out = Enable T•Q0•$\overline{Q1}$•$\overline{Q2}$•Q3
for BCD counters HC160 and HC162

Ripple Carry Out = Enable T•Q0•Q1•Q2•Q3
for binary counters HC161 and HC163

CONTROL FUNCTIONS

Resetting — A logic zero on the Reset pin (pin 1) resets the internal flip-flops and sets the outputs (Q0 through Q3) to logic zero. The HC160 and HC161 reset asynchronously, and the HC162 and HC163 reset with the rising edge of the Clock input (synchronous reset).

Loading — With the rising edge of the Clock, a logic zero on Load (pin 9) loads the data from the Preset Data Input pins (P0, P1, P2, P3) into the internal flip-flops and onto the output pins, Q0 through Q3. The count function is disabled as long as Load is low.

Although the HC160 and HC162 are BCD counters, they may be programmed to any state. If they are loaded with a state disallowed in BCD code, they will return to their normal count sequence within two clock pulses (see the Output State Diagram).

Count Enable/Disable — These devices have two count-enable control pins: Enable P (pin 7) and Enable T (pin 10). The devices will count when these two pins and the Load pin are high. The logic equation is:

Count Enable = Enable P•Enable T•Load

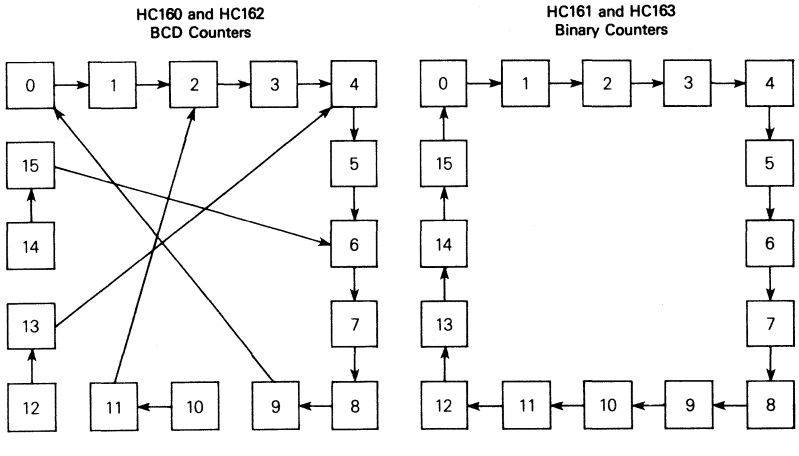
The count is either enabled or disabled by the control inputs according to Table 1. In general, Enable P is a count-enable control; Enable T is both a count-enable and a Ripple-Carry Output control.

TABLE 1. COUNT ENABLE/DISABLE

Control Inputs			Result at Outputs	
Load	Enable P	Enable T	Q0-Q3	Ripple Carry Out
H	H	H	Count	High when Q0-Q3
L	H	H	No Count	are maximum*
X	L	H	No Count	High when Q0—Q3 are maximum*
X	X	L	No Count	L

*Q0 through Q3 are maximum for the HC160 and HC162 when Q3 Q2 Q1 Q0 = 1001.
Q0 through Q3 are maximum for the HC161 and HC163 when Q3 Q2 Q1 Q0 = 1111.

OUTPUT STATE DIAGRAM



SWITCHING WAVEFORMS

FIGURE 1

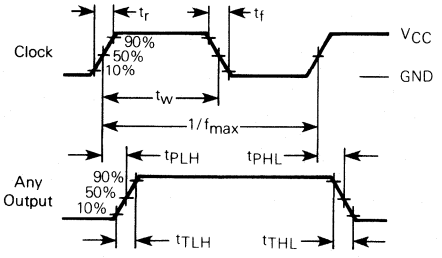


FIGURE 2

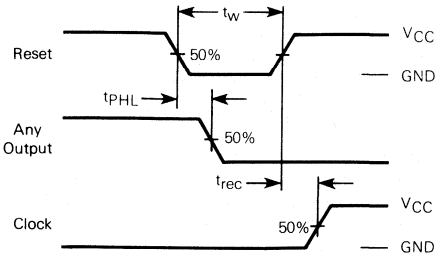


FIGURE 3

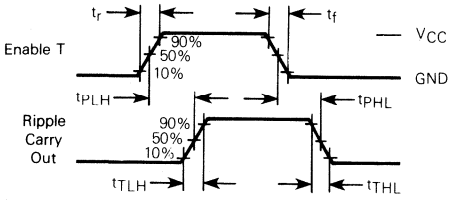


FIGURE 4

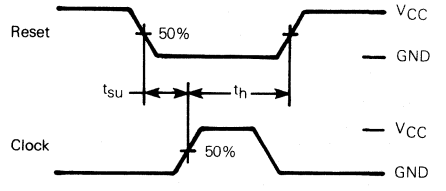


FIGURE 5

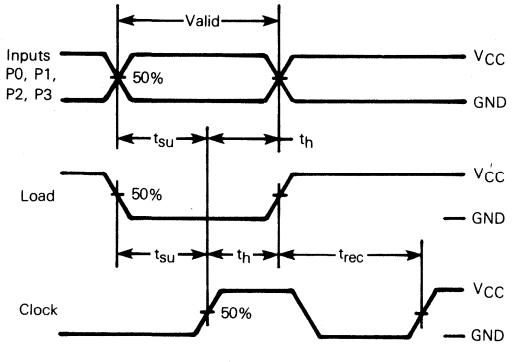


FIGURE 6

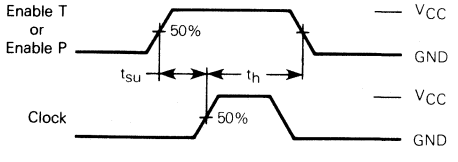
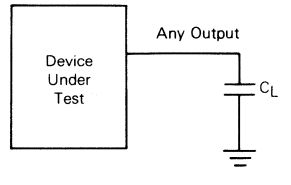
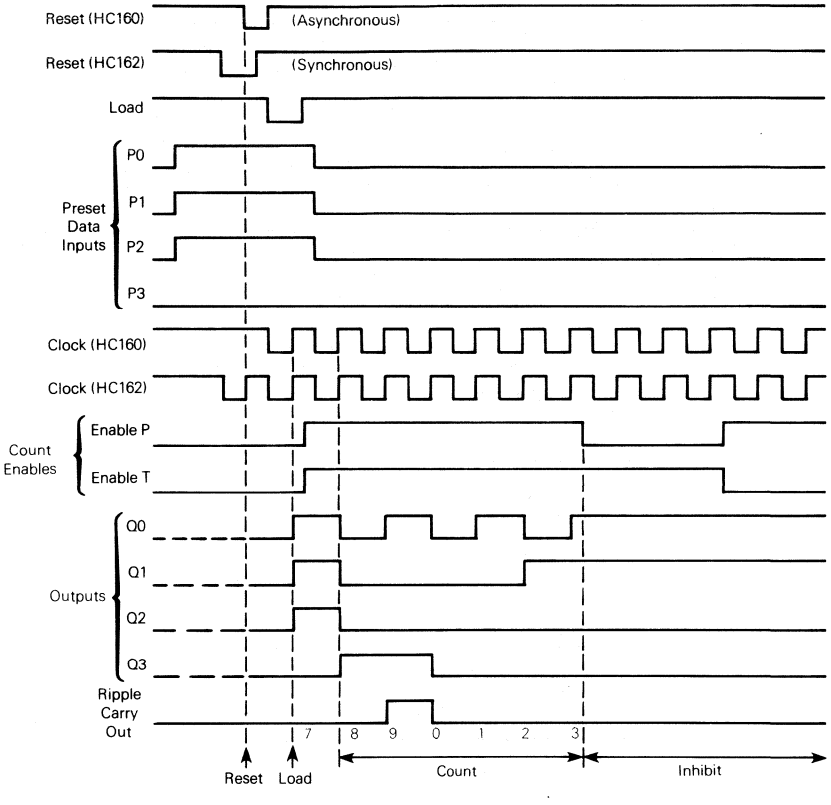


FIGURE 7 — TEST CIRCUIT



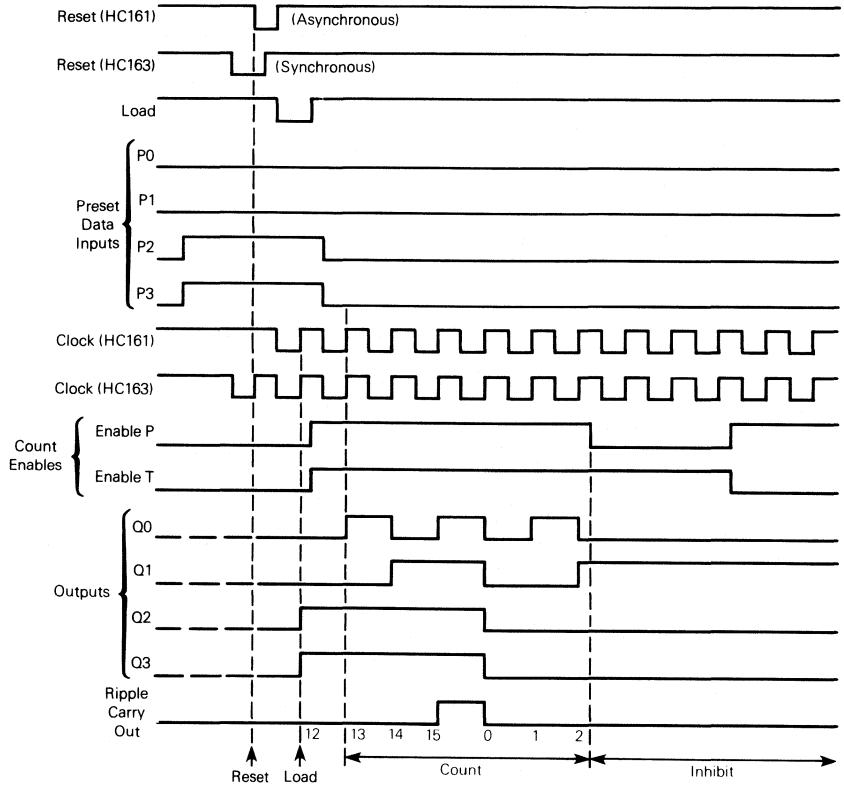
HC160, HC162 TIMING DIAGRAM

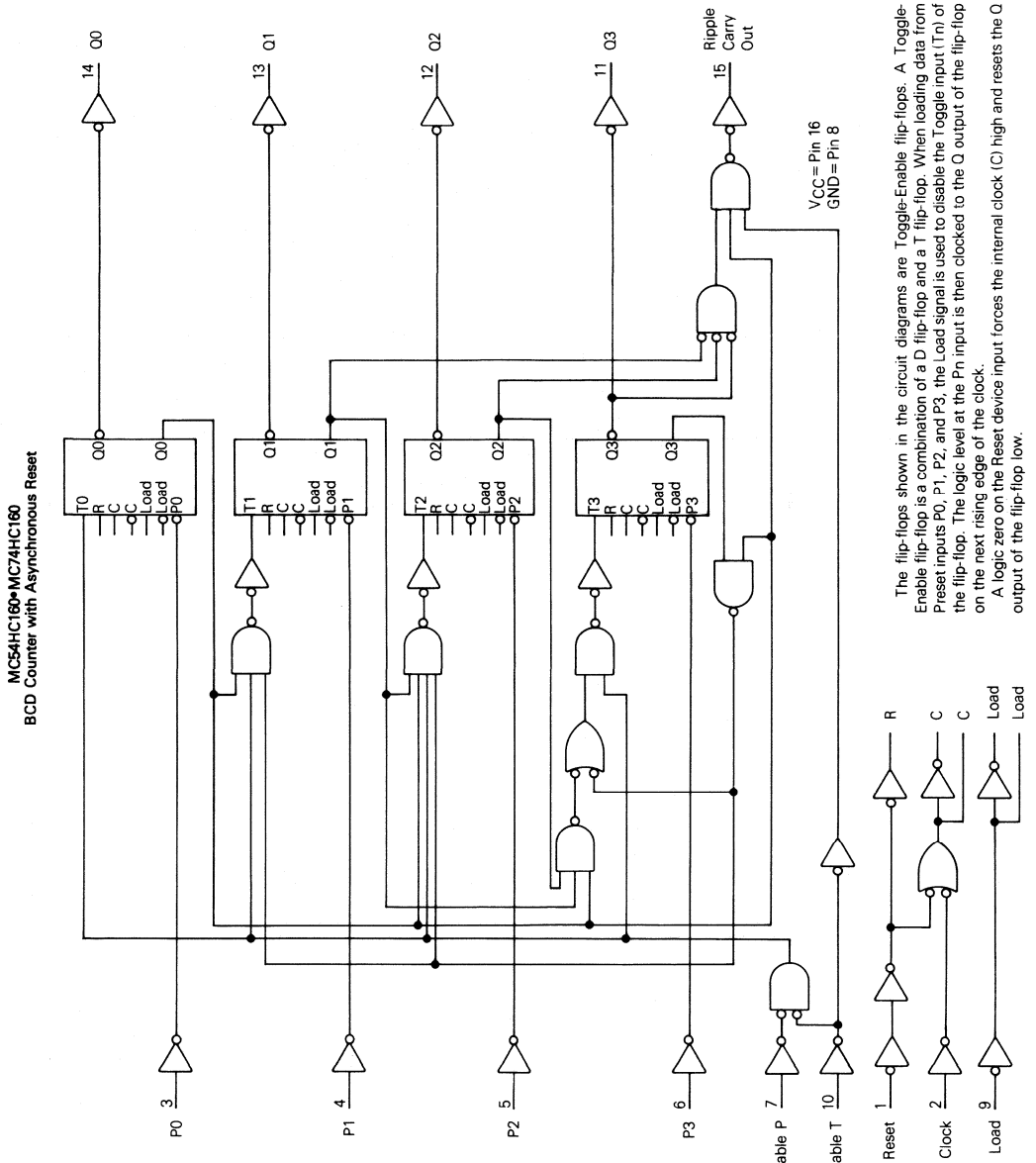
Sequence illustrated in waveforms:
1. Reset outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.



HC161, HC163 TIMING DIAGRAM

Sequence illustrated in waveforms:
1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.





The flip-flops shown in the circuit diagrams are Toggle-Enable flip-flops. A Toggle-Enable flip-flop is a combination of a D flip-flop and a T flip-flop. When loading data from Preset inputs P0, P1, P2, and P3, the Load signal is used to disable the Toggle input (Tn) of the flip-flop. The logic level at the Pn input is then clocked to the Q output of the flip-flop on the next rising edge of the clock.

A logic zero on the Reset device input forces the internal clock (C) high and resets the Q output of the flip-flop low.

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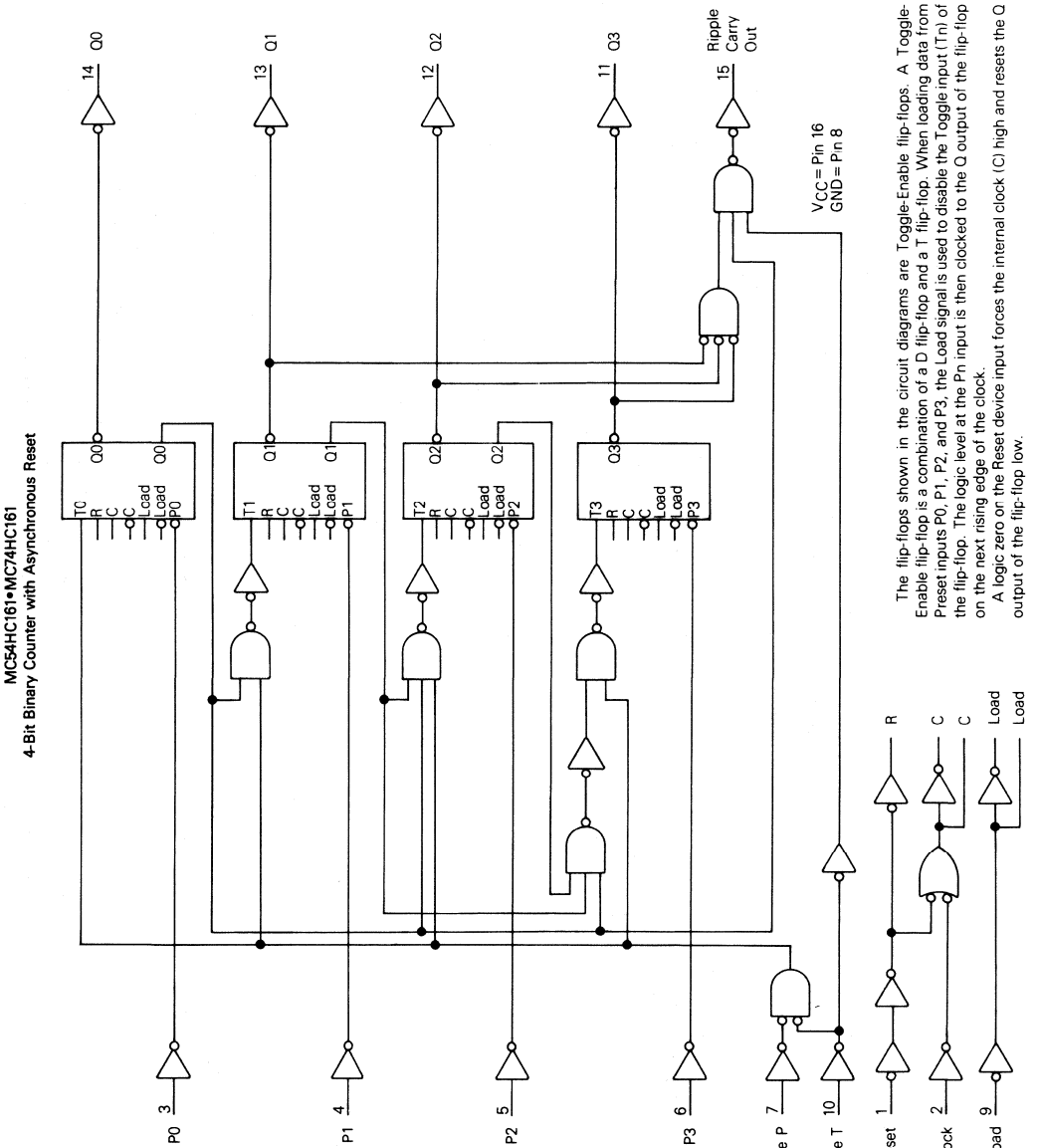

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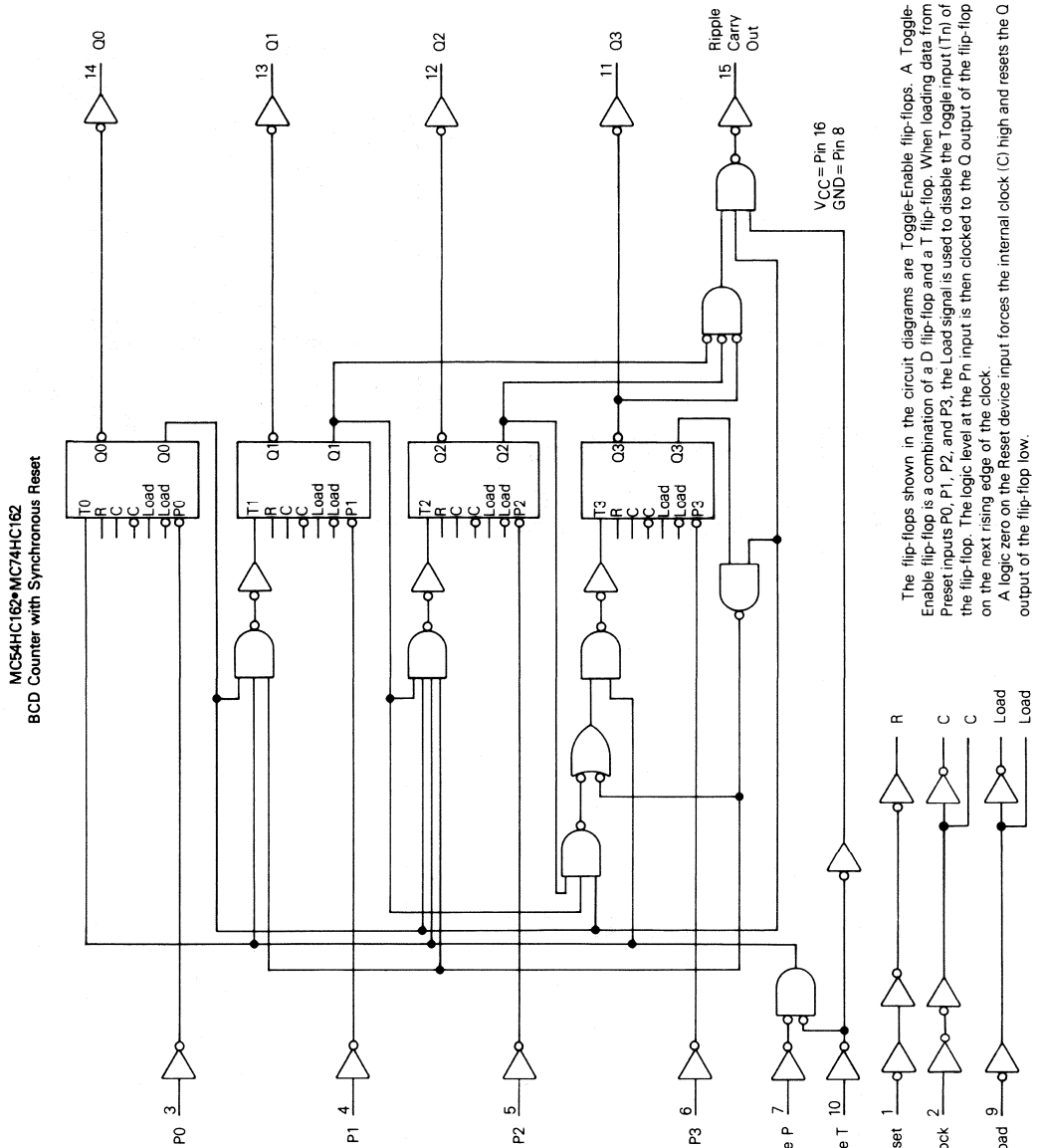

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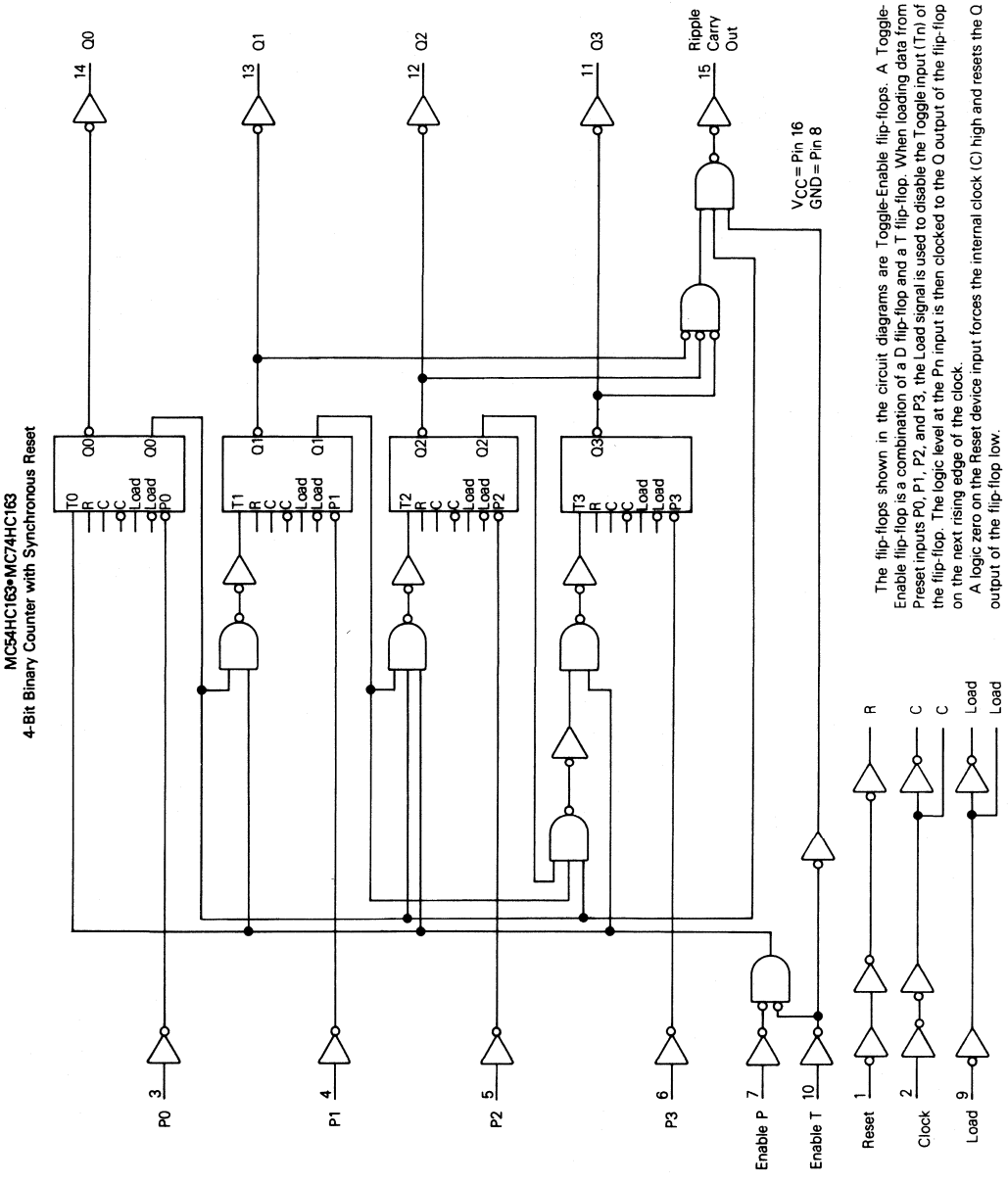

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