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ML8464B, ML8464C

Pulse Detector

GENERAL DESCRIPTION

The ML8464 is a Pulse Detector designed for use in magnetic disk applications to detect the amplitude peaks on the output of the read/write amplifier. These signal peaks are caused by flux reversal on the disk media, which when connected to the read/write amplifier result in an output consisting of a series of pulses of alternating polarity. The relative time position of these signal peaks is indicated by the leading edge of the TTL output pulses. The Pulse Detector accurately represents the time position of these peaks.

The ML8464 contains three major blocks. The amplifier block contains a wide bandwidth differential amplifier with Automatic Gain Control (AGC) and a precision full wave rectifier. The time channel block includes a programmable differentiator followed by a bidirectional one shot multivibrator. The gate channel block includes a differential comparator with programmable hysteresis, a D flip-flop and an output bi-directional one shot multivibrator. The ML8464C internally connects the time channel output to the D flip-flop.

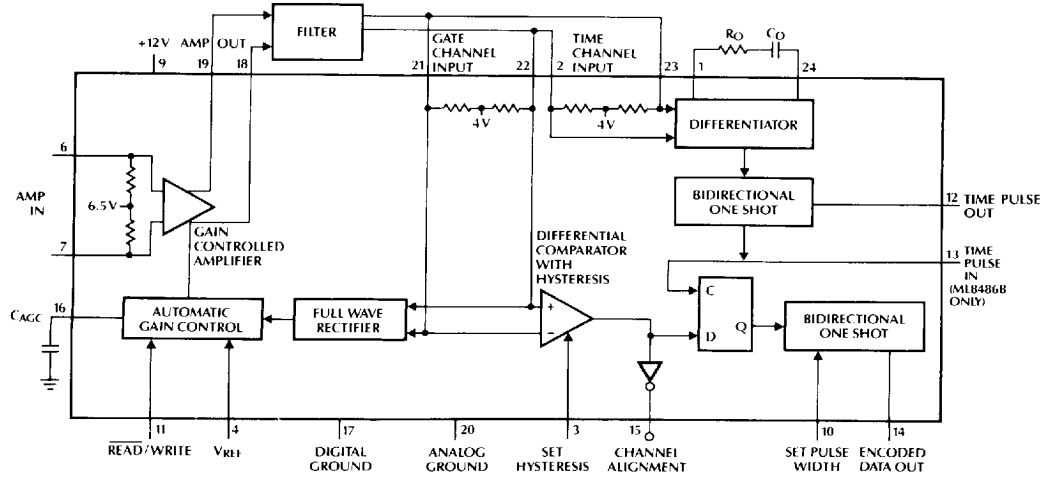
FEATURES

- Wide differential input signal range 20–660 mV_{P-P}
- TTL compatible digital Inputs and Output
- Externally gain controlled input differential amplifier
- Variable hysteresis comparator with gating circuitry
- Differentiator with externally programmable time constants
- Standard 12V power requirement
- Available in 24-pin DIP package, or a 28-pin surface mount PCC
- Improved pulse pairing (±1 ns max.)
- Handles RLL (1, 7) or (2, 7) data to 24 MB/s

ML8464B FEATURES

- Direct replacement for DP8464B

BLOCK DIAGRAM



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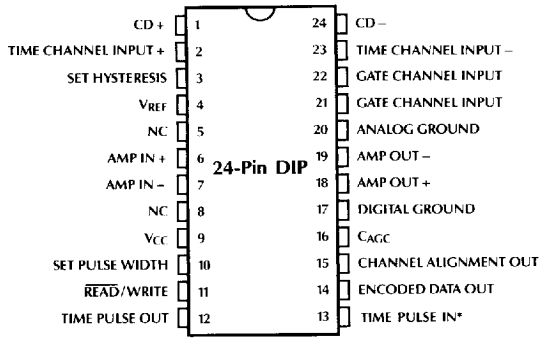
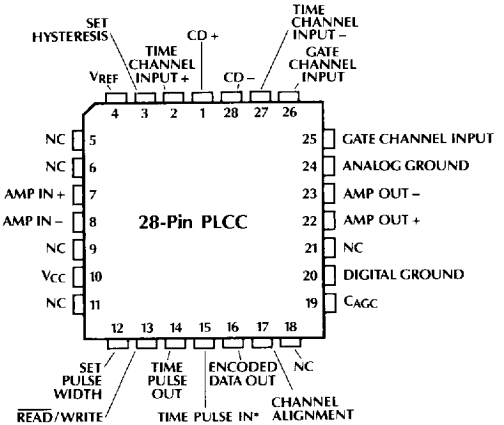
PIN CONNECTIONS



NC = No Connect
* THIS PIN IS A NO CONNECT ON THE ML8464C.



PIN DESCRIPTION

NAME	FUNCTION
Amp In+, Amp In–	Differential inputs to the Amplifier. The output of the read/write head amplifier should be capacitively coupled to these pins.
Amp Out+, Amp Out–	Differential outputs of the Amplifier. These outputs should be capacitively coupled to the gating channel filter and to the time channel filter.
Gate Channel Inputs	Differential inputs to the AGC block and the gating channel. Must be capacitively coupled from the Amp Out.
Time Channel Input+, Time Channel Input–	Differential inputs to the time channel differentiator. A filter is required between these pins and Amp Out pins to band limit the noise and to correct for any phase distortion due to read circuitry. Also inputs must be capacitively coupled to prevent disturbing the DC input level.
CD+, CD–	External differentiator network is connected between these two pins.
Set Hysteresis	DC voltage on this pin sets the amount of hysteresis on the differential comparator.
V_{REF}	AGC circuit adjusts the gain of the amplifier to make the differential peak to peak voltage on the Gate Channel. Input is four times the DC voltage on this pin.
C_{AGC}	External capacitor between this pin and Analog ground is connected for the AGC.
Set Pulse Width	External capacitor between this pin and Digital ground is connected to control the pulse width of the Encoded Data Out.
$\overline{\text{Read}}$/Write	TTL input. When low, the chip is in read mode and active. When High, the chip is forced into stand by mode.
Channel Alignment	Buffered output of the differential comparator with hysteresis. This output is TTL on the ML8464B, and is open emitter on ML8464C. The ML8464C is specified with a 2KΩ pull-down resistor to ground.
Time Pulse In (ML8464B only)	This is the TTL input to the clock of the D flip-flop. Usually it is connected to the Time Pulse Out pin.
Time Pulse Out	ML8464B: This is the TTL output from the bidirectional one shot following the differentiator. Usually it is connected to the Time Pulse In pin. ML8464C: Open emitter-follower test point.
Encoded Data Out	TTL output. Leading edge of this pin indicates the time position of the peaks.
V_{CC}	12V power supply.
GND	Digital ground. Digital signals should be referenced to this pin.
AGND	Analog ground. Analog signals should be referenced to this pin.

5

FUNCTIONAL DESCRIPTION

The output from the read/write amplifier is AC coupled to the amp input of the ML8464. The amplifier's output voltage is fed back via an external filter to an internal fullwave rectifier and compared against the external voltage on the V_{REF} pin. The AGC circuit adjusts the gain of the amplifier to make the peak to peak differential voltage on the Gate Channel Input four times the DC voltage on the V_{REF}. Typically the signal on the amp out will be set for $4V_{P-P}$ differential. Since the filter usually has a 6dB loss, the signal on the Gate Channel Input will be $2V_{P-P}$ differential. The user should therefore set 0.5V on V_{REF} which can be done with a simple voltage divider from the +12V supply or other suitable reference.

The peak detection is performed by feeding the output of the amplifier through an external filter to the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. However, if the signal exhibits shouldering, the differentiator will also respond to noise near the baseline. To avoid this problem, the signal is also fed to a gating channel which is used to define a level either side of the baseline. This gating channel is comprised of a differential comparator with hysteresis and a D flip-flop. The hysteresis for this comparator is externally set via the Set Hysteresis pin. In order to have data out, the input amplitude must first cross the hysteresis level which will change the logic level on the D input of the flip-flop. The peak of the input signal will generate a pulse out of the differentiator and bidirectional one shot. This pulse will clock the new data at the D input through to the output. In this way, when the differentiator is responding to noise at the baseline, the output of the D flip-flop is not changing since the logic level into the D input has not been changed. The comparator circuitry is therefore a gating channel which prevents any noise near the baseline from contaminating the data. The amount of hysteresis is twice the DC voltage on the Set Hysteresis pin. For instance, if the voltage on the Set Hysteresis pin is 0.3V, the differential AC signal across the gate channel input must be larger than 0.6V before the comparator will change states. In this case, the hysteresis is 30% of a 2V peak to peak differential signal at the gate channel input.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	14V
TTL Input Voltage	5.5V
TTL Output Voltage	5.5V
Input Voltage	5.5V
Differential Input Voltage	+3V
θ_{JA} for 24-Pin Plastic DIP (Copper Lead Frame)	60°C/Watt
θ_{JA} for 28-Pin PLCC (Copper Lead Frame)	60°C/Watt
Storage Temperature Range	–65°C to +150°C

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions of T_A = 0 to 70°C, V_{CC} = 12.0V ± 10%, V_{REF} = 0.5V, Set Hysteresis = 0.3V, Read/Write = 0.8V unless otherwise noted. (All pin numbers refer to DIP package.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
AMPLIFIER						
Z_{INAI}	Amp In Impedance	0.8	1.0	1.5	kΩ	
A_{VMIN}	Min Voltage Gain			6.0	V/V	AC Output $4V_{P-P}$ Differential
A_{VMAX}	Max Voltage Gain	180			V/V	AC Output $4V_{P-P}$ Differential
V_{CAGC}	Voltage on C_{AGC}	2.8	4.5 3.4	5.5	V V	A_V = 6.0 A_V = 180
GATE CHANNEL						
Z_{INGCI}	Gate Channel Input Impedance	1.75	2.5	3.25	kΩ	
I_{CAGC^-}	Current that charges C_{AGC}	−1.5	−2.5	−3.5	mA	Pin 16 = 3.9V Pin 21 – Pin 22 = 1.3V
I_{CAGC^+}	Current that discharges C_{AGC}		1	5	μA	Pin 16 = 5.0V Pin 21 – Pin 22 = 0.7V
I_{VREF}	V_{REF} Input Bias Current		−0.01	−100	μA	
V_{THAGC}	AGC Threshold	0.88	1.0	1.12	V	Pin 16 = 4.2V See Note 1
I_{SH}	Set Hysteresis Bias Current		−60	−100	μA	
V_{THSH}	Set Hysteresis Threshold	0.48	0.6	0.72	V	See Note 2
TIME CHANNEL						
Z_{INTC}	Time Channel Input Impedance	3.5	5	6.5	kΩ	
I_{CD}	Current into pins 1 & 24 that discharges C_D	2.1	2.7	3.4	mA	
WRITE MODE						
Z_{INAI}	Amplifier Input Impedance in Write Mode	100		500	Ω	Pin 11 = 2V
I_{CAGC}	Pin 16 Current in Write Mode		1.0	5.0	μA	Pin 11 = 2V Pin 16 = 3.9V Pin 21 – Pin 22 = 1.3V
DIGITAL PINS						
V_{IH}	High Level Input Voltage	2.0			V	ML8464B: Pins 11, 13 ML8464C: Pin 11
V_{IL}	Low Level Input Voltage			0.8	V	
V_I	Input Clamp Voltage			−1.5	V	V_{CC} = 10.8V, I_I = −18mA
I_{IH}	High Level Input Current			20	μA	V_{CC} = 13.2V, V_I = 2.7V
I_I	Input Current at Maximum Input Voltage			1	mA	V_{CC} = 13.2V, V_I = 5.5V
I_{IL}	Low Level Input Current			−200	μA	V_{CC} = 13.2V, V_I = 0.5V
V_{OH}	High Level Output Voltage	2.4			V	V_{CC} = 10.8V, V_{IOH} = −40μA See notes 3, 7
V_{OL}	Low Level Output Voltage			0.5	V	V_{CC} = 10.8V, I_{OL} = 800μA, see note 7
I_{OSC}	Output Short Circuit Current			−100	mA	V_{CC} = 13.2V, V_O = 0V
I_{CC}	Supply Current		54	75	mA	V_{CC} = 13.2V

5

DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions of T_A = 0 to 70°C, V_{CC} = 12.0V ± 10%, V_{REF} = 0.5V, Set Hysteresis = 0.3V, Read/Write = 0.8V unless otherwise noted. (All pin numbers refer to DIP package.)

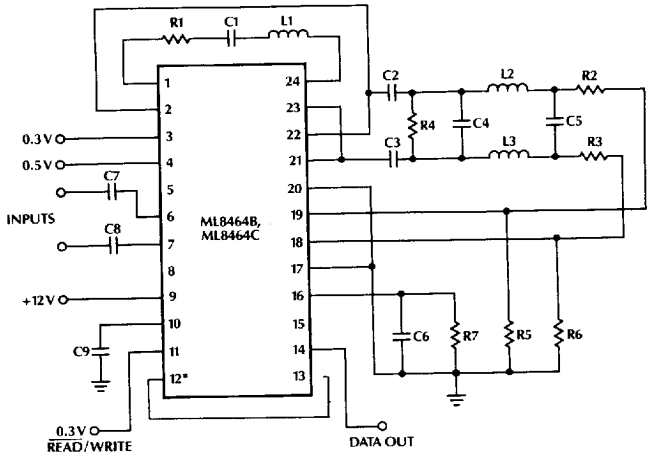
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL PINS (Continued)						
V_{OHCA}	Channel Alignment Pin V_{OH}					(Note 3)
	ML8464B	2.4			V	I_{OH} = –40μA
	ML8464C		7.6		V	10kΩ Load to GND
V_{OLCA}	Channel Alignment Pin V_{OL}					(Note 3)
	ML8464B			0.4	V	I_{OL} = 800μA
	ML8464C		6.9		V	10kΩ Load to GND
V_{OHTP}	Time Pulse Out Pin V_{OH}					
	ML8464B	2.4			V	10kΩ Load to GND
	ML8464C		9.6		V	10kΩ Load to GND
V_{OLTP}	Time Pulse Out Pin V_{OL}					
	ML8464B			0.4	V	10kΩ Load to GND
	ML8464C		8.6		V	10kΩ Load to GND

AC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply range of V_{CC} = 10.8 to 13.2V, T_A = 0 to 70°C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
ML8464-1						
t_{P-P}	Pulse Pairing		±0.5	±1.0	ns	
ML8464-1.5						f = 2.5MHz
t_{P-P}	Pulse Pairing[6]		±0.8	±1.5	ns	V_{IN} = 40mV_{P-P} differential
ML8464-2						See note 4
t_{P-P}	Pulse Pairing		±1.5	±3.0	ns	

Note 1: The AGC threshold is defined as the voltage across the gate channel input when the voltage on C_{AGC} is 4.2V.
Note 2: The Set Hysteresis threshold is defined as the voltage across the gate channel input when the channel alignment output voltage changes state.
Note 3: To prevent inductive coupling from the digital outputs to amplifier inputs, the TTL outputs should not drive more than one ALS TTL load.
Note 4: The filter and differentiator network are described in the pulse pairing set-up.
Note 5: All limits are guaranteed by 100% testing or alternate methods.
Note 6: The 1.5 ns pulse pairing specification is available only on the ML8464C, not the ML8464B.
Note 7: ML8464B: Pins 12, 14, 15
ML8464C: Pins 14 and 15 only.



PULSE PAIRING SET UP

PARTS LIST

R1	220Ω	C1	82pF
R4	680Ω	C2, C3, C6	0.01μF
R2, R3	240Ω	C4	100pF
R5, R6	3.3kΩ	C5	15pF
R7	100kΩ	C7, C8	0.0022μF
L1	1.5μH	C9	47pF
L2, L3	4.7μH		

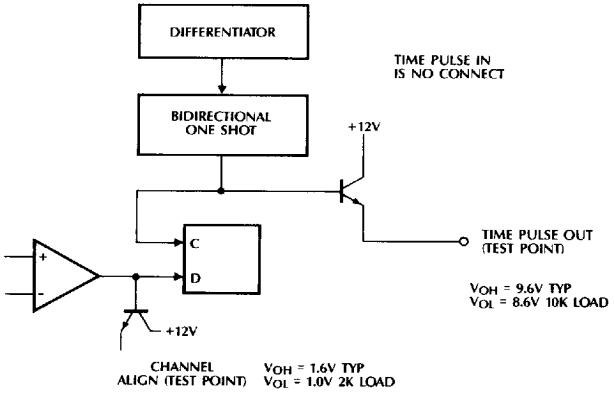
* The connection between pins 12 and 13 is required only for the ML8464B.

5

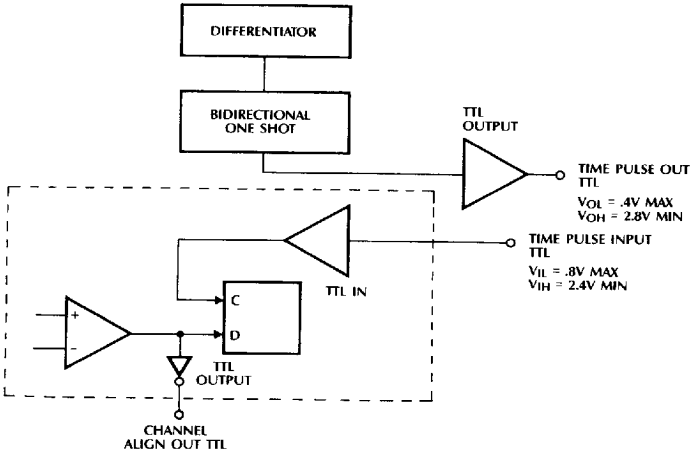
PULSE PAIRING MEASUREMENT

The scope probe is connected to pin 14 (Encoded Data Out) and triggered off of its positive edge. The trigger holdoff is adjusted so that the scope first triggers off the pulse associated with the positive peak and then off the pulse associated with the negative peak. Pulse pairing is displayed on the second pair of pulses on the display. If the second pair of pulses are separated by 6ns, then the pulse pairing for the part is ±3ns.

ML8464C



ML8464B



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DIFFERENCES BETWEEN ML8464C AND ML8464B

THE EXTERNAL DELAY

The ML8464B open circuits the digital signal at pins 12 and 13. This allows for the insertion of an external delay filter. The ML8464C has no TTL buffers at these pins and closes the signal path internally bringing out a test point at pin 12. Hence, the ML8464 does not allow for the external delay.

TEST POINTS

The ML8464B has two TTL test points at pins 12 and 15. The ML8464C uses open emitter followers in an ECL configuration. Hence, the voltage levels are not similar at pins 12 and 15 on both devices. The typical voltage level at pins 12 are V_{OH} = 9.6V, V_{OL} = 8.6V and at pin 15 are V_{OH} = 1.6V, V_{OL} = 1.0V.

AGC GAIN CONTROL FACTOR

The AGC reference level is a DC voltage externally set at V_{REF} (pin 4). Increasing this DC voltage will increase the gain of the gain controlled amplifier.

AGC gain control factor =

$$\frac{V_{OUT\ PEAK} = \text{peak of the AGC amp}}{V_{REF}}$$

$$\text{AGC gain control factor} = \frac{2.5V_{PP}}{0.5V_{DC}} = 5 \text{ for ML8464B}$$

$$= \frac{2.0V_{PP}}{0.5V_{DC}} = 4 \text{ for ML8464C}$$

Thus, at V_{REF} = $0.5V_{DC}$, V_{OUT} AGC = 2.5V for ML8464B and 2.0V for ML8464C. This smaller signal amplitude should be taken into consideration at the hysteresis comparator. To set the desired amount of hysteresis, and external DC control voltage is used. The particular settings for V_{REF} and control voltage at pin 3 that optimizes the ML8464B performance may not necessarily optimize the ML8464C performance.

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE	PULSE PAIRING
ML8464C-1CP	0°C to +70°C	MOLDED DIP (P24)	±1 ns
ML8464C-1CQ	0°C to +70°C	MOLDED PCC (Q28)	±1 ns
ML8464C-1.5CP	0°C to +70°C	MOLDED DIP (P24)	±1.5 ns
ML8464C-1.5CQ	0°C to +70°C	MOLDED PCC (Q28)	±1.5 ns
ML8464C-2CP	0°C to +70°C	MOLDED DIP (P24)	±3 ns
ML8464C-2CQ	0°C to +70°C	MOLDED PCC (Q28)	±3 ns
ML8464B-1CP	0°C to +70°C	MOLDED DIP (P24)	±1 ns
ML8464B-1CQ	0°C to +70°C	MOLDED PCC (Q28)	±1 ns
ML8464B-2CP	0°C to +70°C	MOLDED DIP (P24)	±3 ns
ML8464B-2CQ	0°C to +70°C	MOLDED PCC (Q28)	±3 ns