MM5290 16K RAM Functional Description

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INTRODUCTION

This functional description covers the operation of the MM5290 16k dynamic RAM currently manufactured by National Semiconductor. This device is directly interchangeable with the MK4116. The National design has some internal differences, but these are transparent to the user, making the MM5290 a direct replacement for the MK4116.

Block Diagram

The block diagram shown in *Figure 1* shows the functional relationship between major blocks of circuitry in the MM5290. The multiplexed address, unlatched output and gated $\overline{CAS}$ features are shown. The row decoder column decoders and two 64 x 128 memory arrays with sense amplifiers between them are drawn in blocks that indicate their actual physical relationship on the die. This arrangement, with sense amplifiers in the middle and column decoders duplicated along each side, reduces cross talk (coupled noise) between address and column lines. Noise margin is improved because column line length is minimized.

Clock Generation

The MM5290 has multiplexed addressing necessitating separate row (Row Address Strobe, $\overline{RAS}$) and column (Column Address Strobe, $\overline{CAS}$) strobes. The timing relationship between these two strobes is made non-critical by gating $\overline{CAS}$ with the internal $\overline{RAS}$ clock. This is shown in *Figure 1*, along with the fact that $\overline{CAS}$ gates the write enable ($\overline{WE}$) control. These three signals are the source of the internal clocks (row, column and write clocks). Another way to describe this is: 1) the row clocks are referenced to $\overline{RAS}$; 2) the column clocks are referenced to either $\overline{RAS}$ or $\overline{CAS}$, depending on the $\overline{RAS}$ to $\overline{CAS}$ delay; and 3) the write clocks are referenced to $\overline{CAS}$ or $\overline{WE}$, depending on which occurs later. The block diagram in *Figure 1* indicates which blocks of circuitry the internal clocks control.

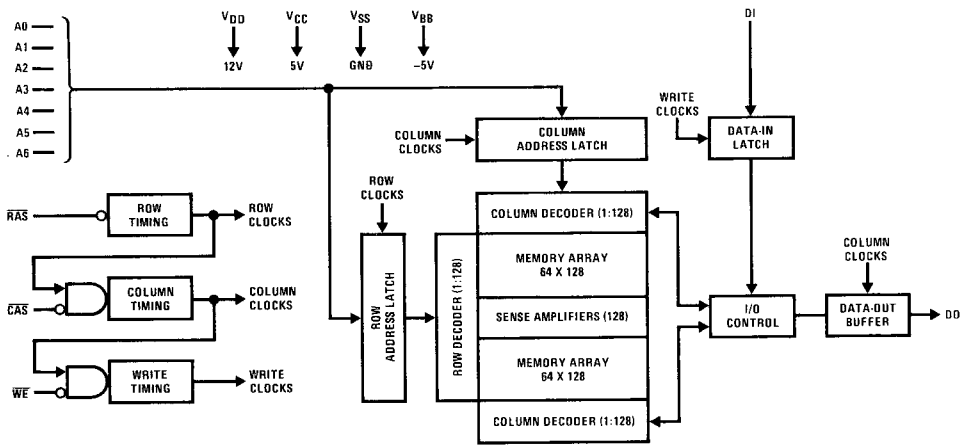


FIGURE 1. MM5290 Block Diagram

Memory Cell

The basic memory cell consists of a transistor and capacitor as shown in *Figure 2*. Data is stored by selecting a cell and charging or discharging the storage capacitor C_S through transistor Q1. Q1 is then turned OFF (cell deselected) and data is retained until charge is lost through leakage current or the cell is refreshed. Each memory cell must be refreshed every 2 ms to guarantee data retention.

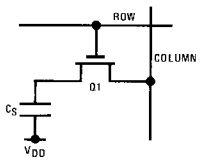


FIGURE 2. Basic Memory Cell

Cell Selection

Figure 3 shows a block diagram indicating how an individual memory cell is selected (addressed). First, the row address is latched in by $\overline{RAS}$. This is decoded to select 1 out of the 128 rows. Actually, there are 128 cells tied to each row so that 128 cell transistors (Q1 in *Figure 3*) are turned ON. Second, the column address is latched in. This is decoded to select 1 of the 128 columns. The row and column coincidence selects an individual cell for either reading or writing data.

Read Operation

Figure 4 shows a simplified version of the array of cells with the read/write circuitry. The array consists of 16,384 memory cells plus 2 rows of 128 reference cells. These are separated into 2 arrays by 128 sense amplifiers as shown. If row address AX5 is a logic "0", a row in the top half of the memory is being selected while the reference cells on the other side of the sense amplifier are also selected. Data is stored in complementary form in this half (top) of the array. The other half (bottom) of the array stores the data in true form when row address AX5 is a logic "1". A logic "0" in the array is defined as 0V stored in the cell and a logic "1" as +V.

Although the usual time reference in a cycle of operation is the high-to-low transition of $\overline{RAS}$, the prior events of discharging all row lines (to 0V) and precharging all column lines (to V_{DD}) must occur before a cycle of operation can be successfully completed. The starting point then is all row lines discharged and all column lines precharged. Then a row address is latched and the 128 cells connected to the selected row line are "read" by the 128 sense amplifiers. This also refreshes them. When a column address is latched, 1 of the 128 columns is connected to the I/O bus and the data of the selected cell becomes available on the DO pin.

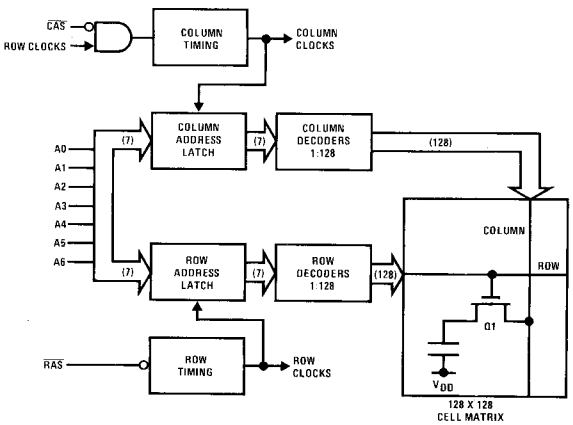


FIGURE 3. Block Diagram of Cell Selection

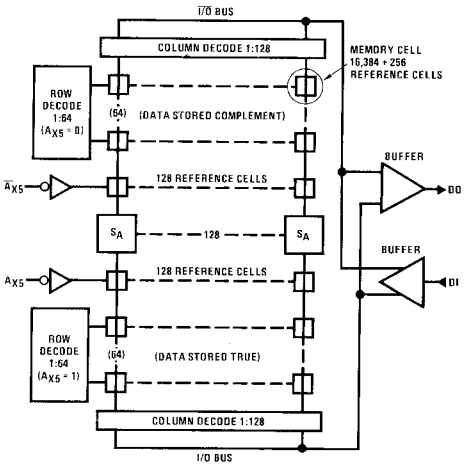


FIGURE 4. Simplified Read-Write Circuitry

Sense Amplifier Operation

Figure 5 shows a simplified version of a sense amplifier together with a selected memory cell and the reference cell associated with "reading" the cell. When the cell is selected by the row address, a reference cell on the opposite side of the differential sense amplifier is also selected. (In fact, the entire row of 128 reference cells is selected.) If the selected memory cell contains a "1", then the storage capacitor C_S has the same potential as the left column line and no charge is transferred through Q1. If the selected cell contains a "0", then charge will be transferred through Q1 and shared between C_S and C_{CL}. The voltage of the column line will be reduced by ΔV where ΔV is a function of the ratio of C_S to C_{CL}.

Simultaneously with the events happening with the memory cell and the left column line, the right column line will always be reduced by 1/2 ΔV because charge will be transferred through Q2 between the capacitor of the reference cell labeled 1/2 C_S and C_{CL}. (All reference cells begin the cycle with a "0" stored on the storage capacitor.) This means that the sense amplifier will have a voltage difference of $\pm 1/2\ \Delta V$ across it with the polarity depending on the data stored in the memory cell. The sense amplifier regeneratively amplifies the difference and restores the data in the memory cell. This signal is also amplified by the output buffer and made available at the output pin (DO).

Write Operation

Figure 6 shows a block diagram of the write circuitry. The Data In buffer drives the column line of the selected cell either low (to ground) or high (to V_{DD}) depending on the logic level of DI. Transistor Q1 is ON because the cell has been selected and the storage capacitor C_S is written to the voltage of the column line. Then Q1 is turned OFF and C_S retains the data.

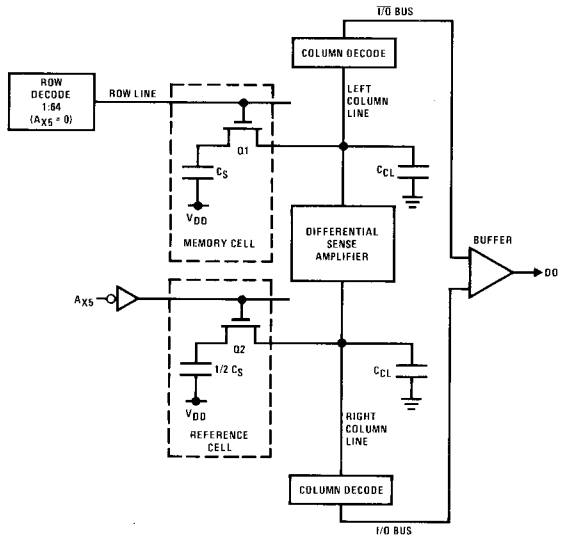


FIGURE 5. Simplified Read Circuitry

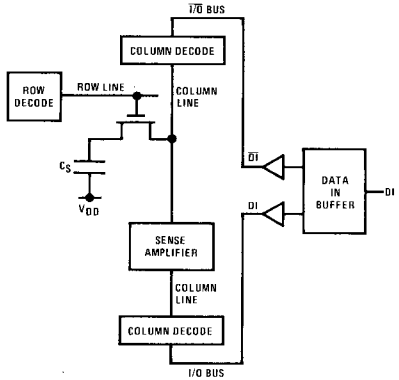


FIGURE 6. Simplified Write Circuitry

Refresh

One side of the storage capacitor of the memory cell is a polysilicon V_{DD} line. The other side is a diffused junction (the drain of a transistor). The leakage of this junction normally increases with temperature and limits the data retention. This "dynamic" nature of the data storage requires that the cells be refreshed periodically (every 2 ms with today's technology) to retain data. A row of cells (128) is refreshed whenever any valid $\overline{RAS}$ cycle occurs. This means it takes 128 cycles to refresh the MM5290. Operating power is reduced and the output kept in the high impedance state when $\overline{CAS}$ is kept high and $\overline{RAS}$ is cycled for each of the 128 row addresses ($\overline{RAS}$ Only Refresh) to refresh the memory.

Most of the circuitry used in the MM5290 is dynamic and must also be "refreshed" for the memory to function properly. This is accomplished automatically when the dynamic cells are refreshed. This dynamic circuitry requires several cycles after power-up or after the refresh limit has been exceeded before proper device operation can be assured.

Read Timing

The read cycle timing is indicated in *Figure 7*. The cycle begins with $\overline{RAS}$ going low. This latches the row address. The address bus must be stable at this time: $\overline{CAS}$ then switches low sometime later. Again the address bus must be stable at the time $\overline{CAS}$ goes low because the column address is latched at that time. $\overline{WE}$ must be high coincidentally with $\overline{CAS}$ low during the read cycle. Data Out (DO) will be valid before t_{CAC} (access time from $\overline{CAS}$) or t_{RAC} (access time from $\overline{RAS}$) whichever is limiting. The output will return to TRI-STATE® in t_{OFF} time when $\overline{CAS}$ switches high. The valid data can be maintained to the end of the cycle (in fact, into the next cycle) because t_{CRP} minimum ($\overline{CAS}$ to $\overline{RAS}$ precharge time) is specified as a negative quantity in the data sheet.

Write Timing

There are 3 types of write cycles specified in the data sheet. These are called an Early Write, a Read-Write and a Read-Modify-Write cycle.

The Early Write cycle is characterized by $\overline{WE}$ going low no later than t_{WCS} minimum ($\overline{WE}$ to $\overline{CAS}$ set-up time) before $\overline{CAS}$. This could be called a "write only" cycle. The output remains in the high impedance state throughout the cycle while data is written into the desired location *(Figure 8a)*. D_{IN} is latched when $\overline{CAS}$ goes low and must be stable then rather than being referenced to $\overline{WE}$. The $\overline{WE}$ pulse width must be a minimum of t_{WP} and both the leading and trailing edges of $\overline{WE}$ have several timing constraints with respect to $\overline{RAS}$ and $\overline{CAS}$. Refer to the data sheet for these specifications.

The Read-Write cycle *(Figure 8b)* occurs when $\overline{WE}$ is delayed for at least t_{RWD} minimum ($\overline{RAS}$ to $\overline{WE}$ Delay) from $\overline{RAS}$ and the t_{CWD} minimum ($\overline{CAS}$ to $\overline{WE}$ Delay) from $\overline{CAS}$. The data in the selected location is first read; then new data is written into the location. The read portion of the cycle is explained in the section on Read Cycle Timing. The write portion of the cycle begins with data being latched in when $\overline{WE}$ falls and ends with the end of the cycle. The detailed timing is shown in the data sheet.

The Read-Modify-Write cycle *(Figure 8c)* is the Read-Write cycle extended in time so that the data in a particular location can be read, modified if necessary, and then written back into the same location. This requires that the $\overline{WE}$ pulse be delayed the minimum time of t_{RWD} from $\overline{RAS}$ and t_{CWD} from $\overline{CAS}$ plus an additional time shown as t_{MOD}. The additional time is the time required by the system to check the data, modify it as necessary and place it on the input data bus consistent with the required set-up time before $\overline{WE}$ goes low. Note that t_{MOD} is a system parameter. Detailed timing is given in the data sheet.

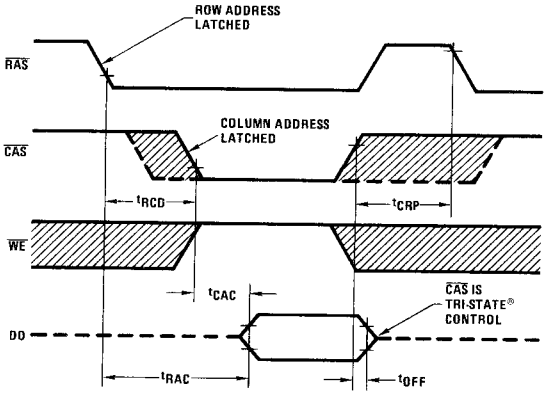


FIGURE 7. Read Cycle

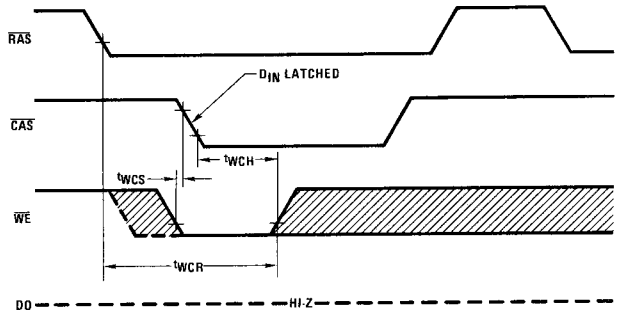


FIGURE 8a. Early Write

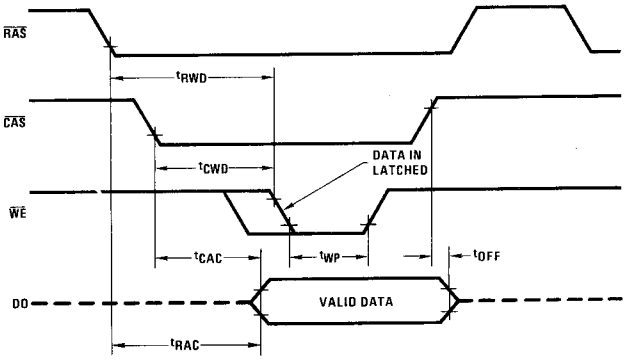


FIGURE 8b. Read-Write

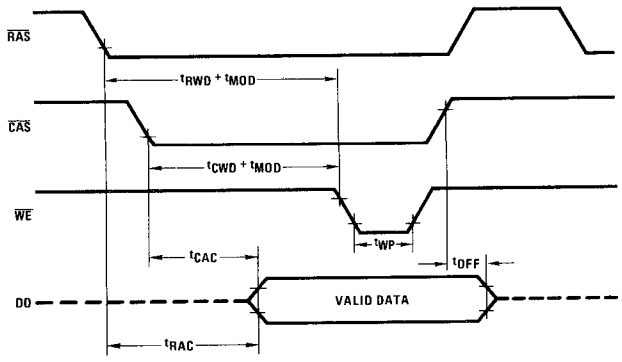


FIGURE 8c. Read-Modify-Write

Page Mode Timing

The MM5290 functions in a page mode operation with up to 128 bits (1 row) per page. Data may be read or written in this mode of operation.

Figure 9 shows the timing for a page mode Read cycle. The cycle starts like a normal read cycle with the access time of the first bit (bit 0) either t_{RAC} or t_{CAC} whichever is limiting. The rest of the page mode read is accomplished by keeping $\overline{RAS}$ low and cycling $\overline{CAS}$ an additional 127 times while changing to a new column address each time. $\overline{WE}$ may be held high continuously or cycled. If $\overline{WE}$ is cycled, it must meet the timing constraints shown in the data sheet. $\overline{RAS}$ cannot be held low for more than 32 μs so that the maximum $\overline{CAS}$ cycle time is approximately 250 ns to read the full 128 bits of data in a page (row).

Figure 10a shows the timing for a page mode Early Write cycle. The cycle begins as a normal early write cycle. The rest of this mode of operation is accomplished by keeping $\overline{RAS}$ low and cycling $\overline{CAS}$ an additional 127 times while changing to a new column address each time. The input data (D_{IN}) must be referenced to the falling edge of $\overline{CAS}$ and not $\overline{WE}$. $\overline{WE}$ may be held low or pulsed. The output will remain in the high impedance state throughout the cycle.

Figure 10b shows the timing for a page mode Read-Write cycle. The cycle begins as a normal read-write cycle. Then $\overline{RAS}$ is held low and $\overline{CAS}$ is cycled an additional 127 times while a new column address is selected each time. $\overline{WE}$ must be kept high for the t_{CWD} time (to guarantee the data is read) and then switched low for t_{WP} time to accomplish writing the new data. The data to be entered (D_{IN}) must be referenced to $\overline{WE}$ with the appropriate set-up and hold times shown in the data sheet. Extending the t_{CWD} time to allow for modifying data and then writing it back into the same location would make this a Read-Modify-Write page mode cycle.

Refresh Timing

The MM5290 must be refreshed every 2 ms. Any valid cycle of $\overline{RAS}$ will refresh a row of 128 bits. It requires 128 cycles, (1 for each row of the matrix) to refresh the entire memory. *Figure 11* shows $\overline{RAS}$ only refresh. Only $\overline{RAS}$ switches. $\overline{CAS}$ is held high which reduces I_{DD} and TRI-STATES the output.

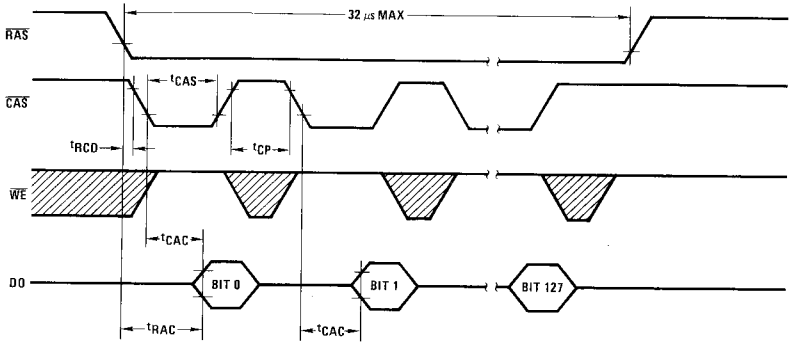


FIGURE 9. Page Mode Read Cycle

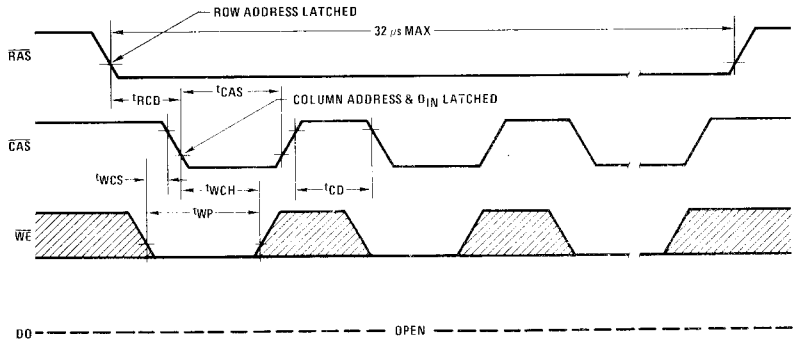


FIGURE 10a. Page Mode Early Write Cycle

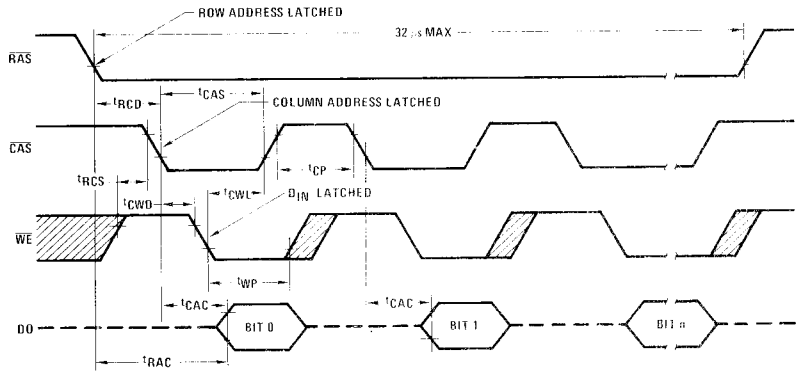


FIGURE 10b. Page Mode Read-Write Cycle

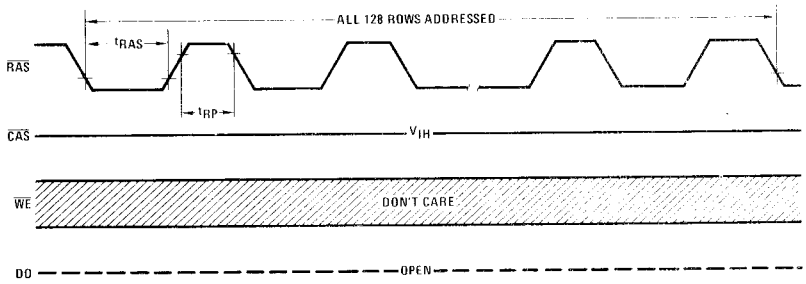
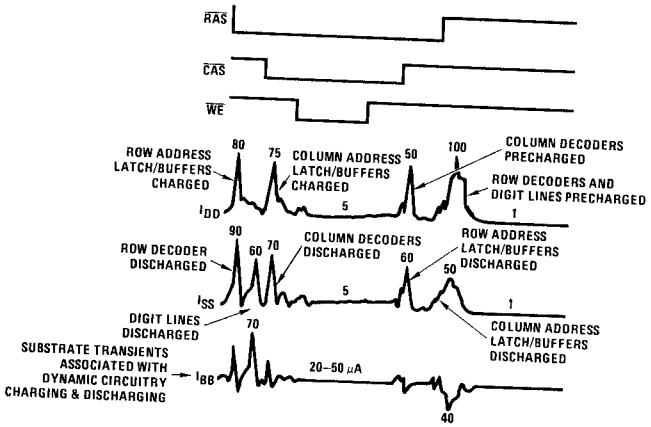


FIGURE 11. $\overline{RAS}$ Only Refresh Cycle

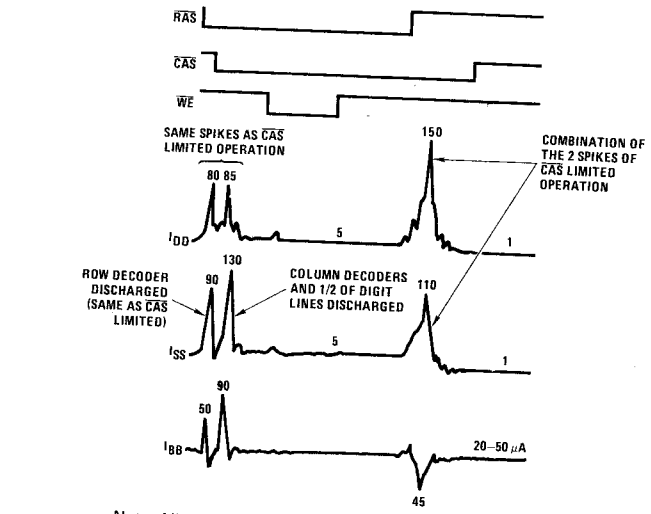
Current Transients

Figures 12 and 13 show the current waveforms for I_{DD}, I_{SS} and I_{BB}. When the MM5290 is operated with $\overline{CAS}$ limited timing, the transients associated with the row and column clocks are separated in time. The major events causing the transients are indicated in *Figure 12*. When the operation is $\overline{RAS}$ limited, some of the transients overlap. This is shown in *Figure 13*. The transients are then additive and maximum transient peaks occur. Adequate capacitive decoupling* at the board level is necessary to maintain power supply voltage transients within the data sheet specification of ±10%.



Note. All values in mA unless shown otherwise.

FIGURE 12. $\overline{CAS}$ Limited Timing Transients



Note. All values in mA unless shown otherwise.

FIGURE 13. $\overline{RAS}$ Limited Timing Transients

*Refer to "Dynamic RAM Board Design Made Easy"

Trouble Shooting Check List For Memory Systems Using the MM5290

1. Are all power supplies within spec, including spikes, at all points on the card?
   - V_{DD} = 12.0V ± 10%? ☐ Properly decoupled? ☐
   - V_{CC} = 5.0V ± 10%? ☐ Properly decoupled? ☐
   - V_{BB} = −5.0V ± 10%? ☐ Properly decoupled? ☐
2. Are there at least 8 legal RAS cycles after power-up before the memory is used? ☐
3. Are the input high and low levels within spec?
   - $V_{IHC} \geq 2.7V$ for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$? ☐
   - $V_{IH} \geq 2.4V$ for A_0-A_6, DI? ☐
   - $V_{IL} \leq 0.8V$ for all inputs? ☐
4. Are the transition times for the input signals within spec? ☐
   Has the ringing been damped by a series resistor where necessary? ☐
5. Is DO load within spec (I_{OH} = −5.0 mA max., I_{OL} = 4.2 mA max.)? ☐
6. Are clock pulse widths and precharge times OK?
   - $\overline{RAS}$ pulse width? ☐ $\overline{RAS}$ precharge time? ☐
   - $\overline{CAS}$ pulse width? ☐ $\overline{CAS}$ precharge time? ☐
   - $\overline{WE}$ pulse width? ☐
7. Is timing $\overline{RAS}$-limited ($t_{RCD} \leq t_{RCD}$ max.)? ☐
   or $\overline{CAS}$-limited ($t_{RCD} > t_{RCD}$ max.)? ☐
8. Are all address set-up and hold times within spec?
   - t_{ASR} and t_{RAH} for the row address? ☐
   - t_{ASC} and t_{CAH} ($\overline{CAS}$ limited timing) or t_{AR} ($\overline{RAS}$ limited timing) } for the column address? ☐
9. Are the $\overline{WE}$ set-up and hold times within spec?
   - t_{RCS} and t_{RCH} for a read cycle? ☐
   - t_{RWL} and t_{CWL}, t_{WCH} ($\overline{CAS}$ limited timing) or t_{WCR} ($\overline{RAS}$ limited timing) } for a write cycle? ☐
   - t_{WCS} for an early-write cycle? ☐
   - t_{CWD} ($\overline{CAS}$ limited timing) or t_{RWD} ($\overline{RAS}$ limited timing) } for a read-write or a read-modify-write cycle? ☐
10. Are the DI set-up and hold times within spec?
    - t_{DS} and t_{DH} relative to later of $\overline{CAS}$ or $\overline{WE}$ or t_{DHR} relative to $\overline{RAS}$ for $\overline{RAS}$ limited timing. } ☐

MM5290 Bit Map and Address Decoding

INTRODUCTION

Disturb testing requires a detailed knowledge of the topology and address decoding of a dynamic RAM. The MM5290 has its own unique topology and address decoding which is described in this write-up.

Figure 1 shows the MM5290 cell array diagram. It is oriented with a top view, as if a die were in a dual-in-line package, with pin 1 in the upper left hand corner. In this orientation the row decoders are across the bottom and the column decoders are along the sides. (Actually the column decoders are duplicated on each side.)

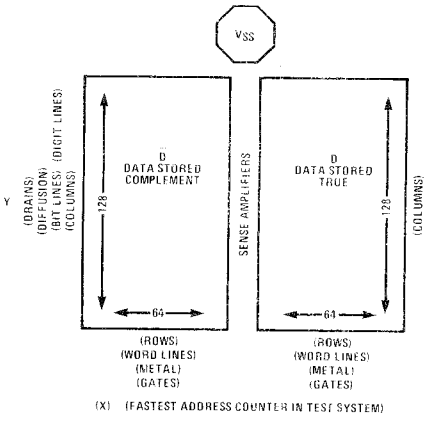


Figure 1. MM5290 Cell Array Diagram

Terminology is listed for those of us who may be confused by vertical rows, horizontal columns, bit lines, word lines, etc., so that definitions are clear. The terms "row" and "column" will be used from now on in this paper. X and Y address counter definitions are shown also. Note that even though the data out is not inverted from a user's point of view, the data is stored in complementary form in the left cell array.

Figure 2 shows the address decoding. This is shown with the cells indicated in a regular array. This is not the case and the actual topology will be discussed later. The assumptions are:

1. This is the same orientation as in figure 1.
2. One chooses the lower left hand corner of the array as the starting reference.
3. The row address counter is the faster of the two address counters providing the binary addresses.
4. The leads are translated on the test fixture as shown in figure 3.
5. The cells may be numbered in decimal from 0 to 16,383 and the numbers of the cell correspond to the binary format as shown in figure 4.

Based on these assumptions, figure 2 shows the position of the cells addressed by stepping through the binary addresses in sequence, rows fast. Several cells are numbered in figure 2 to indicate the sequence. Another way to show the address decoder translation is shown in figure 5. The row address counter counts 4 left to right (arrow a); then during the next 4 counts the

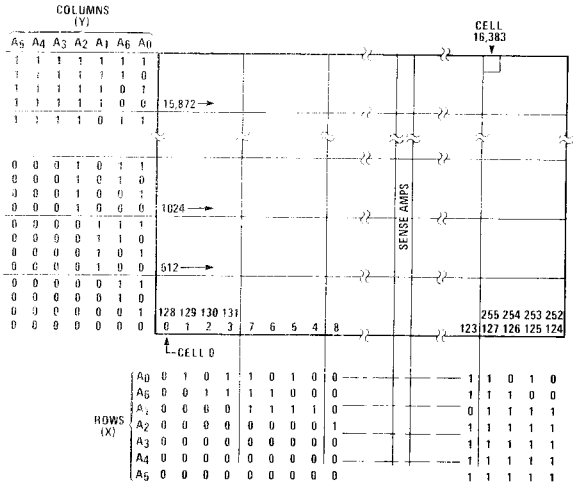


Figure 2. MM5290 Bit Map and Address Decoding

physical connections make it address cells from right to left (arrow b). This left-to-right, right-to-left sequence (in groups of 4) is repeated for 128 rows. The column address counters count in normal sequence starting with 0 at the bottom and up through 127 at the top. If the column address counter increments once for each 128 row count, then all cells of the array are addressed as follows: Column 0 is addressed (in the 4 left-to-right, then 4 right-to-left sequence), then column 1 and on to column 127, where the number of the column corresponds to the decimal equivalent of the binary column address.

Now that we can "follow the map" to any cell location, there is one more step to determine which cells are physically adjacent (as opposed to having sequential or "adjacent" address). Figure 6 shows a simplified sketch of the topology of the MM5290. The orientation (vertical rows, horizontal columns and lower left corner reference) is the same as in the other figures. The decimal numbering of the rows and columns, corresponding to figure 5, are shown. The shaded lines are metal rows. The clear lines are diffused column lines.

Examining the sequencing of the rows shows that rows 3 and 6, 4 and 9, etc., have physically adjacent cells. A test program using sequential binary addressing to assure reading adjacent cells in rows would require reading ±5 rows from the row of interest. Similarly, a column can have diagonally adjacent cells 2 column addresses away so that it requires ±2 columns to assure addressing all physically adjacent cells.

Further analysis indicates that the diffused column lines electrically isolate the cells between them from the rest of the array. Also, one of the adjacent cells (on the left or right) is always connected to the row line of the cell being investigated. This adjacent cell cannot be exercised without refreshing the cell of interest and all other cells in that row. The most practical and efficient disturb testing would exercise only the adjacent cell (on the left or right) not connected to the row line of the cell of interest and the two diffused column lines that isolate the cell in question from the rest of the array.

SUMMARY

The purist will exercise all 8 physically adjacent cells. A pragmatist will exercise the one adjacent cell not connected to the same row and the diffused column lines which isolate the cell. The efficient pragmatist will *not* use sequential binary addressing to exercise only one cell and two column lines when doing a disturb test on a cell.

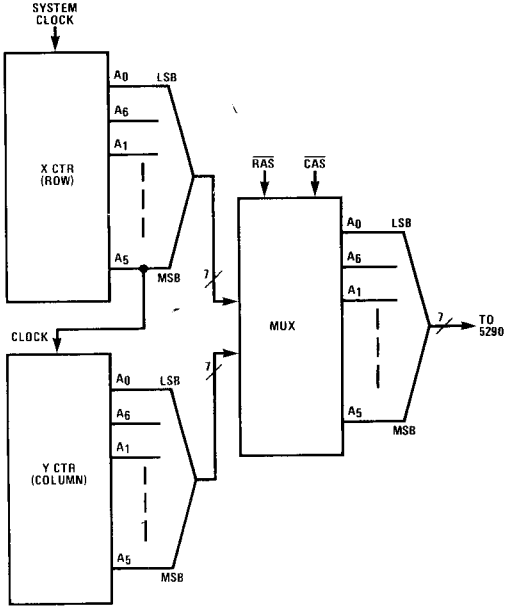


Figure 3. Test System Address Counters Showing X Counter as the "Fastest" Changing Address Counter

CELL NO.	COLUMN (MSB) A_5	A_4	A_3	A_2	A_1	A_6	A_0 (LSB)	ROW (MSB) A_5	A_4	A_3	A_2	A_1	A_6	A_0 (LSB)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
•				•							•			
•				•							•			
•				•							•			
•				•							•			
•				•							•			
•				•							•			
512	0	0	0	0	1	0	0	0	0	0	0	0	0	0
•				•							•			
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16,383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 4. MM5290 Address Coding

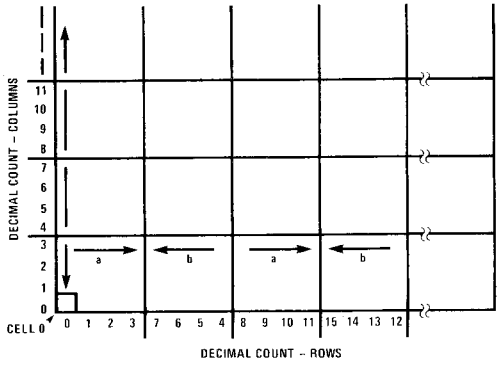


Figure 5. Addressing Bit Location

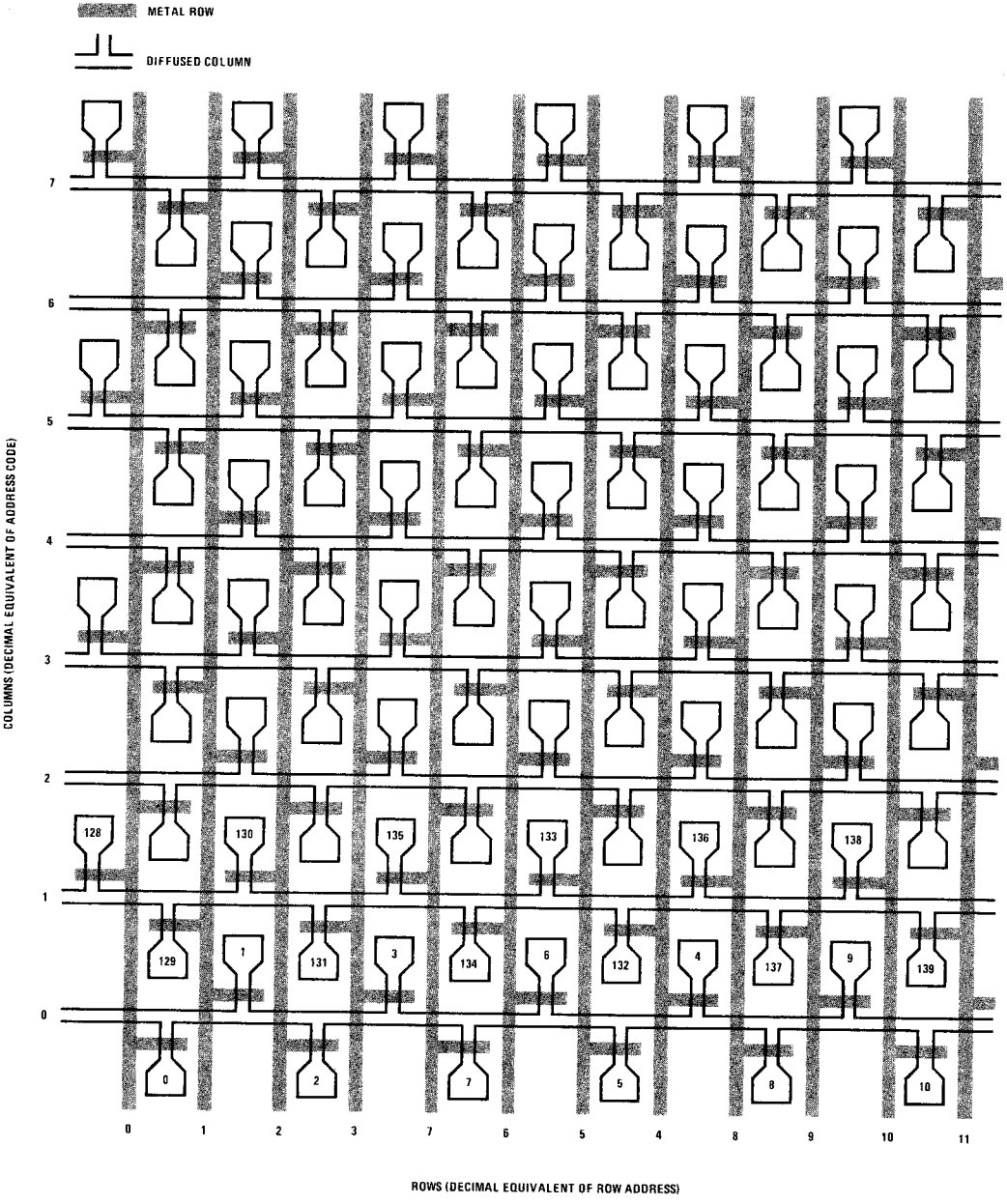


Figure 6. Simplified Topology (lower left corner of array)

MM5290 RAM Test Description

INTRODUCTION

National Semiconductor's 16k dynamic RAM is done with sophisticated computer controlled RAM test systems.

This test description covers the general flow of the MM5290 done to insure a high quality product.

Wafer sort and quality assurance programs generally follow the described parametric and pattern testing and these are not included.

The following points are important to successful testing of the MM5290.

The following V_{BB} rule should be observed to prevent possible damage to a unit under test:

a. Power-up: V_{BB} must be brought up prior to any power supply or input signal.
b. Power-down: V_{BB} must be maintained until all other supplies and inputs have been brought to zero.

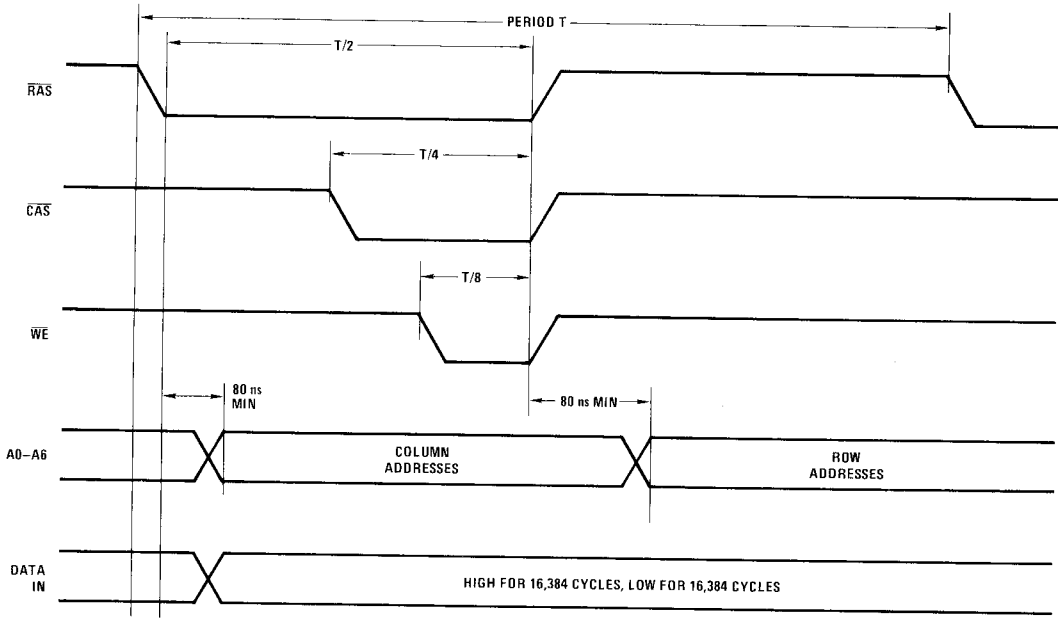
Several cycles are required after power-up *or after the maximum refresh period has been exceeded* before proper device operation is achieved. Any 8 cycles which perform refresh are sufficient.

No input signal (including transients) can be more negative than V_{BB} by 0.5V. This can forward bias the substrate and may cause damage to the device. This should be especially considered in burn-in ovens in which signals may not be well controlled.

Capacitive decoupling at the test fixture should maintain the peak-to-peak transients on V_{DD}, V_{BB} and V_{CC} lines at equal to or less than 400 mV *as measured between the appropriate voltage pin and ground pin on the device under test* (not open socket or the backside of the fixture).

This MM5290 final test description is in a preliminary form. It indicates the flow, the burn-in and the basic intent. It will be several months before the testing of this complex RAM is firmly established. The patterns, correlated limits and timing are all subject to shifts to guarantee a quality part. Notice also that no page mode testing is shown. This will probably only be done if the customer requires it. National currently has test capability in place on the Teradyne J387 test system.

Burn-In Timing

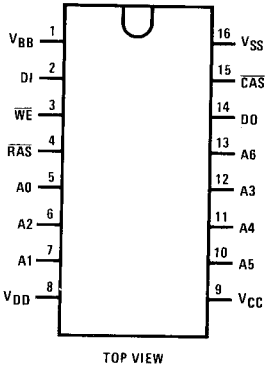


$2.8\ \mu s \leq$ Period T $\leq 5.6\ \mu s$

Note 1: Input timing points: $V_{IH} = 2.2V$, $V_{IL} = 0.6V$.
Note 2: Address lines: $T_R \leq 250$ ns, $T_F \leq 250$ ns.
Note 3: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: $T_R \leq 150$ ns, $T_F \leq 150$ ns.

Burn-In Connection Diagram

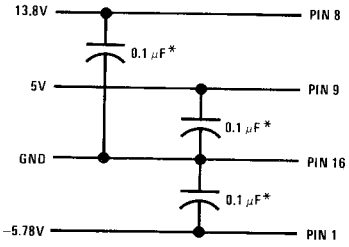
Dual-In-Line Package



TOP VIEW

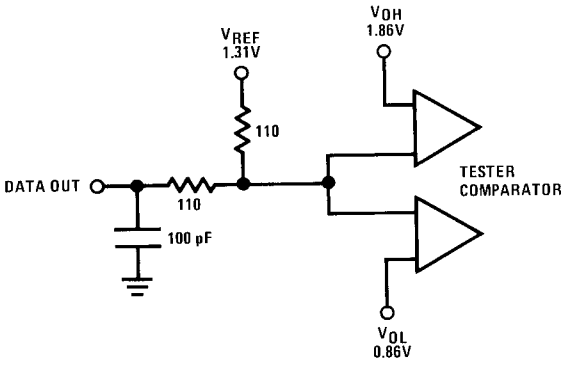
Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0–A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)



*0.1 μF capacitors between 5V and GND, −5V and GND alternate every other socket in each column, 0.1 μF capacitors between 12V and GND every socket.

OUTPUT LOADING

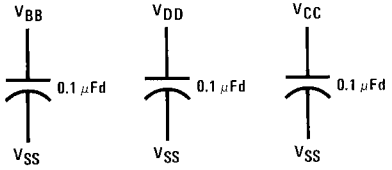


$$I_{SOURCE} = \frac{2.4 - 1.31}{220} = 4.95 \text{ mA}$$

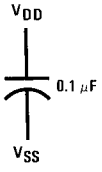
$$I_{SINK} = \frac{1.31 - 0.40}{220} = 4.14 \text{ mA}$$

BYPASS CAPACITANCE

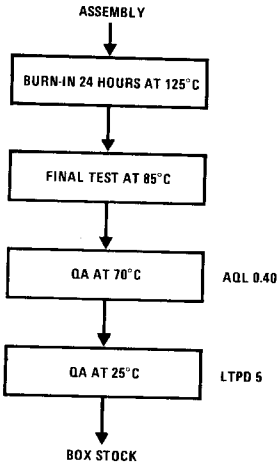
On Handler Backplate



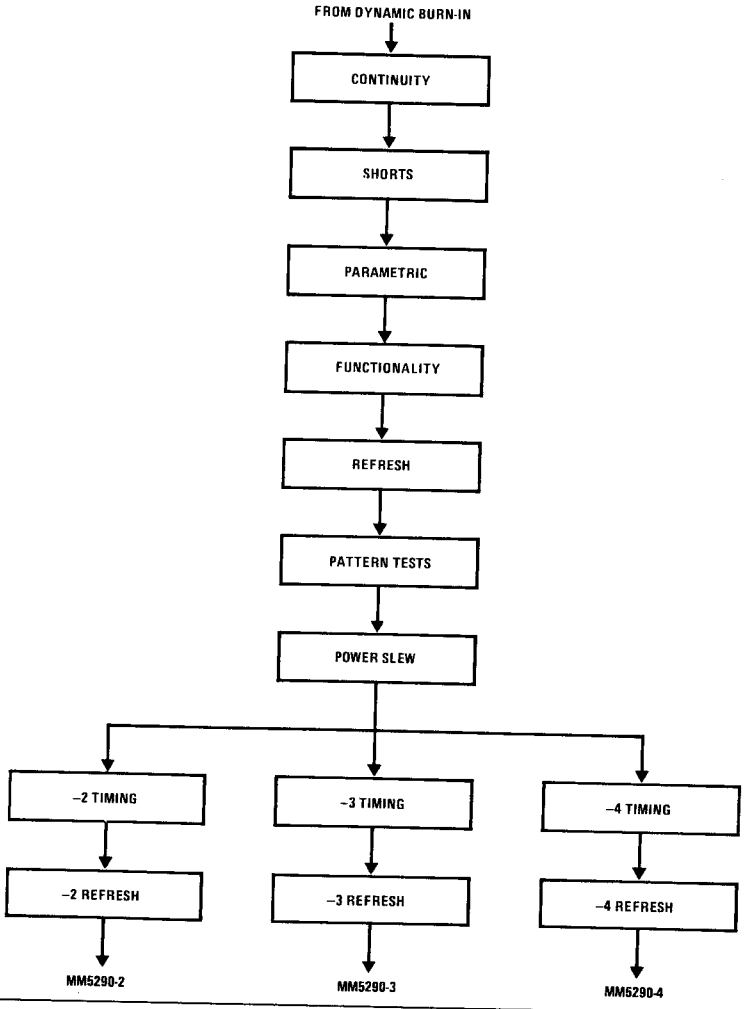
On Siemens Handler Teeth



GENERAL TEST FLOW



FINAL TEST FLOW



Trouble Shooting Check List For Memory Systems Using the MM5280

1. Is CE rise time greater than 10 ns and less than 40 ns? ☐
   Is this true at all points on the board? ☐
2. Does CE meet the min-max V_{IHC} and V_{ILC} spec including ringing at all points on the board? ☐
3. Are the CE on and off time specs being observed? ☐
4. Are the bypass capacitors big enough and close enough so that the power supply variation plus the peak-to-peak noise on the supplies does not exceed the ±5% specifications? ☐
5. Do all TTL level signals reach their respective V_{IH} and V_{IL} levels before CE reaches 2V? ☐
6. Is the output loaded properly? ☐
   No more than one TTL load and no more than 50 pF. Is the V_{CC} bypassed properly? ☐
7. Is the memory being refreshed properly? ☐
   Are all rows (A0 through A5) being refreshed every 2 ms? ☐
8. Are address setup and hold time specs being observed (including CS)? ☐
9. Are address setup and hold times being observed during refresh, including column addresses and CS? ☐
10. Is timing of output data strobe meeting access time spec? Is it being strobed at a time when noise from other signals is at a minimum? ☐
11. Is WE input at V_{IH} level for entire read cycle? ☐
12. Is minimum WE width (t_{WP}) spec being observed? ☐
13. Are the write timing specs (t_{CW} and t_{WI}) with respect to CE being observed? ☐
14. Is the D_{IN} stable early enough before the end of CE in order to meet the t_D spec (150 ns)? ☐
15. Does the data on D_{IN} remain stable until CE has reached 2V at the end of CE? ☐
16. Are the clock drivers bypassed with high frequency capacitors close to the clock driver package? ☐
17. Do the clock drivers have damping resistors? Are they large enough value for the lower CE capacitance of the MM5280? ☐
18. Are the clock lines short to reduce ringing? ☐
19. Are the clock drivers close to the memory array to avoid the impedance mismatch between loaded and unloaded lines? ☐
20. Are data input and output lines running perpendicular to clock lines or at least far away to minimize coupling? ☐
21. Is part being conditioned (refreshed) after power-up? ☐