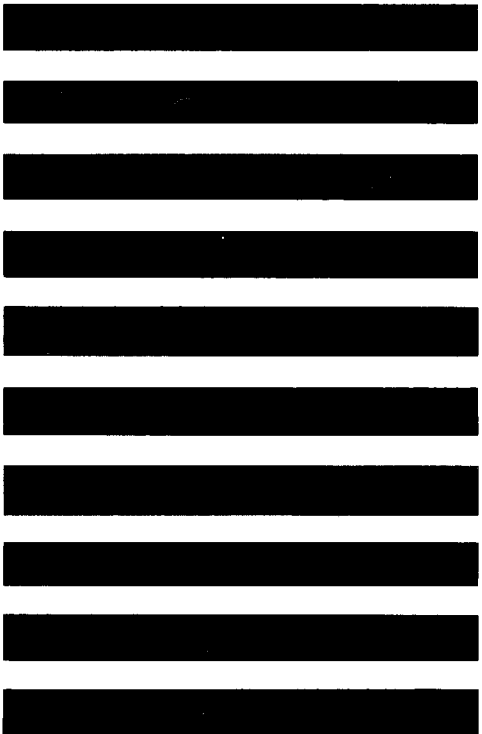


McMOS

INTEGRATED CIRCUITS

Chapter 2

DESIGN INFORMATION



INTRODUCTION

This chapter presents the systems designer with a complete portfolio of Motorola McMOS design information. The information contained will enable the designer to gain a theoretical and practical background of CMOS systems design and implementation. Areas such as powering, operation, physical information, input/output considerations, loading, etc. are presented in significant detail. Interfacing techniques and three-state operating capability expand and highlight the blend of useful design information for the CMOS logic technology.

McMOS POWER SUPPLY CONSIDERATIONS

Three major advantages of the McMOS technology are:

- very low power dissipation,
- wide power supply voltage operating range, and the
- switching threshold remains as a constant ratio (typically 45% of the power supply voltage) throughout the full voltage range of the device.

These three major advantages enable a designer to operate a system designed with McMOS logic from unregulated and/or poorly-filtered power supplies, while at the same time eliminating the special cooling equipment often found to be a necessity in large bipolar systems. In addition, new areas of design in battery-operated and battery-back-up systems have been introduced using the McMOS logic family.

Obviously, an understanding of the limitations and tradeoffs as well as the flexibility of a CMOS system power supply design can provide the designer with a realized savings in total systems costs and also a means of implementing new designs previously not possible using other technologies.

OPERATING RANGE

Motorola McMOS devices are specified in two power supply ranges. The "AL" series (military temperature range devices) is designed to operate with a net potential difference between the V_{DD} and V_{SS} terminals that may vary from 3 to 18 volts. The "CL" and "CP" series (extended commercial temperature range devices) are designed to operate from 3 to 16 volts.

The published maximum allowable operating supply voltage ($V_{DD} - V_{SS}$) appears to be conservative when compared with the maximum 25 to 35 V low-current junction avalanche measurements obtained in the laboratory. Such maximum supply voltages are not really conservative if the device is forced further into avalanche and the secondary breakdown effects are observed, as shown in Figure 2-1. Sustaining currents (I_S) generally vary only from 10 to 50 mA, but such a current jump can be catastrophic to the device. Once in this breakdown mode, in which the power supply differential ($V_{DD} - V_{SS}$) is above the source voltage (V_S), any on-chip current transient having a

value greater than the required sustaining current can forward bias parasitic bipolar devices present in all CMOS devices. The resulting high currents will produce a short circuit reflected at the power supply.

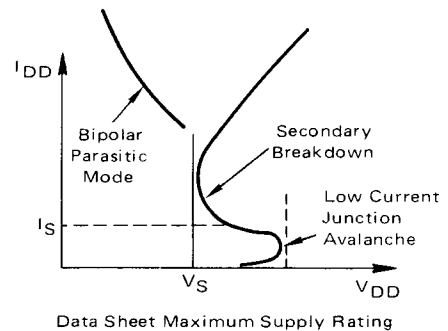


FIGURE 2-1 – SECONDARY BREAKDOWN CHARACTERISTICS

Minimum recommended supply voltage values also require significant consideration. The industry-standard minimum value of 3 V is based on the maximum allowable individual device threshold voltage levels for either P- or N-channel transistors, whichever value is larger. At this minimum value, the CMOS device performs satisfactorily in all "standard" digital logic applications. However, a small but important class of circuit applications exists which require supply voltages greater than the sum of both the P- and N-channel thresholds. Direct feedback circuits such as the linear amplifier and RC oscillator shown in Figure 2-2 represent such applications. In general, caution is necessary when using innovative feedback biasing schemes below a 4 V supply level.

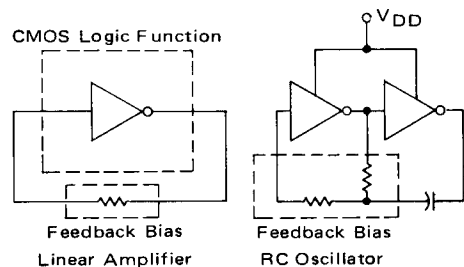


FIGURE 2-2 – LINEAR BIASING SCHEMES

POWER DISSIPATION

Power dissipation in a CMOS device is comprised, in varying degrees, of three basic components:

- quiescent power dissipation, P_Q , (a power dissipation due to surface leakage currents),
- P_{TC} (a power dissipation due to switching through-current), and

- P_L (a CV^2f power dissipation due to the charging and discharging of internal and external capacitances).

Total power dissipation P_T , is the sum of these basic components and is given by the equation:

$$P_T = P_Q + P_{TC} + P_L$$

QUIESCENT DISSIPATION

The first power dissipation component, P_Q (quiescent), is a product of the power supply voltage V_{DD} , and the leakage current I_L , (typically in the nanoampere range). This leakage is due to a combination of surface effects and a network of parasitic diode junctions which are normally reverse-biased and are shown in Figure 2-3(a). The leakage is simulated in the CMOS inverter cross-section shown in Figure 2-3(b).

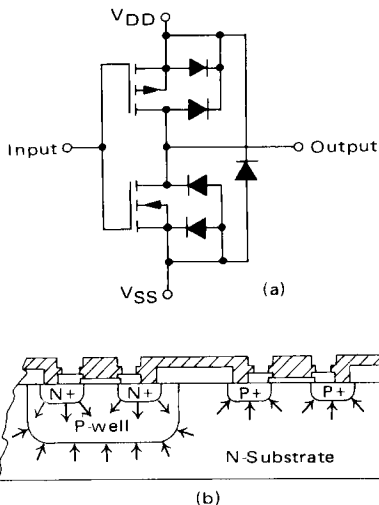


FIGURE 2-3 – LEAKAGE CURRENTS OF P-N DIODE JUNCTIONS

The quiescent power dissipation is extremely low (typically in the nanowatt range) and is usually a negligible portion of the total power dissipation of an operating system. However, many CMOS designs may require long periods of “Standby” operation, during which the logic devices are not actually switching. The worst case power supply drain (often a battery in such a “standby” system) may be calculated by summing the maximum quiescent power dissipation specifications (available in the individual CMOS device data sheet) of all devices within the system.

DYNAMIC DISSIPATION

The remaining two components of power dissipation, P_{TC} and P_L , occur during the dynamic operation of a CMOS device. The through-current dissipation P_{TC} , is a result of current that momentarily flows from the power supply to ground when

a CMOS device switches between logic levels. This through-current I_{TC} is a complex function of the input and output rise and fall times, the input signal frequency, the power supply voltage, and the various parameters (mobility, geometric, channel dimension, etc.) of the MOS transistors.

The through-current I_{TC} has a peak value which can be approximated by the equation:

$$I_{TC} \propto K_0 (V_{DD} - K_1)^2$$

where: K_0 is a constant dependent on the N- and P-channel mobility, geometry, and temperature. The constant K_1 is dependent upon the individual MOS device thresholds. A typical normalized plot of this relationship is shown in Figure 2-4.

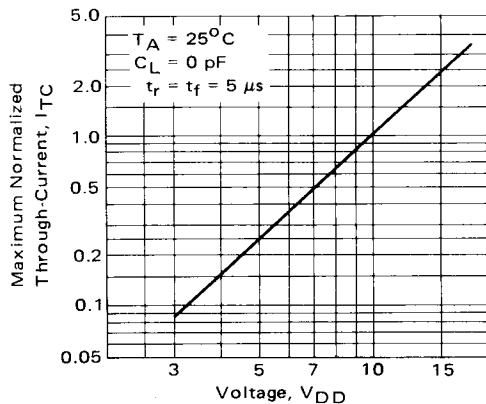


FIGURE 2-4 – NORMALIZED PLOT OF THROUGH-CURRENT VERSUS VOLTAGE

The waveform of the through-current in relationship to the voltage transfer characteristics of a typical inverter pair is shown in the oscillograph, Figure 2-5. The energy contained in the through-current pulse will be a function of the input clock transition time (the time the device remains in the active ON region). The peak current (previously shown in Figure 2-4) can be measured with no-load capacitance. As load capacitance is applied and the input transition time is decreased, the through-current magnitude decreases from its peak value to practically zero as will be described later.

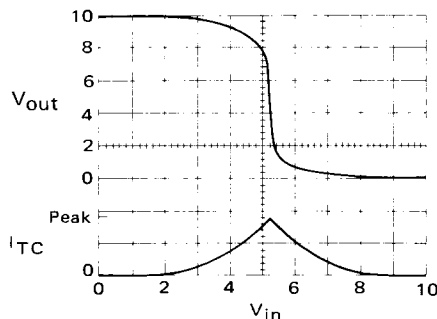


FIGURE 2-5 – THROUGH-CURRENT AND TRANSFER CHARACTERISTICS

The power dissipation, due to through-current P_{TC} , may be theoretically defined as frequency times the integral of the product of the supply voltage and the through-current. This relationship is illustrated by the equation:

$$P_{TC} = f \int_0^{t_r} V_{DD} I_{TC} dt.$$

However, I_{TC} , previously was shown to be:

$$I_{TC} \propto K0 (V_{DD} - K1)^2.$$

Therefore:

$$P_{TC} \propto fKV^N,$$

where: f = frequency,

K = constant (dependent on device parameters),

N = non-integral number greater than 3.

The second component of the dynamic power dissipation, P_L , is proportional to the energy required to charge and discharge the load capacitance C_L and the small internal circuit capacitance. Power is basically defined as energy per unit time. Therefore, the energy storage E of a capacitor is given by the equation:

$$E = 1/2 CV^2.$$

Since the capacitance is alternately charged and discharged through the CMOS device during one complete cycle of the input frequency f , the power P_L is given by the equation:

$$P_L = CV^2f.$$

Thus, the dynamic dissipation increases linearly with the frequency and load capacitance and also as the square of the power supply voltage V_{DD} . Figure 2-6 shows this relationship for a typical CMOS gate.

The power dissipation shown in Figure 2-6 applies for input rise/fall times of 20 nanoseconds. For fast rise and fall times the previously described through-current dissipation P_{TC} is negligible. As the transition times increase, the power (P_{TC}) increases appreciably and is a complex function of the transition times and capacitance.

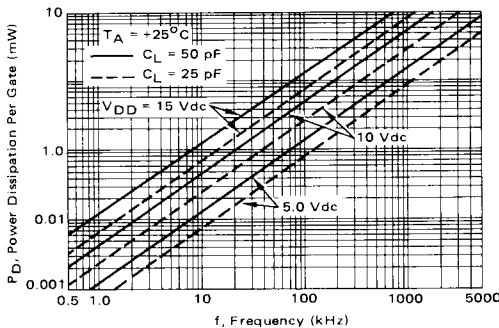


FIGURE 2-6 – TYPICAL GATE POWER DISSIPATION CHARACTERISTICS

Figure 2-7 (a through c) shows the relationship of the power supply current I_{DD} into the device and the ground current I_{SS} out of the device as a function of the capacitance and transition times. The waveforms in (a) show the currents I_{DD} , I_{SS} and I_{TC} for a rise (t_r) and fall (t_f) time of 10 μ s at a 15 pF load. The lesser magnitude of the current pulses (first pulse of I_{DD}) represents the maximum through-current I_{TC} of the device at a given voltage V_{DD} . The increase in amplitude in the current pulse (I_{DD} when V_{out} goes positive or I_{SS} when V_{out} goes negative) is representative of the current required to charge (or discharge) the 15 pF load capacitance. The magnitude of the through-current in (a) is used as the normalizing factor in the current waveforms of (b) and (c).

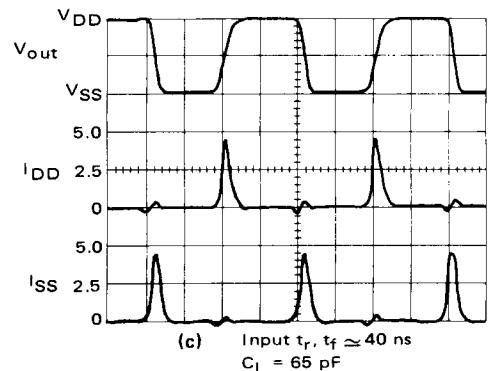
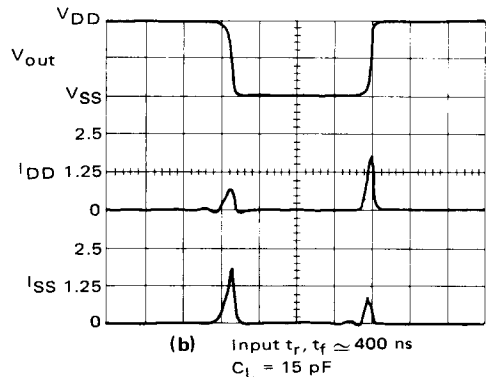
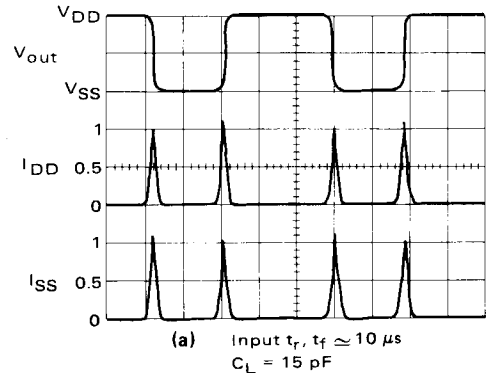


FIGURE 2-7 – SWITCHING CURRENT WAVEFORMS

Oscillograph (b) was made with the same 15 pF load as (a); however, the input transition times (t_r , t_f) are now 400 ns. Again, the smaller current pulses are through-current. The magnitude of the current I_{TC} in (b) has decreased slightly from that in (a). Also, due to the faster transition time, the current pulse width has also decreased. This indicates that some of the charge is being diverted to the load capacitance.

In (c) the capacitance is increased to 65 pF and t_r and t_f are equal to 40 ns. The sinusoidal characteristic of the through-current, present with very fast transition times, is due to the charging and discharging of the parasitic internal capacitances. The previously observed I_{TC} pulse is now almost entirely directed to the load and the dissipation P_{TC} and is negligible when compared with the CV^2f dissipation P_L . The magnitude of the load current has increased for two reasons. First, the load was increased and now requires approximately four times the previous charge. Second, the charge is an integral of this pulse and since the transition times were decreased (hence the current pulse width decreased), the magnitude must increase to supply the same charge.

Figure 2-7 serves to illustrate the relative changes in charging current as a function of load capacitance and also shows the effect of the input transition time on the through-current and the resultant increase in power dissipation. All of the MSI or complex functional McMOS devices have their inputs buffered and thus do not have a severe through-current versus input transition characteristic. However, the system designer should be cautious when using high current drivers with high supply voltages so that the device power dissipation is not exceeded with a long input rise or fall time.

REGULATION AND BATTERY OPERATION

Because of the wide power supply operating range and the constant ratio of the switching threshold to the supply voltage, simple and inexpensive unregulated supplies of the type shown in Figure 2-8(a) may be used to power a system comprised of McMOS devices. The three primary design considerations of such a supply are:

- the voltage level must remain between the minimum and maximum specifications of the device,
- the lowest instantaneous supply level must allow the devices to operate at the necessary maximum system frequency (see the section entitled "Operating Speed Considerations" in this chapter), and
- the filter capacitor must be large enough to supply the peak instantaneous switching current requirements of the McMOS system.

The zener diode D_Z , in Figure 2-8(a) supplies protection by limiting the maximum voltage V_{DD} , supplied to the McMOS system. The resistor R_S , is chosen to supply the peak transient current of the load current, I_L , (plus the required zener

current for maintaining its breakdown) when the input voltage V_S is at the peak value. This design philosophy assumes the transient portion of the load current I_L will charge capacitor C to the zener voltage during the non-switching time of the McMOS system. The current rating on the zener diode D_Z is dictated by the relationship of the equation:

$$I_Z(\max) = \frac{V_S(\text{peak}) - V_Z}{R_S}$$

This assumes the capacitor is fully charged to V_Z and the system is operating in a quiescent (non-switching) mode. The capacitor C is selected by the following equation:

$$C = \frac{q}{V'}$$

where: $q = I_p \{(\text{pulse width}) (N)\} + \{I_Q (t)\}$,

and $V' = V_{\text{zener}} - V_{DD \text{ min}}$.

The required charge q has two components. The major component is the transient peak load current, I_p , times its pulse width multiplied by the number N of transients during the non-conduction period of diode D_1 . The second component is the product of the quiescent current I_Q and the non-conduction time t . V_{DD} is the minimum supply voltage dictated by the specifications of the McMOS devices and the maximum desired operating speed.

A battery back-up supply is easily implemented by replacing the filter capacitor with rechargeable battery as shown in Figure 2-8(b). The battery voltage is selected for the desired operating voltage V_{DD} . The zener diode D_Z has a breakdown voltage greater than the battery voltage and is equal to or less than the maximum V_{DD} McMOS device ratings.

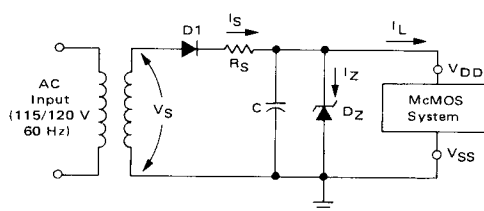


FIGURE 2-8(a) — McMOS UNREGULATED POWER SUPPLY

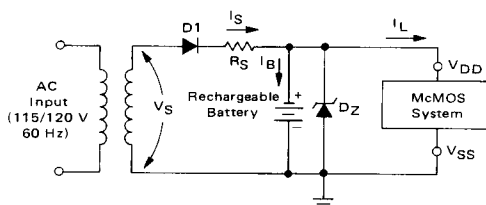


FIGURE 2-8(b) — McMOS BATTERY BACK-UP POWER SUPPLY

In this manner, only the zener conducts and also provides protection during power line transients (which develop voltage spikes due to the battery's characteristic impedance). The resistor R_S in this system supplies the average load current I_L and also a battery "trickle-charge" current I_B . Resistor R_S is calculated by the equation:

$$R_S = \frac{V_{Smax} - V_{battery}}{I_{Lavg} + I_B \text{ ("trickle")}}$$

In the event of a power line failure, the CMOS system can operate for relatively long time periods because of the low dissipation associated with the CMOS family. This type of supply can be used to power CMOS memories and provide a quasi-nonvolatile memory system.

The circuit in Figure 2-9 gives a good indication of how easily a CMOS power supply level can be derived from a high voltage dc source by using a resistor, a zener and a filter capacitor. The zener in this case is actually regulating the voltage rather than providing just overvoltage protection, as in the battery backup supply. Resistor R_S is again calculated from the dc supply voltage, the average load current I_L , and the necessary zener bias current I_Z . The capacitor C, is selected to supply the peak transient load current and maintain the minimum voltage V_{DD} required for the system operating speed.

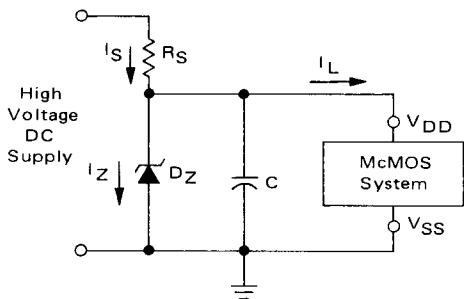


FIGURE 2-9 – DERIVING CMOS POWER FROM HIGH VOLTAGE DC SOURCE

NOISE IMMUNITY

CMOS devices exhibit a sensitivity to only negative-going noise spikes on the power supply line and to only positive-going spikes on the ground. However, bipolar logic families show various degrees of sensitivity to both positive and negative spikes on the power and ground lines, depending upon the output logic state of the device. The sensitivity of the CMOS device will vary as a function of the power supply voltage. This variation is due to the changing of the switching thresholds and the effects of supply voltage on the conductance of the internal MOS transistors. For additional information on noise margins and noise energy immunity of CMOS devices refer to Motorola Application Note AN-707.

THERMAL CONSIDERATIONS

Another advantage realized with CMOS device technology is excellent temperature stability. The "AL" series devices are designed to operate over the full military temperature range of $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$. Additionally, the commercial ceramic "CL" series and the plastic "CP" series package devices are designed to operate over an extended temperature range of $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (standard commercial range is only $0 \leq T_A \leq +70^{\circ}\text{C}$). This extended temperature range is a bonus to designers who do not want to pay the premium price of military temperature range devices for systems that must operate reliably in varying temperature environments. The two major categories of wide temperature range design considerations are package dissipation and specification variations with temperature.

PACKAGE DISSIPATION

CMOS devices consume almost negligible power in the quiescent state and increasing amounts of power in direct proportion to the capacitive load, the operating frequency, and the square of the power supply voltage. A normal CMOS digital system operating at moderate speed does not require special consideration of package dissipation capability.

Special cases invariably arise, however, when the designer is required to extend operation of particular devices to their limits (special load driving, high frequency operation, analog applications, input diode clamping, etc.). In addition, there are specially designed buffers and driver devices that have high current driving capability. Package dissipation and thermal management in these cases may become significant considerations to the designer. Therefore, it is advantageous to know the dissipation capability of standard CMOS packages, as described further.

THERMAL MANAGEMENT

Circuit performance and long term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low. Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. Therefore, the temperature increase depends upon the amount of power dissipated in the circuit and the resulting thermal resistance figure between the heat source and the reference point.

The average temperature at the junction is a function of the system ability to remove heat generated in the circuit (from the junction region to the ambient environment). The basic formula for converting power dissipation to estimated junction temperature is expressed as follows:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA}), \quad (1)$$

or

$$T_J = T_A + P_D (\theta_{JA}), \quad (2)$$

where:

T_J = junction temperature,

T_A = ambient operating temperature,

P_D = calculated power dissipation,

θ_{JC} = thermal resistance, junction to case,

θ_{CA} = thermal resistance, case to ambient,

θ_{JA} = thermal resistance, junction to ambient.

Only two terms on the right side of equation (1) can be varied by the user, namely the ambient temperature, and the device case-to-ambient thermal resistance, θ_{CA} .

Internally, the thermal resistance of an integrated circuit is a function of the package material and size and also the method used in bonding the IC die to the package. The worst case and typical thermal resistance values for some standard IC packages are given in Table 2-1. In Figure 2-10 this basic data is converted into a graph showing the maximum power dissipation allowable at various

Package Description	$\theta_{JA} - ^\circ\text{C/Watt}$ (Still Air)		$\theta_{JC} - ^\circ\text{C/Watt}$
	Worst Case	Typical	Worst Case
Plastic Dual-In-Line, 14 lead or 16 lead (Gold Eutectic Die Bond)	200	135	90
Ceramic Dual-In-Line, 14 or 16 lead (Gold Eutectic Die Bond)	155	100	50
Ceramic Dual-In-Line, 24 lead	100	70	35
Plastic Dual-In-Line, 24 Lead	140	95	50

TABLE 1 – WORST CASE AND TYPICAL THERMAL RESISTANCE RATINGS FOR SELECTED IC PACKAGES.

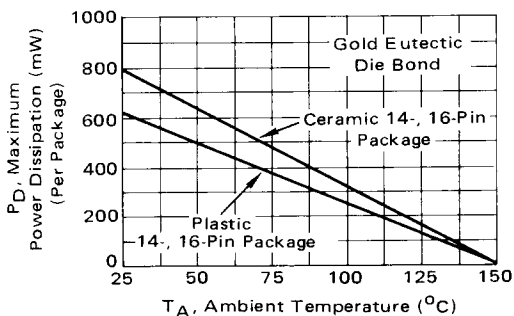


FIGURE 2-10 – AMBIENT TEMPERATURE POWER DERATING

ambient temperatures for circuits mounted in the 14-pin and 16-pin plastic and ceramic packages; the data also considers the maximum permissible junction temperature for devices packaged in plastic or ceramic. These measurements are taken in still air without heat sinks, since moving air and heat sinking would decrease the value of θ_{CA} .

SPECIFICATION VARIATION WITH TEMPERATURE

The fact that a logic family is designed to functionally operate over a wide temperature range does not necessarily mean that specifications will not vary with changes in the ambient temperature. A quick glance at the electrical characteristics section of a data sheet will verify that parameters such as output drive, quiescent power dissipation, and switching time parameters do indeed vary with temperature. Fortunately, these variations are predictable enough that a designer, with information included in this section, can interpolate and extrapolate the performance of the selected CMOS devices over their full temperature rating.

VOLTAGE TRANSFER CHARACTERISTIC VARIATIONS

An inherent advantage of the generic complementary MOS process is the tendency of the N- and P-channel thresholds to "track" together over wide temperature variations in such a manner that the input threshold to a CMOS device remains quite constant. As seen in Figure 2-11, the variation of threshold over the full military temperature range is typically less than five percent. By comparison, a bipolar threshold may vary as much as 40 percent.

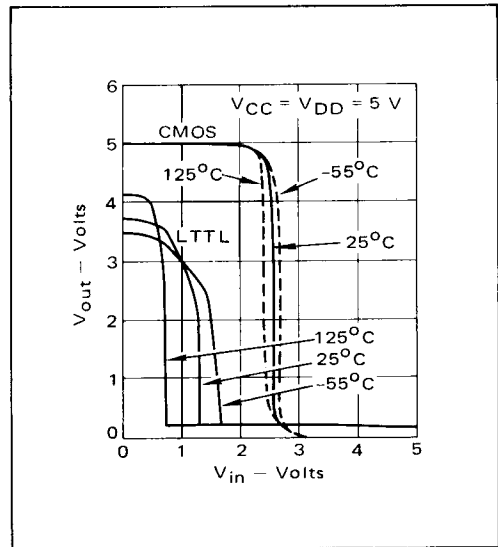


FIGURE 2-11 – TRANSFER CHARACTERISTICS OF THE CMOS INVERTER SHOWS MUCH LESS DEPENDENCE ON TEMPERATURE THAN DOES TTL.

Threshold variation over temperature becomes an important factor when determining worst case noise margins, but it is of greater concern in quasi-analog circuits such as 2-gate oscillators and "one-shot" multivibrators. The threshold levels in these types of circuits directly affect frequency, duty cycle, and time-out. Therefore, the stability of CMOS devices over temperature is a definite advantage in these "special" applications.

LEAKAGE CURRENT VARIATIONS

Leakage current plays an important role in quiescent power supply and three-state loading considerations. When designing a circuit which must operate over wide temperature ranges, the effect of temperature on leakage must be considered in worst case design.

Leakage, as previously described, is due primarily to internal reverse-biased P-N junction leakage. As such, the leakage increases exponentially with increasing temperature, as indicated by the formula:

$$I_L = (T_1) = I_L(T_0) e^{\Delta T/K},$$

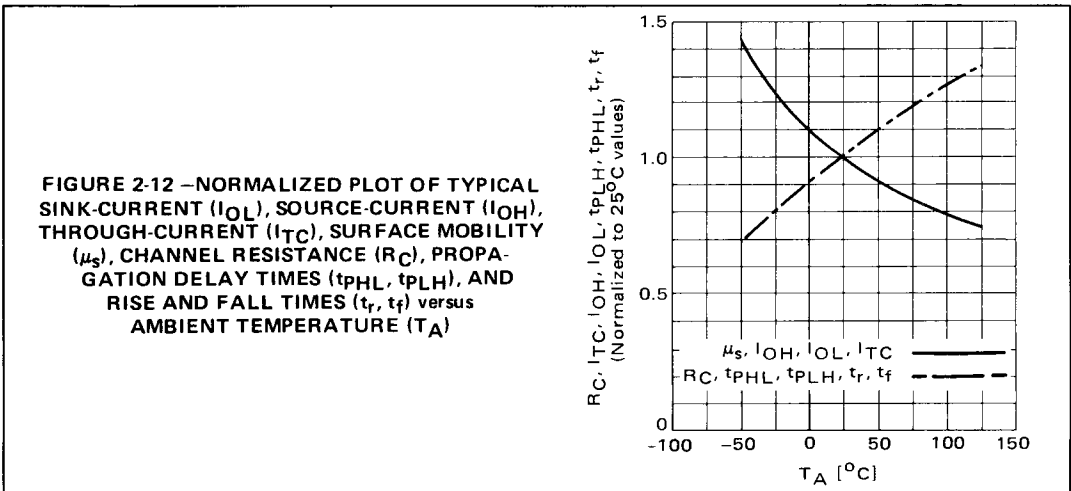
where $I_L(T_0)$ is the leakage current measured at temperature T_0 , K is the constant of the rate of increase, and the temperature change is $\Delta T = T_1 - T_0$.

The channel resistance of an MOS device is inversely proportional to the surface mobility of the majority carriers (holes in a P-type device and electrons in an N-type device). Since the mobility is a function of temperature, it is not surprising to find that channel resistance and thus, the current and switching time parameters change with variations in temperature.

The normalized graph of the current and switching parameters versus ambient temperature, Figure 2-12, should prove a useful tool to the designer in predicting the typical performance to be expected of a CMOS circuit at different temperatures.

INPUT RATINGS AND CONSIDERATIONS

The input of a Complementary MOS device is insulated from the MOSFETs channel regions by a thin layer of silicon dioxide (SiO_2). The high impedance and a 5 picofarad input capacitance make unconnected or floating inputs excellent energy storage nodes having the potential for large voltage buildups. The Motorola CMOS process uses resistor-diode gate-protection networks to siphon the accumulated energy away from the MOS transistors and thereby prevent permanent damage to the input gate oxide regions. In addition to



For silicon junctions, I_L doubles approximately every $10^\circ C$, thus making $K_{Si} = 14^\circ C$. A CMOS device that has 5×10^{-9} ampere leakage at room temperature ($25^\circ C$) may be expected to have 5×10^{-6} ampere leakage at $125^\circ C$.

CHANNEL RESISTANCE EFFECTS

Variations in the channel resistance of the P-type and N-type MOSFETs in a CMOS circuit affect several important device characteristics, namely current sinking and sourcing capability (I_{OL} , I_{OH}), switching through-current (I_{TC}), propagation delay (t_{PHL} , t_{PLH}), and output voltage rise and fall times (t_r , t_f).

device handling precautions, other user considerations include device maximum ratings, termination of unused inputs and input signal waveforms.

INPUT VOLTAGE

To prevent a destructive high-current mode, caused by forward biasing the input protection diodes, the signal voltage V_{in} must be confined to the range of $V_{SS} \leq V_{in} \leq V_{DD}$. The input thresholds establish the maximum input LOW signal voltage V_{NL} , and the minimum input HIGH signal voltage V_{NH} . These thresholds are specified as a dc noise margin and are defined as the maximum

voltage change from an ideal logical "1" or "0" input level, which will not produce a change of state at the output. The guaranteed noise margin for standard Motorola CMOS devices is 30% of V_{DD} with a typical value of 45% V_{DD} .

To illustrate, the ideal "0" and "1" input levels are V_{SS} and V_{DD} , respectively. Therefore (using positive logic notation), using the formula $V_{IL} = V_{SS} + 0.3 V_{DD}$ equals the guaranteed minimum maximum input logic "0" threshold level, and V_{IH} is equal to $0.7 V_{DD}$ or the guaranteed maximum minimum input logic "1" level. Typical values are: $V_{IL} = V_{SS} + 0.45 V_{DD}$, and $V_{IH} = 0.55 V_{DD}$.

The calculations relate that if the input level V_{in} is in the range $V_{SS} \leq V_{in} \leq V_{SS} + 0.3 V_{DD}$, the output level V_O is guaranteed not to have changed state and will be within the range of $0.7 V_{DD} \leq V_O \leq V_{DD}$ for inverting functions, or within the range of $V_{SS} \leq V_O \leq V_{SS} + 0.3 V_{DD}$ for non-inverting functions. For a further description of thresholds and noise margin see Motorola Application Note AN-707.

INPUT CURRENT

The very high input impedance (typically 10^{12} ohms) requires an almost negligible source or sinking drive. The typical input current I_{in} , is 10 pA dc. However, there are many system designs that utilize the input protection diodes to clamp the signal levels. In these applications, it is necessary to limit the input currents to the ± 10 mA dc maximum rating per package pin. This 10 mA maximum rating also applies to the V_{DD} and V_{SS} pins. Therefore, if the device has four inputs (all of which may be HIGH forward-biasing the input diodes) the current limit on each input would be 10 mA divided by 4 or 2.5 mA. The same reasoning applies if more than one input is below the V_{SS} level.

UNUSED INPUTS

A problem associated with floating CMOS device input pins occurs after the device is installed in an operating system. Energy injected through stray external circuit wiring capacities produces unpredictable, time-varying input values. Power dissipation increases, since the input gates tend to spend more time in their active, biased-ON region. As a result, the uncertainties of the gate logic states combine and cause system failure. This problem is eliminated if all unused CMOS input pins are connected to the appropriate power supply bus.

The proper termination level is determined by the truth table of the device being used. In the case of multi-input gates, it is recommended that unused NAND inputs be connected to V_{DD} and unused NOR inputs be connected to V_{SS} . This will improve reliability and provide maximum device input performance. If an entire gate or portion of a device is not used, it is still necessary to terminate the inputs even though the output is not loaded.

INPUT RISE/FALL TIMES

Special consideration must be given to the specified worst case maximum (slowest) clock input rise and fall times for edge triggered devices such as flip-flops, shift registers and counters. The specified values vary from 5 μ sec to infinity and the system designer should consult the device data sheet for this parameter. A description of input waveforms will be presented later.

INPUT PROTECTION NETWORKS

The system designer must remain aware that MOS devices can be seriously damaged if subjected to high electrical fields in the gate oxide regions. Normally the gate oxide is 1000 \AA to 1200 \AA thick; this range also defines a maximum potential difference that can be tolerated across the gate oxide. The gate oxide breaks down at a gate-to-substrate potential of about 100 V and results in permanent damage to the device.

Unfortunately, the electrical environment during pc board or socket insertion and device handling is very hostile. For example, static voltages generated by a person walking across a common waxed floor, have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). These static voltages are potentially disastrous when discharged into a CMOS input considering the energy stored in the capacity (≈ 300 pF) of the human body at these voltage levels. There are two methods used for input protection: a single diode protection method and a double diode-resistor configuration. Both methods provide adequate input protection and all CMOS devices use one of these two protection methods.

Present CMOS gate protection structures can generally only protect against overvoltages in the hundreds of volts range. This is usually sufficient for "in-socket" overvoltage, but an order of magnitude less than that typically found in the handling environment. Following are some suggested handling procedures for CMOS devices.

- Store unused devices in conductive foam, conductive rails, or connect all leads together using a similar electrical shorting method.
- Use grounded tip soldering irons.
- Ground all test equipment.
- All low impedance equipment (such as pulse generators, etc.), should be disconnected from device inputs before dc power supplies are turned-off.
- All unused device inputs should be connected to V_{DD} or V_{SS} .

SINGLE DIODE METHOD

Figures 2-13(a) and 2-13(b) show the single diode protection method. Since the P-tub and the N-substrate are lightly doped, the junction breakdown is high and typically 120 V. Therefore, a heavily doped N+ region and a lightly doped P-region are used for the diodes. The junction between

these two regions (N+ and P-) breaks down at approximately 30 V, and is well below the 100 V gate-to-substrate breakdown.

The single diode method provides protection by clamping positive levels to V_{DD} . Negative protection is provided by the 30 V reverse breakdown. The diode is designed to operate in the breakdown region without damage, provided currents are kept under 10 mA.

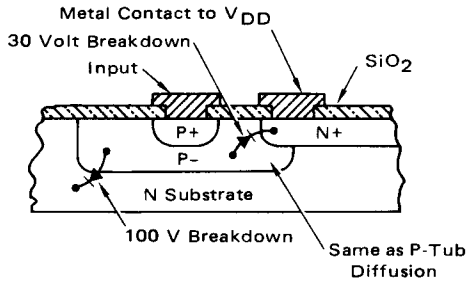


FIGURE 2-13(a) – PHYSICAL DIAGRAM, SINGLE DIODE PROTECTION METHOD

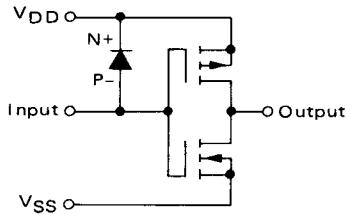


FIGURE 2-13(b) – SCHEMATIC DIAGRAM, SINGLE DIODE PROTECTION METHOD

DIODE-RESISTOR METHOD

The second method, while adding some delay time, provides protection by clamping positive and negative potentials to V_{DD} and V_{SS} , respectively. Figures 2-14(a) and 2-14(b) show the circuitry and diffusion cross-section for the diode-resistor protection method.

The input protection circuit consists of a series isolation resistor R_S , whose typical value is 1.5 k ohms, and diodes D1 and D2, which clamp the input voltages between the power supply pins V_{DD} and V_{SS} . Diode D3 is a useful distributed parasitic structure resulting from the diffusion fabrication of R_S .

In addition to circuit isolation, the series resistor R_S produces a small propagation delay due to the 5 pF gate capacitance. This delay (typically 6 to 7 ns) allows excess energy present at the input terminal to be diverted through the protective diodes before reaching the sensitive gate dielectric.

Diodes D1 and D2 are both of the N+, P- type and have a sharp 30-35 volt avalanche breakdown characteristic. Positive (breakdown mode) and negative (forward conduction) overvoltage protection,

with respect to V_{SS} (V_{DD} – open circuit), is provided by diode D1. Diode D2 similarly provides positive (forward conduction) and negative (breakdown mode) overvoltage protection with respect to V_{DD} when V_{SS} is left open. Both diodes limit the applied voltages to well within the critical breakdown potentials of the gate dielectric.

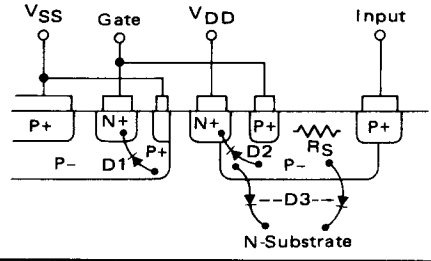
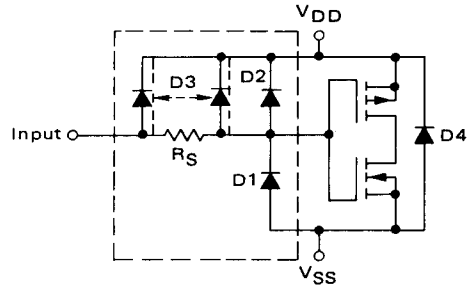


FIGURE 2-14(a) – PHYSICAL DIAGRAM, DIODE-RESISTOR INPUT PROTECTION METHOD



Added Protection Circuitry At Each External Input lead

Notes:

$R_S = 1.5 \text{ k}\Omega$ Nominal

Avalanche Voltages:

BVD1 = 30 V

BVD2 = 30 V

BVD3 = 80 V

BVD4 = 120 V

FIGURE 2-14(b) – SCHEMATIC DIAGRAM, DIODE-RESISTOR INPUT PROTECTION METHOD

USING THE INPUT DIODES IN CIRCUIT DESIGN

Circuits such as integrators, differentiators and oscillators may forward bias the input protection diodes and actually depend on them to clamp the input signal levels. The forward bias currents generated by such circuit configurations is limited by the impedance and drive capability of the driving device and generally will not exceed the input limitations.

An application that requires consideration, as to the single diode versus the diode-resistor input method, is the two stage oscillator shown in Figure 2-15.

Waveforms for the single diode input network show that the diode clamps the input voltage V_1

to the positive V_{DD} voltage. The negative portion of V_1 is not limited (the protection diode has not avalanched) and will go negative with respect to V_{SS} by the magnitude of the threshold voltage V_T . This effect will cause the time t_1 to be less than time t_2 and will give the output waveform V_O a duty cycle less than 50%.

The waveforms for the diode-resistor input method show that the input signal V_1 is limited to both the V_{DD} and V_{SS} supply voltages. In this case, times t_1 and t_2 are approximately equal, the duty cycle is 50% and the output period T is less than the period of the output for the single diode device.

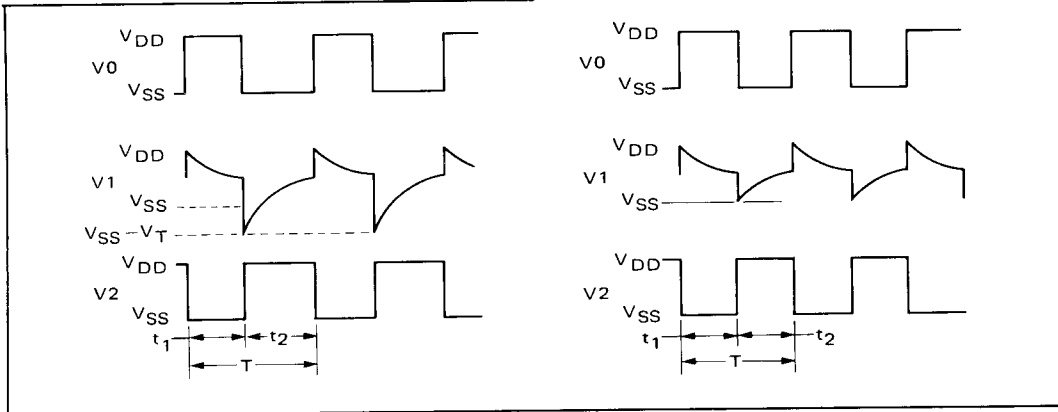
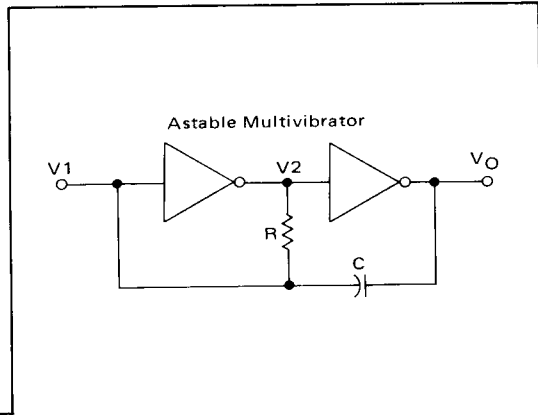


FIGURE 2-15 – WAVEFORM COMPARISON OF INPUT METHODS

Figure 2-16 shows the same astable circuit as Figure 2-15 with the addition of a compensating resistor R_S . Besides compensating for input threshold and power supply variation, resistor R_S also provides isolation from the input protection network. The waveforms illustrate that times t_1 and t_2 are approximately equal and the period T will not vary (as a function of the type of protection circuit the input device has).

The inputs to CMOS devices can be driven with signals outside the range of V_{SS} to V_{DD} if a series resistor is used to limit the current to less than the 10 mA maximum. However, consideration must also be given to the increase in rise, fall and propagation delay times produced by the series resistance and the 5 pF input capacitance. This technique obviously should not be used on the inputs of edge-triggered devices. It is recommended that the inputs be buffered by an additional gate for these devices.

The 10 mA input current limit is established by the device internal metalization. Exceeding the 10 mA limit will cause metal migration and possible long term degradation of the device lifetime.

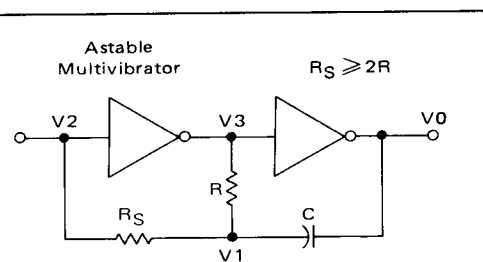
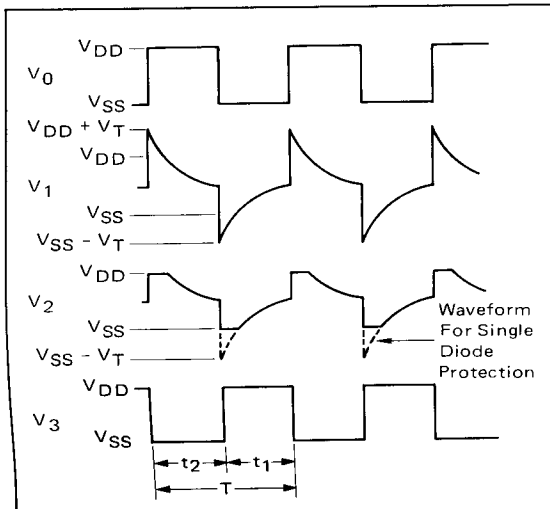


FIGURE 2-16 – DIODE-RESISTOR INPUT METHOD WITH ADDITION OF COMPENSATING RESISTOR R_S

INPUT WAVEFORMS

The 10 to 90% maximum clock transition time for sequential circuits is normally specified in the 5 to 15 μsec range, depending upon the supply voltage used; data ripple-through, false triggering problems, etc. occur above these values. As the system transition times approach these limits, potential timing problems and increased power dissipation levels should be considered.

The possible 15 to 20% process variation in input threshold voltage among random device samples could lead to clock-skew problems, even in synchronous logic systems where clocking is not normally a problem.

As in the example in Figure 2-17, a fairly long clock rise time could produce data ripple-through on the cascaded edge-triggered storage elements. As long as the edge-sensitive clock transition time (t_{rC}) is confined to a value of less than the sum of the propagation delay time of the driving output stage (for the estimated capacitive load) and of the hold-time of the following parallel clocked device as shown in Figure 2-17, there will not be a problem.

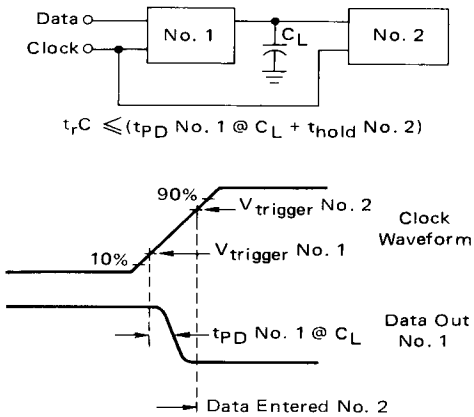


FIGURE 2-17 — SYNCHRONOUS OPERATION LIMITED BY CLOCK TRANSITION TIME

The maximum t_{rC} transition time due to skew effects could be in the 100 nsec range for the worst case situation of high speed devices having maximum allowed threshold voltage deviations. As clock transition times increase, system power needs also increase; this action results because the logic elements are exhibiting longer periods of time in the active (higher power) operating region.

Schmitt trigger circuit configurations can be utilized for wave shaping very slow external input signals and also provide a decrease in input power dissipation and an increase in overall system performance. The MC14583 dual Schmitt trigger is an ideal solution to applications requiring such wave shaping. Other Schmitt trigger designs can be found in the articles referenced in the supplementary literature section of this data book.

Several of the CMOS counter and shift register designs incorporate input circuitry having a Schmitt trigger type hysteresis which also eliminates the requirement of a maximum input rise time specification. These counters are very useful for generating a system clock from the common 60 Hz power line frequency. The inputs of such devices can be connected directly to the 120 Vac line through a series connected 1 megohm resistor. A capacitor must also be added between the device input and the V_{SS} pins to absorb the kilovolt line spike energy commonly found on many power lines. The rectification of the ac input voltage is again performed by the internal protection diodes and the current is limited by the series resistor.

OUTPUT LOADING CONSIDERATIONS

Like any logic family, CMOS is limited in the amount of current (sink and source) drive capability while still maintaining a defined logic state. CMOS device output current characteristics are found in a set of curves (refer to Figure 2-18) defined as output drain characteristics. The logic designer should consult these curves when designing specialized systems requiring high current drives. These drain characteristics vary as a function of voltage and temperature and have an effect on the maximum operating speed of the logic system.

OUTPUT CHARACTERISTICS

As shown in Figure 2-18, CMOS N- and P-channel enhancement mode transistors have two basic regions of operation, saturated and non-saturated. The boundary between the two regions is the locus of points at which the drain-to-source voltage (V_{DS}) is equal to the gate-to-source voltage (V_{GS}) minus the device threshold voltage (V_T).

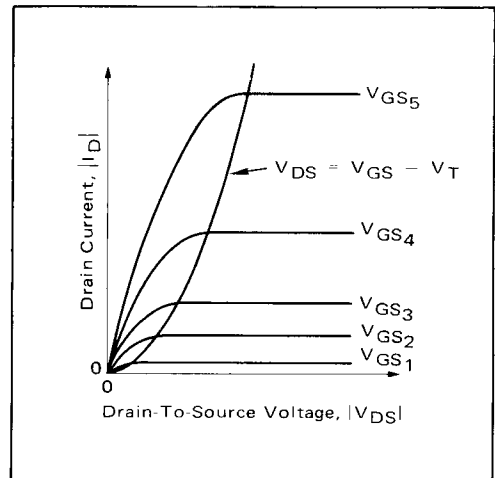


FIGURE 2-18 — OUTPUT DRAIN CHARACTERISTICS

In the non-saturated region, the characteristics of the MOSFET are similar to a resistor; the impedance of the channels is approximated by the slope of the curves. The current in this region is given by the equation:

$$I_D = 2K (V_{GS} - V_T) V_{DS} - K V_{DS}^2,$$

where K is a constant dependent upon processing parameters and the channel geometry.

In the saturated region, the MOSFET behaves similar to a current source as illustrated by the constant drain current independent of the drain-to-source voltage. The currents in the saturated region are given by the equation:

$$I_D = K (V_{GS} - V_T)^2.$$

The maximum drain current I_D is almost proportional to the square of the gate-to-source voltage V_{GS} . In Motorola CMOS logic, the gate-to-source voltage is limited to the power supply voltage ($V_{DD} - V_{SS}$). Hence, it can be stated that the drive capability of CMOS is proportional to the square of the power supply voltage.

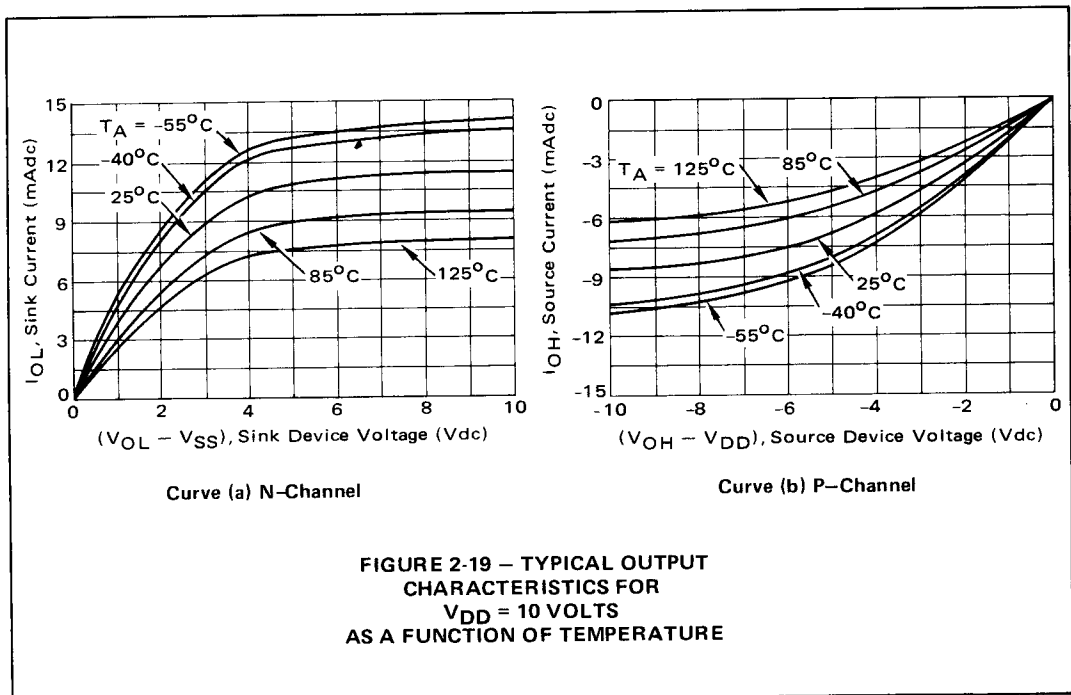
The output drain characteristics also vary as a function of temperature as shown in Figure 2-19. The typical characteristics for a standard CMOS output N-channel device, operating with a supply of 10 volts, is shown in Figure 2-19(a). The complementary P-channel characteristics are shown in Figure 2-19(b). For device temperatures above 25°C, the decrease in drain current can be approximated by a negative temperature coefficient of approximately -0.3%/°C. Refer to Figure 2-12 for a curve of the change in drain current versus temperature.

CONSIDERATIONS AND PRECAUTIONS

The standard CMOS input is capacitive and requires approximately ± 10 pA of drive current. Thus, the fan-out on a current basis is in the order of 10^6 devices. The actual fan-out of a CMOS device is limited only by a capacitive load consideration based upon the desired system operating frequency.

Assume that a capacity-loaded CMOS gate has an input signal with almost zero transition time. The output device then charges (or discharges) the load capacitance along the drain characteristic curve for V_{GS} and exits from the saturated region ($V_{DS} = V_{DD}$) to the non-saturated region ($V_{DS} = 0$). This means that initially the voltage across the capacitor changes in a linear fashion due to the constant current $I_D(\text{sat})$. As the drain-to-source voltage V_{DS} decreases to less than that defined for saturation, the current to the load decreases. At this point, the voltage change on the capacitor is no longer linear and, as a result, slows down "rounding off" the rising or falling output waveform as it approaches its limits of V_{DD} or V_{SS} , respectively.

Since the capacitance $\frac{dv}{dt}$ is a function of drain current I_D , the output rise/fall times and also the system operating speed will be limited by the CMOS supply voltage. Operating temperature, because it effects the maximum drain current, will also limit system speed. Considerations on system speed with respect to capacitance, voltage and temperature will be described later in Chapter 2 under the heading Operating Speed.



The outputs of a CMOS device consist of a complementary pair, one device for sourcing current and another for sinking current. The outputs of a CMOS device cannot be connected in a "wire-OR" configuration because of the complementary pair configuration. Three-state logic will be described later in Chapter 2.

Many times temporary shorts result from testing mistakes or improper board assembly. When such excessive currents flow and the chip temperature increases, the short circuit current will decrease because of the negative temperature coefficient. This "built-in" thermal protection will usually prevent burn-out on a short term basis. In general, devices with standard family output characteristics can be shorted to the supply rails, provided the supply voltage is 5 volts or less; at this supply voltage, saturation currents are less than the maximum device ratings of 10 mA per pin. Precautions are necessary when using the high current buffers or operating with high supply voltages so that the maximum device current and dissipation limits are not exceeded.

The CMOS drive capability is limited if the outputs are required to maintain a specified logic level. However, if the output is used to drive a discrete device such as a transistor or LED, large currents (within maximum ratings) can be achieved by operating the device in the saturated region. Details on interfacing to other devices will be described shortly.

INTERFACING TECHNIQUES

There are many digital system designs which require low-power dissipation CMOS devices to be integrated with devices of other semiconductor technologies. This raises the question of how to interface between CMOS and other logic families. Most logic families have a compatible set of input-output parameters defined in terms of family unit loads specified at a restrictive or tight tolerance power supply voltage. The CMOS guaranteed power supply operating range of 3 to 18 volts encompasses all of the significant logic families available today. This operating range, together with the simplicity of the input and output characteristics, makes the CMOS technology particularly easy to interface with devices of other technologies. The interface techniques to be described assume the following initial conditions.

1. The power-supply voltage level and tolerances are chosen to accommodate the interfaced logic elements, since CMOS integrated circuit devices will operate over a much wider voltage range.
2. The logic levels at the interface between CMOS and other logic elements will meet or exceed the specified worst case logic levels of the other elements.
3. Fan-in and fan-out rules at the interface shall be derived from the current sinking or sourcing capability of the driving elements.

By adopting these three conditions, the designer can ensure appropriate noise margins at the interface between dissimilar elements.

INTERFACING CMOS WITH TTL, DTL

Since both the DTL (diode-transistor logic) and TTL (transistor-transistor logic) bipolar digital IC families require only a single supply, CMOS devices are well-suited for use with DTL and TTL logic forms. There are two major considerations when interfacing CMOS with bipolar logic elements. The first consideration is whether CMOS can sink the input current requirement of the bipolar logic. The second consideration is whether the output logic levels of the bipolar devices are compatible with the CMOS input threshold levels.

Figure 2-20 shows the input/output level and current requirements of CMOS/bipolar interfaces. For a logic "0" input, the standard medium power TTL and DTL devices have a current sink drive requirement of 1.6 mA at a level of 0.4 volts. Standard gate CMOS devices will not sink 1.6 mA of current. To increase the output current sinking capability of the CMOS device, a 2-input or 4-input CMOS NOR gate could be used with all the gate inputs tied together in parallel. For higher fan-outs, the use of buffer devices (as shown in Figure 2-20) is recommended. These buffers are capable of driving two medium power TTL or two DTL loads with an I_{OL} of 3.2 mA at 0.4 volts. By paralleling the inputs and outputs of the CMOS buffers, even large fan-outs can be obtained. The logical "1" output of any CMOS device has no difficulty driving any TTL or DTL device since the V_{OH} level of 4.5 volts (while sourcing the micro-ampere leakage of the bipolar devices) is 2.5 volts higher than the 2.0 volt V_{IH} input level.

Low-power TTL (LTTL) logic requires a current sinking drive of 0.18 milliamperes at a voltage level less than 0.3 volts. As shown in Figure 2-20, any standard gate CMOS device will drive one LTTL load over the full military temperature range. However, in most cases, two LTTL loads can be driven over the full temperature range. Further, at 25°C any CMOS device will typically drive 4 LTTL loads without burden. The Motorola CMOS buffers are capable of at least 10 LTTL loads over the full temperature range. In the non-saturated mode, as is the present case, the drain current is directly proportional to the drain to source voltage. Therefore, higher fan-outs than the number guaranteed on the data sheet can be obtained with some sacrifice in noise immunity over extended temperatures.

When interfacing bipolar logic to CMOS, the primary consideration is whether the bipolar output levels are compatible to the CMOS input thresholds. The guaranteed CMOS thresholds for a logic "0" or "1" input are respectively 30% and 70% of the power supply voltage; further, with a 5 volt supply this is 1.5 volts and 3.5 volts, respectively. The bipolar V_{OL} level of 0.4 volts is more than capable of driving a CMOS device

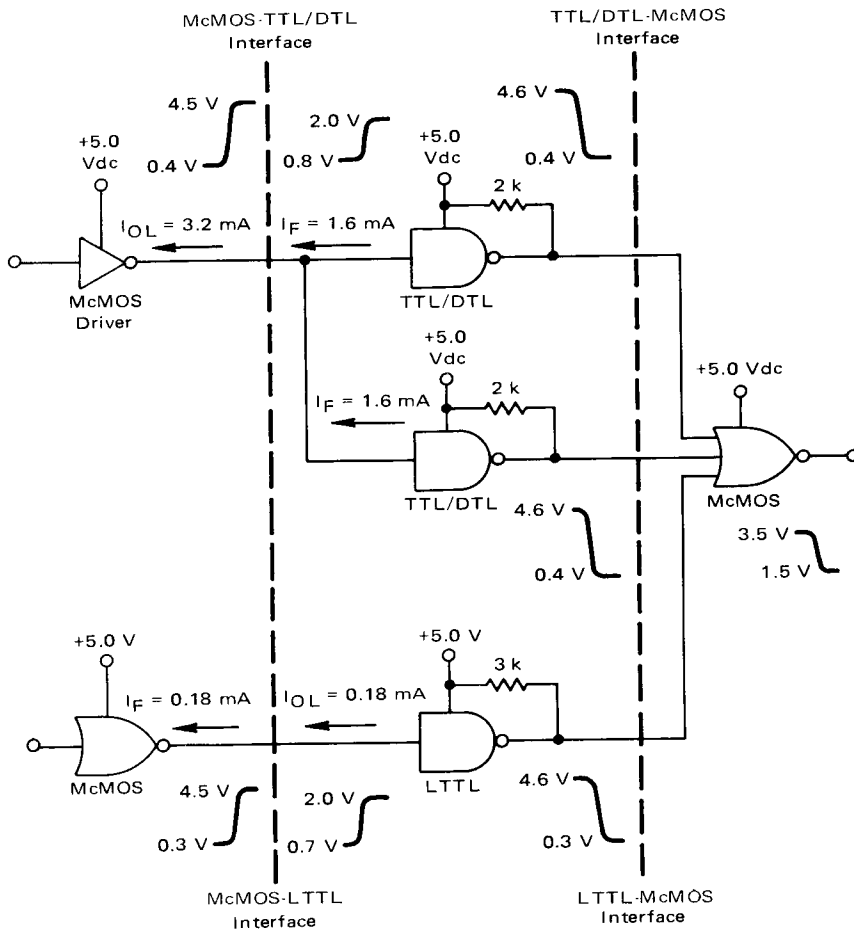


FIGURE 2-20 – McMos/BIPOLAR SYSTEMS INTERFACE

input to a logical "0" level. The major area of concern is the logic "1" state. The V_{OH} level of TTL/DTL devices is generally specified at 2.4 volts while sourcing $400 \mu\text{A}$. This is an absolute worst case bipolar specification and since McMos inputs only require about 10 picoamperes drive current, the typical V_{OH} level of a bipolar active pull-up output driving McMos would be equal to approximately two P-N junction voltage drops below V_{CC} , or typically 3.6 volts. This level is greater than the required 3.5 volt input of McMos; however, there is very little noise margin. For this reason, it is recommended that a pull-up resistor be added to the circuit from the bipolar output to V_{CC} as shown in Figure 2-20. Resistor values of 2 k ohms for TTL/DTL (or 3 k ohms for LTTL) provide

satisfactory pull-up and very satisfactory input rise times to the McMos device. It should be noted that when utilizing a bipolar-to-McMos interface, the driver should not fan-out to bipolar circuits, only to other McMos devices. However, when using a McMos-to-bipolar interface, fan-out may include both bipolar and McMos devices. As can be seen in Figure 2-20, the noise margins at the collective interface either maintain or exceed the 0.4 volt dc margins of the bipolar logic families. In general, the noise margin at the interface between CMOS and other 5 volt logic systems is higher than that of the bipolar system alone. This situation exists because of the higher positive logic levels at the CMOS interface.

Five volt operation of McMos restricts the

maximum speed capability, and in many systems where speed is of importance McCMOS may be powered with a supply voltage of 15 volts. Figure 2-21 shows the techniques used to interface McCMOS devices operating at 15 volts with 5 volt bipolar devices. Here the "down" translation is easily achieved by using the McCMOS buffer translators specifically designed for this application.

The "up" translation can be performed by using one of two different methods. One method uses a high voltage, open collector TTL gate such as the MC7406 with a pull-up resistor to the 15 volt V_{DD} supply. The value of the pull-up resistor must be considered in relation to system speed. Since a McCMOS input loading is typically characterized by 5 picofarads, the rise time at the 7406-McCMOS interface will be determined by the resistor and the number of McCMOS loads. High speed and fast rise times may dictate the use of low resistance values and a significant increase in power dissipation.

The second method of "up" translation has a reasonable power dissipation while still maintaining an acceptable rise time. The device used in this method is a MHTL, MC666 level translator. This device is an active pull-up, bipolar High Threshold Logic (HTL) component which has inputs for translating from RTL, DTL or TTL operating levels to 15 volt logic levels.

McCMOS device series since typical power dissipation ratings have less than 2 microwatts per gate.

The McCMOS series can also be used to expand the MHTL generic designs by providing the complex functions (expansion) for MHTL. The only prerequisite is that proper interface of the two logic types be implemented as shown in Figure 2-22. Both logic types operate from a single +15 Vdc supply. The output logic levels of the typical McCMOS gate are made equal to input of the MHTL circuit (i.e., $V_{OH} = 13.5$ volts and $V_{OL} = 1.5$ volts for the high and low levels, respectively). Since the MHTL gate responds only to signals that exceed the input logic levels ($V_{IH} = 8.5$ volts and $V_{IL} = 6.5$ volts), the full MHTL 5.0 volt noise margin is maintained at the interface. The number of MHTL circuits that can be driven by a typical McCMOS gate (fan-out) is determined from the output characteristics. Each MHTL input represents a load current (I_{OL}) of approximately 1.2 milliamperes. The McCMOS output voltage (V_{OL}) will remain below 1.5 volts when the device sinks 1.2 milliamperes; this corresponds to a fan-out of the one MHTL load.

Interfacing the MHTL gate to drive McCMOS circuits (fan-in) is a somewhat different design consideration. Because the input current to a driven McCMOS gate is negligibly small, an MHTL circuit can drive a very large number of McCMOS inputs

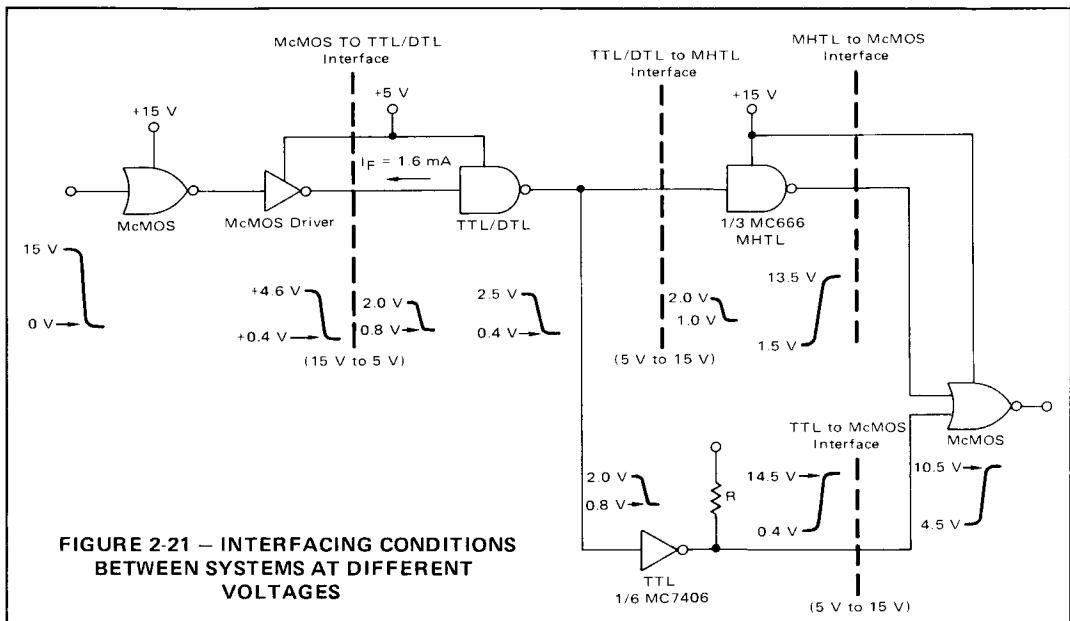


FIGURE 2-21 — INTERFACING CONDITIONS BETWEEN SYSTEMS AT DIFFERENT VOLTAGES

INTERFACING McCMOS WITH MHTL

McCMOS functions can be used to expand the versatility of standard, industrial high threshold logic systems where a large signal swing and high noise immunity are important. MHTL is generically limited in per device functions by an inherently high power dissipation which is typically 25 mW per logic gate. The condition does not exist in the

(50 or more). However, since the input to a McCMOS gate is essentially capacitive (about 5 pF per input) and the internal load resistor of passive MHTL circuits is 15 k ohms, this capacitive loading effect could add an RC time constant of 75 nanoseconds per fan-out. Therefore, the number of McCMOS circuits that can be connected is limited primarily by the system dynamic response.

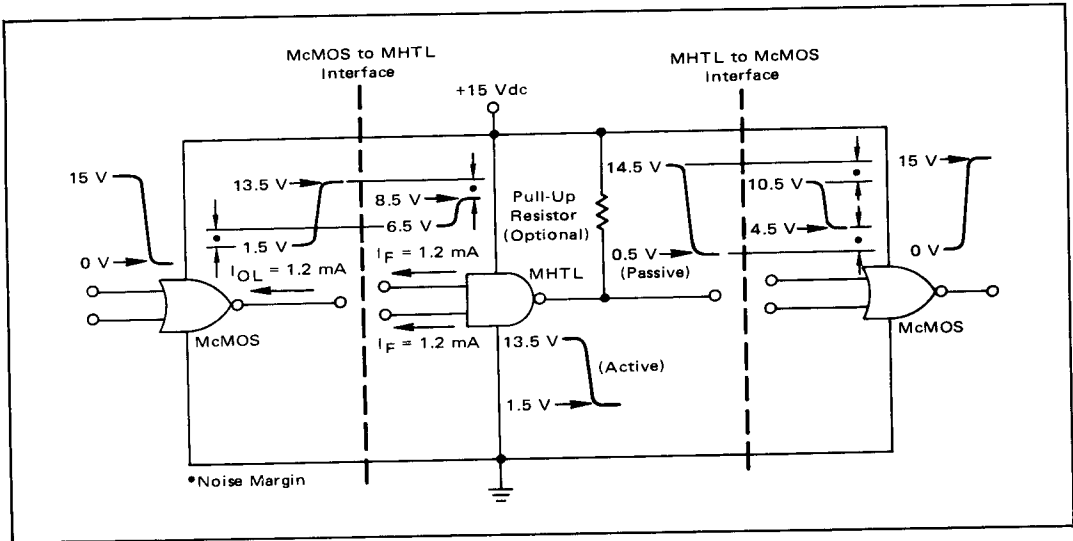


FIGURE 2-22 – INTERFACING CONDITIONS BETWEEN McMOS AND MHTL CIRCUITS

For this reason, a pull-up resistor is recommended at the output of the MHTL circuit to improve speed. Values range from 1.5 k ohms to 5 k ohms, depending on the desired switching speed, allowable power dissipation, and the desired noise immunity factor. A low value pull-up resistor will raise the V_{OL} output level and increase power drain, but it can also increase switching speed by as much as 85 percent. The best compromise appears to be the use of a passive output HTL circuit with an inherently low saturation voltage and a moderate value (2 k to 3 k ohms) external pull-up resistor. An active pull-up MHTL circuit will also drive a large number of McMOS gates with

adequate speed, but both the high-noise and low-noise margins will be reduced.

Because McMOS and MHTL can interface directly with each other, they serve to complement one another in system designs where noise immunity or high voltage operation is important. MHTL provides pulse shapers, high current drivers and other interface elements while McMOS will provide complex functions which cannot be economically built with MHTL. Figure 2-23 shows the organization of a system design using McMOS and MHTL with some recommended MHTL interface component types.

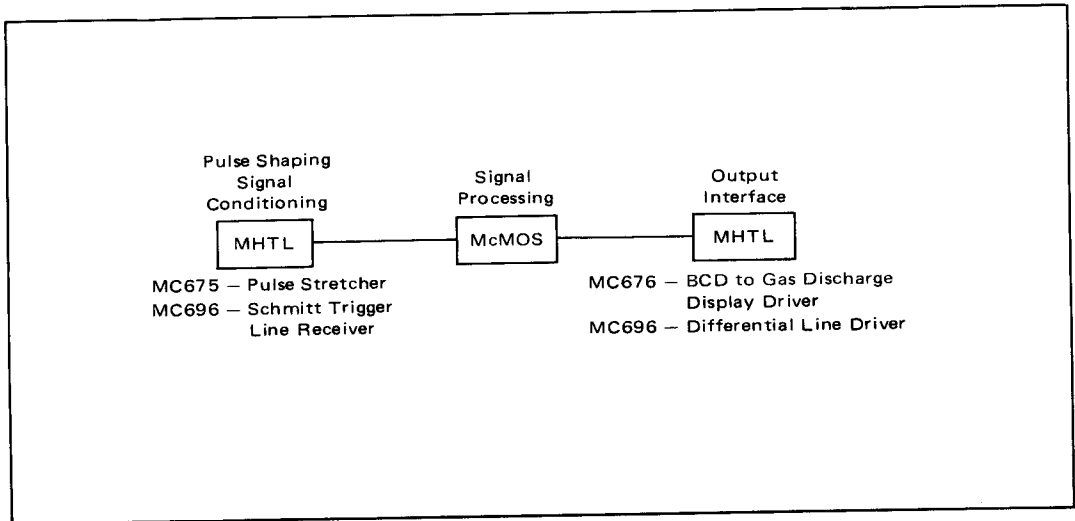


FIGURE 2-23 – USING A COMBINATION OF McMOS AND MHTL

INTERFACING McMOS WITH MECL

In systems with McMOS and MECL negative voltage power supplies are commonly used. The McMOS series can operate at -5.2 V (the MECL supply) or at higher voltages. The advantage of using the higher voltages is that McMOS can operate at higher speeds.

The interface from a McMOS output to MECL levels is shown in Figure 2-24(a). Note that the McMOS operates between ground and $-V_{SS}$; V_{SS} can be any voltage within the range of the McMOS device (18 V maximum). The McMOS output directly drives the MECL 10,000 input. If V_{SS} is greater than -5.2 V, a diode clamp is required to prevent the MECL input from dropping more than a diode voltage drop below the -5.2 V (V_{EE}).

The MECL 10,000 input requires a current of $265 \mu\text{A}$ (maximum worst case) and has input threshold voltages of $V_{IHA} = -1.105$ V and $V_{ILA} =$

pulls the McMOS input to within 800 or 900 mV of ground. If $V_{SS} = -5.2$ V, the transistor switches from -0.9 V to -5.2 V. The high level noise margin will be approximately 0.66 V and the low level noise margin will be approximately 1.56 V. With a greater V_{SS} , noise margins will be correspondingly larger.

INTERFACING McMOS WITH OTHER MOS TECHNOLOGIES

Other than CMOS, the most common Metal Oxide Semiconductor technology available today are the P-channel high threshold (PMOS) components. Becoming more common are low threshold devices (silicon gate and $\langle 100 \rangle$ devices). The main difference between the two MOS types is the supply voltage necessary for operation. Typical high threshold supplies are $V_{SS} = 0$ V,

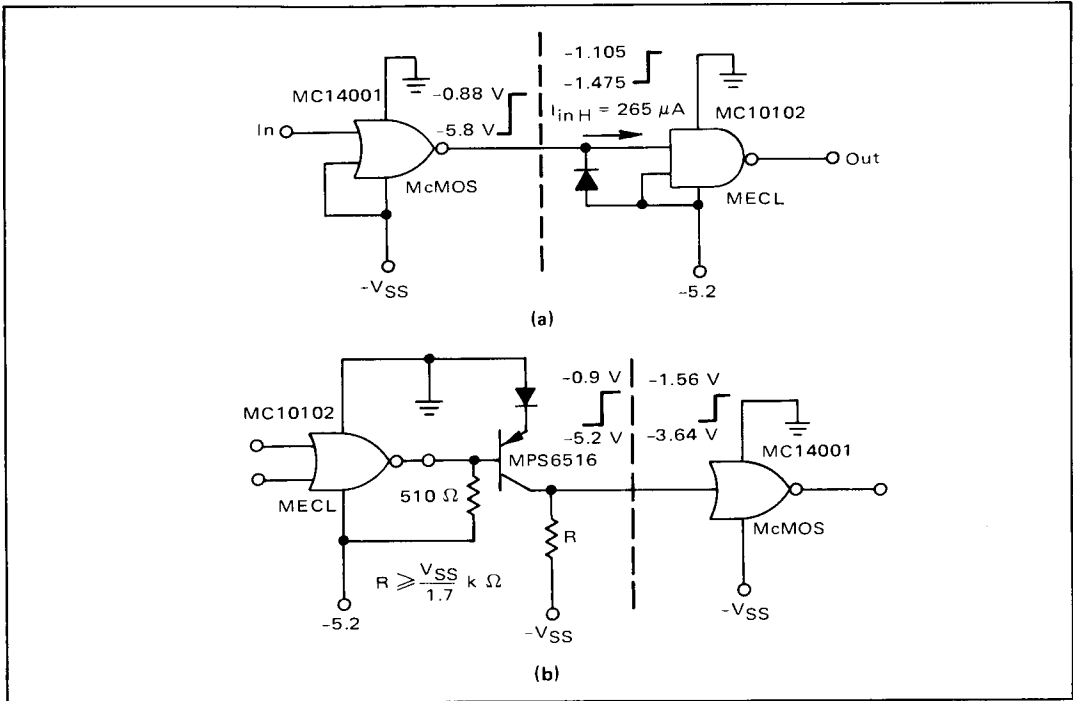


FIGURE 2-24—McMOS—MECL AND MECL—McMOS INTERFACE SYSTEMS

-1.475 V (25°C). The noise margin is therefore in excess of 225 mV in the high state and 4.3 V in the low state.

Level translation is required to drive a McMOS input with a MECL device. The 800 mV voltage output swing of MECL is not sufficient to drive a McMOS input. The MECL 10,000 output is used to switch a transistor to drive the McMOS input (Figure 2-24(b)). The high MECL output level (~ 900 mV typical) is not sufficient to forward bias the transistor ($V_{BE} + V_{\text{diode}}$). The low output level of -1.7 V typical turns on the transistor and

$V_{DD} = -13$ V and $V_{GG} = -27$ V. Corresponding low threshold supplies are $V_{SS} = +5$ V, $V_{DD} = -5$ V and $V_{GG} = -12$ V. Another important difference is that high threshold devices generally use negative logic convention ("0" is the most positive level and "1" the most negative) while low threshold devices use positive logic convention. The typical output swing for both high and low threshold devices goes from V_{SS} to V_{DD} when driving the high input impedance McMOS logic function.

The wide supply range of McMOS and the high

input impedance of MOS and McMOS devices make interfacing a simple matter. Figure 2-25(a) shows a McMOS to high threshold PMOS interface while Figure 2-25(b) shows a McMOS to low threshold PMOS interface.

Another technology commonly used in many logic systems today are N-channel MOS (NMOS) devices. NMOS like PMOS, is available in both the metal gate and silicon gate processes. Very large memories, such as the MCM6570 8192-bit Read Only Memory, are manufactured using the NMOS process.

Although NMOS devices operate using conven-

be interfaced, regular CMOS gates will not drive the device and a CMOS driver/buffer is required. For this reason, the system designer must be thoroughly familiar with the specific NMOS device to be used (the logic level and current requirements) and select the proper selection of a compatible interfacing CMOS device.

INTERFACING CMOS WITH BIPOLAR LSI

Yet another series of logic integrated circuits available to the system designer are the bipolar large scale integration (LSI) devices. These circuits consist of large gate arrays which are mask-program-

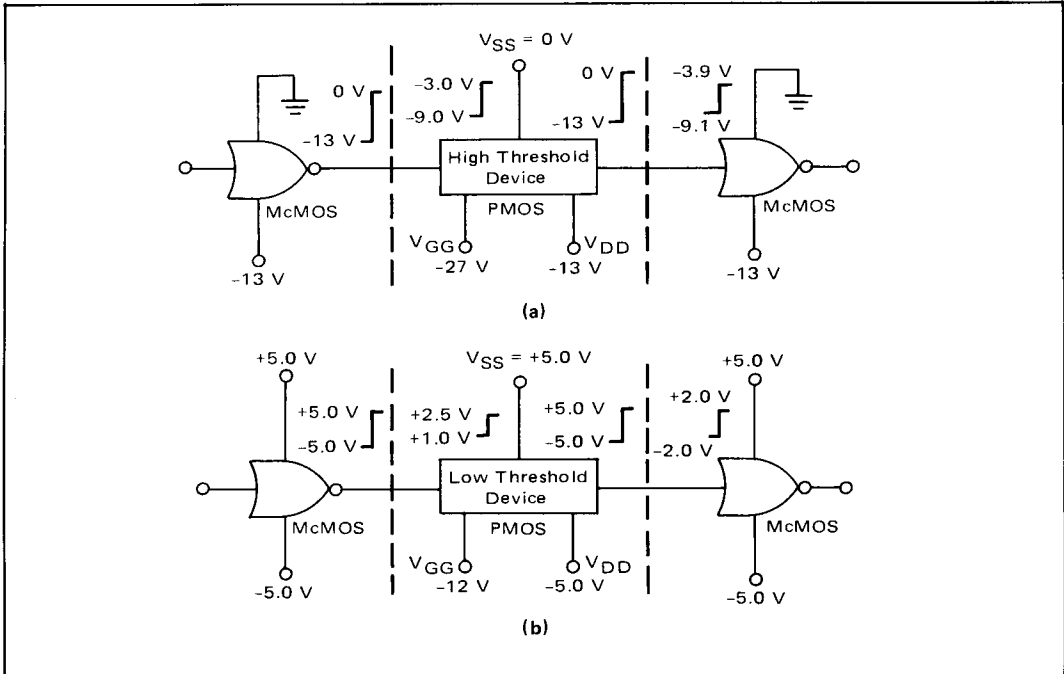


FIGURE 2-25 – McMOS – PMOS AND PMOS – McMOS INTERFACE SYSTEMS

tional positive logic with positive power supplies in the 5 to 15 volt range (with the exception of a small negative back-bias supply) and use positive logic convention, special consideration must be used when interfacing with CMOS devices. The positive voltage power supplies necessary for NMOS are also compatible with CMOS devices; further, the CMOS devices are normally operated with V_{DD} at a positive voltage and V_{SS} at ground potential. An area of concern to the designer exists when a system requires interfacing NMOS and CMOS. The concern applies primarily to the NMOS device inputs. Several NMOS devices are manufactured with TTL type inputs which use internal pull-up devices. This manufacturing technique requires the designer to use TTL levels and associated sinking requirements to drive the NMOS devices. If this is the case with the NMOS device to

able to provide specialized complex system functions. One technology used in these gate arrays is termed STRL and illustrated in Figure 2-26. This STRL gate basically consists of a Schottky transistor and four resistors. Interfacing between CMOS and

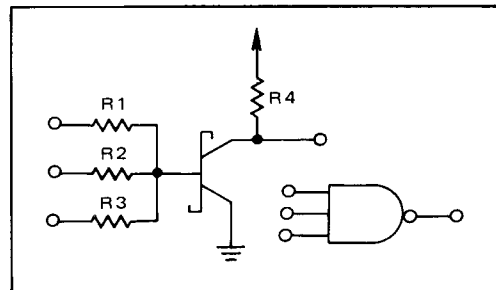


FIGURE 2-26 – A BASIC STRL GATE

STRL gate arrays is shown in Figure 2-27. As shown, the entire system operates with a +5.0 volt supply. While the STRL input levels are exactly like TTL, the STRL family exhibits a much lower sinking requirement I_{inl} . These characteristics make any CMOS device compatible in driving STRL logic with resulting noise margins at the high and low state of 2.5 and 0.5 volts, respectively. STRL also has a TTL fan-out of 1 with TTL-type output logic specifications. However, under worst case consideration with a resistor tolerance of +30% (R_4 in Figure 2-26) and sourcing the total leakage of the Schottky transistor, the V_{OH} level will be approximately 4.2 volts rather than the specified 2.4 volts at an I_{OH} of 300 μA . The worst case noise margins for the STRL to CMOS interface are therefore 0.7 and 1.0 volts, high and low state, respectively.

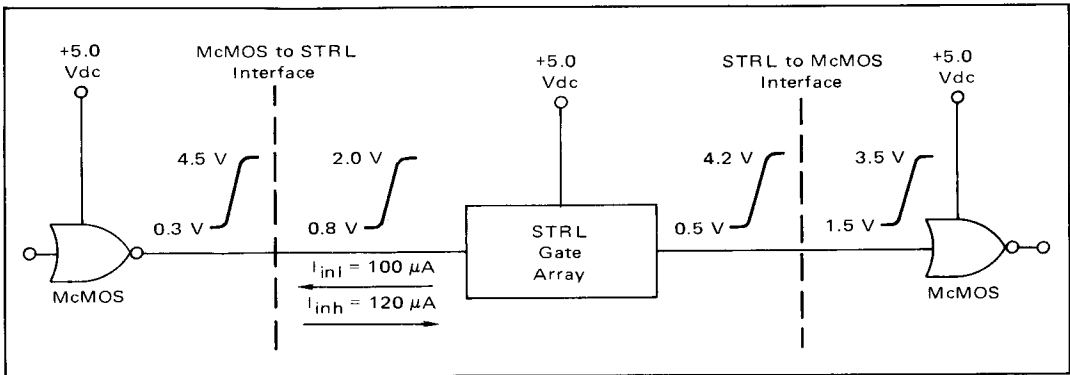


FIGURE 2-27 — McMOS — STRL LSI SYSTEMS INTERFACE

STRL gate arrays are also available with open collector outputs. When using these devices it is necessary to use an external pull-up resistor and a suitable value would be approximately 3 to 4 k ohms. Another of the LSI gate arrays uses low power Schottky TTL logic cells. The input and output characteristics of these cells are similar to standard low power TTL and can also be interfaced with CMOS logic in the same manner as LTTTL.

INTERFACING McMOS WITH OTHER SEMICONDUCTOR DEVICES

One misconception that many circuit designers have with CMOS is that this technology cannot source or sink any appreciable or usable amount of current when interfacing with other than CMOS devices. This is not always true, as this chapter previously described in the section entitled Output Loading Considerations. The sinking and sourcing capability of a CMOS device, as found on data sheets, are measured at specific output voltages and illustrate fixed points in the non-saturated region of the CMOS output drain characteristic curves. In fact, CMOS devices can drive high current loads if large drain to source voltages (V_{DS}) are allowed across the N- or P-channel devices.

However, there are specified current limitations which are 10 milliamperes into or out of any package pin on standard CMOS devices or as high as ± 45 milliamperes per output on certain buffer/driver configurations. Data sheets must be consulted so as not to exceed the device current or dissipation limits.

Figure 2-28 shows an example of a standard CMOS device driving an NPN transistor. The value of the base resistor R_B is dependent upon the value of the CMOS V_{DD} operating voltage. If the supply V_{DD} is 5 volts, the R_B resistor is not required since the source current limit is typically 2.0 milliamperes. This figure is determined from the saturated area of the P-channel drain characteristics. A V_{DD} voltage of 10 volts is marginal for operation when $R_B = 0$ ohms, since the sat-

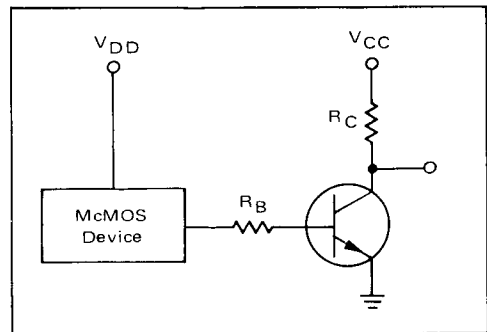


FIGURE 2-28 — McMOS TO DISCRETE INTERFACE

urated P-channel current in this case (approximately 9 milliamperes), is very close to the allowed 10 mA device limit. Therefore, in this application a value of 500 ohms is recommended for resistor R_B . At 15 volts, it is necessary to use a value of approximately 1 k ohm for resistor R_B to limit the current to 10 mA, since the typical saturated current level in this case is approximately 18 mA. The same reasoning applies to applications where driving PNP transistors; the CMOS device N- and P-channel

drain characteristic curves should be consulted to select the proper values of current limiting resistors. Obviously, the choice of pull-up resistor R_C and the transistor are based upon the required drive current level and the h_{FE} versus I_C characteristics of the selected transistor.

The technique used in Figure 2-28 can also be used as a driver interface from McMOS to several TTL or LTTTL gates or devices. The fan-out of such a circuit is dependent upon the current gain of the transistor and the properly selected pull-up resistor R_C .

One specific application of a McMOS device gate driving a high current load is shown in Figure 2-29. In this application, a load current of 4 amperes is required. The selected interface, a 2N6055 power Darlington, requires a base current of 16 milliamperes for a V_{CE} saturation of 2 volts; to supply this current, the McMOS MC14049 hex-inverter, buffer/driver is used. From the P-channel drain characteristics curve, the saturated source current is found to be approximately 32 milliamperes for a V_{DD} of 10 volts. In driving the Darlington with a 20 mA, the McMOS characteristics exhibited a drain to source voltage of -4.0 volts. Therefore, the base resistor R_B can be calculated by the equation:

$$R_B = \frac{V_{DD} - V_{DS} - V_{BE(sat)} - V_{diode}}{I_B}$$

or approximately 100 ohms.

The addition of the diode and 1 k ohm bias resistor in the Darlington emitter circuit ensure a slight reverse bias on the Darlington when the McMOS driver is in the low state and thus prevents thermal runaway. For pulsed operation, the MR751 six

ampere diode is used; for continuous operation, it is recommended that a stud mounted MR1120 be used for power dissipation reasons.

One advantage of using a McMOS device to drive a circuit as shown in Figure 2-29 is that the driver circuit dissipates very little power when in the idle or OFF state. The push-pull type output of McMOS dissipates power only when driving the load device unlike a TTL open collector driver which must shunt all the drive current when the load device is OFF.

By using techniques similar to Figure 2-29, McMOS can be used to directly drive LEDs, optocouplers or other discrete devices. Examples of interfacing to high power drivers, such as SCRs and triacs, are described in Motorola application note AN-712 entitled "Interface Techniques Between Industrial Logic and Power Devices".

INTERFACING SUMMARY

With a wide range of power supply operating voltages and simplified input/output characteristics, McMOS logic elements may be successfully interfaced with any other logic device technology available today. Table 2-2 shows the noise margins, logic levels and fan-out for various logic family interfaces.

McMOS elements can also be used as current drivers for interfacing with a variety of discrete semiconductor devices. The sourcing and sinking capability for driving discretes may be extrapolated from the McMOS device output drain characteristic's curves. By using these curves and observing the device maximum current and dissipation limits, a reliable McMOS to discrete power interface may be achieved.

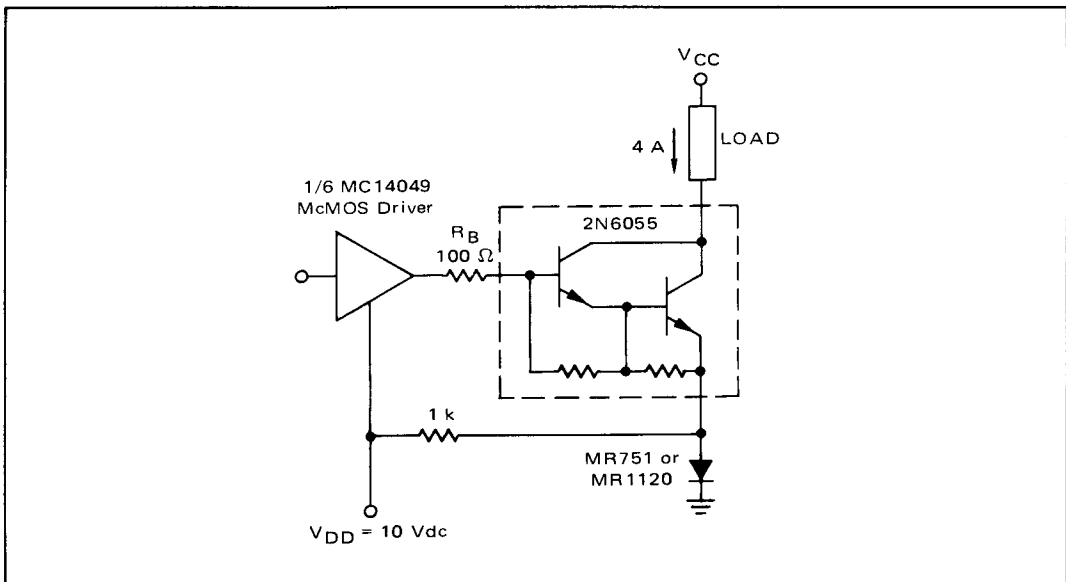


FIGURE 2-29 — McMOS TO BIPOLAR
4 AMPERE DRIVER

TABLE 2-2 – CMOS GENERAL INTERFACE PARAMETERS

INTERFACE	INTERFACE [†] NOISE MARGIN		INTERFACE [‡] LOGIC LEVELS		INTERFACE MAXIMUM FAN-OUT	REMARKS
	"1"	"0"	"1"	"0"		
McMOS-McMOS	1.5 V	1.5 V	3.5 V	1.5 V	> 50	5-volt system.
	3.0 V	3.0 V	7.0 V	3.0 V	> 50	10-volt system.
	4.5 V	4.5 V	10.5 V	4.5 V	> 50	15-volt system.
McMOS-MHTL	5.0 V	5.0 V	8.5 V	6.5 V	1	
MHTL-McMOS	3.0 V	3.0 V	10.5 V	4.5 V	> 50	Active pull-up MHTL
	4.0 V	4.0 V			> 50	Passive pull-up MHTL with 2 k to 5 k ohm pull-up resistor
McMOS-LTTL	2.5 V	0.4 V	2.0 V	0.7 V	1	Two-input CMOS NOR gates driven in parallel will drive two LTTL loads; Four-input CMOS NOR gates driven in parallel will drive four LTTL loads.
LTTL-McMOS	1.1 V	1.2 V	3.5 V	1.5 V	See Remarks	3-k ohm pull-up resistor. Fan-out determined by dynamic requirements.
McMOS-TTL/DTL	2.5 V	0.4 V	2.0 V	0.8 V	2	Buffers only.
TTL/DTL-McMOS	1.1 V	1.1 V	3.5 V	1.5 V	See Remarks	2-k pull-up resistor for TTL or open-collector DTL. Fan-out determined by dynamic requirements.
McMOS-MOS	3.0 V	4.0 V	-3.0 V	-9.0 V	> 50	High Threshold PMOS ($V_{SS}-V_{DD}$) = 13 V
	2.5 V	6.0 V	2.5 V	+1.0 V	> 50	Low Threshold PMOS ($V_{SS}-V_{DD}$) = 10 V
MOS-McMOS	3.9 V	3.9 V	3.5 V	1.5 V	> 50	High Threshold ($V_{SS}-V_{DD}$) = 13 V
	3.0 V	3.0 V	2.0 V	-2.0 V	> 50	Low Threshold ($V_{SS}-V_{DD}$) = 10 V
McMOS-MECL	0.225 V	4.325 V	-1.105 V	-1.425 V	2	V_{DD} = Ground V_{SS} = -5.2 V
MECL-McMOS	0.66 V*	1.56 V*	-1.56 V	-3.64 V	> 50	V_{DD} = Ground V_{SS} = -5.2 V *Typical
McMOS-STRL	2.5 V	0.5 V	2.0 V	0.8 V	2	
STRL-McMOS	0.7 V	1.0 V	3.5 V	1.5 V	See Remarks	Fan-out determined by dynamic requirements.

[†]Interface Noise Margin

- For "1" column-difference between output high level of one device and input high level of next,
- For "0" column-difference between output low level of one device and input low level of next.

[‡]Interface Logic Level: worst case threshold level going from one device to the input of another.

OPERATING SPEED

The operating speed of a logic system is based upon signal propagation delays and the output rise and fall times. In the CMOS logic family these parameters vary as a function of the output load capacitance, the operating voltage, and the device temperature.

CAPACITIVE LOAD EFFECTS

The CMOS family is designed to have equal propagation delays from the low-to-high and high-to-low states (t_{PLH} , t_{PHL} , respectively). In addition, the CMOS devices also have equal rise and fall times (t_r , t_f) with a 15 pF load. These four parameters all vary as a function of the load capacitance and in most data sheets are characterized by a form of the formula:

$$t = K_0 C_L + K_1$$

The formula constants are different for t_r , t_f and the propagation delay $t_{PLH} = t_{PHL}$. Both K_0 and K_1 are device dependent and functions of logic complexity, internal capacitance, carrier mobility, etc. The important coefficient in determining dynamic performance for a given capacitive load is K_0 and is given in nanoseconds per picofarad.

Special consideration must be given to capacitive loading effects, especially to t_r and t_f when driving edge-triggered devices, and also to the propagation delays when operating totally synchronous systems.

(See the previously described section entitled Input Considerations). The effects of the load capacitance on the above mentioned ac parameters are shown in Figures 2-30 and 2-31.

VOLTAGE EFFECTS

The constants, K_0 and K_1 , in the formula above are given in the data sheets for power supply voltages of 5, 10 and 15 volts. The relationships of the delay and transition times with operating voltage are also shown in the typical family characteristics in Figures 2-30 and 2-31. In general, the delay and transition times decrease approximately as the inverse of the operating voltage. Similarly, the maximum operating frequency increases proportionally to the supply voltage.

TEMPERATURE VARIATIONS

As the temperature of a CMOS chip increases, the mobility of the N- and P-channel devices decrease; as a result, longer times to charge or discharge the external load capacitance are required. A previous section entitled Thermal Considerations described and illustrated (Figure 2-12) a normalized plot of the change in delay and transition times as a function of ambient temperatures. To generalize this plot, the increase in delay or transition times is approximately $+0.25\%/^{\circ}\text{C}$ for temperatures increasing above 25°C .

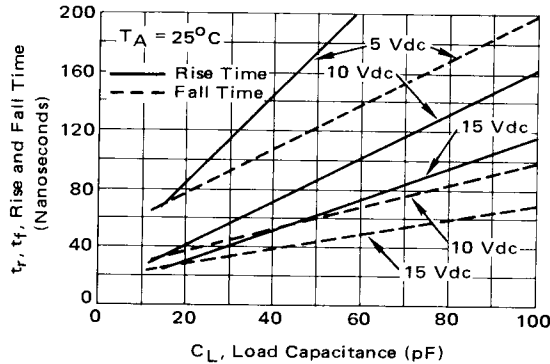


FIGURE 2-30 – TYPICAL RISE AND FALL TIME versus LOAD CAPACITANCE

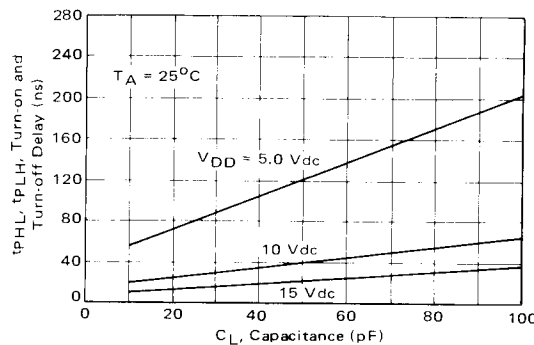


FIGURE 2-31 – TYPICAL PROPAGATION DELAY TIMES versus LOAD CAPACITANCE

THREE-STATE LOGIC AND ANALOG SWITCHING CONSIDERATIONS

In many system applications, the wire-ORing technique of the passive pull-up outputs has been used in bussing type applications. This technique greatly reduces system wiring and package count by the sharing of common input/output lines. When TTL logic was introduced, active pull-up devices were used in the output circuitry rather than the passive elements as in DTL logic. The active pull-up outputs prevented these devices from being used in wired-OR applications, and the only way to achieve the wired-OR was to use logic elements incorporating open collector type outputs with external pull-up resistors. To eliminate the problems of wire-ORing in TTL, the concept of three-state logic was introduced. This allowed the system designer to develop multiplexing schemes which select a single element to drive a common line while disabling all other drivers on that line. The concept also allowed more drivers to be attached to a common input/output bus line.

CMOS, like active pull-up TTL, cannot be wire-ORed since both the current sinking and sourcing devices in a CMOS output are MOS transistors. To illustrate, one may consider two CMOS gates with their outputs connected as shown in Figure 2-32. If the output of gate A is a logic "1" (P-channel transistor ON) and the output of gate B is a logic "0" (N-channel transistor ON), a current path exists from V_{DD} internally through gate A to the output, and also into the output of gate B, and finally to V_{SS} . If the impedances of the N- and P-channel transistors are comparable, the output level between gates A and B will be approximately 1/2 of $(V_{DD} - V_{SS})$.

If the power supply voltage is less than 10 volts, gates A and B will probably not be destroyed in this example. However, the power dissipation will increase and the output level will not be a usable logic state.

To eliminate the problems of wire-ORing, the three-state logic concept is provided in many CMOS logic functions because it can be very easily implemented, as will be described later.

WHAT IS THREE-STATE LOGIC?

The output of a standard logic element has two stable and defined states (a logic "1" or true state and a logic "0" or false state). Both of these states can be represented by a low impedance device coupled to one of the power supply rails. A three-state logic element simply provides an additional third output state. When in the third state (output disable or OFF), the output is effectively disconnected from the logic driving devices by a high impedance network at its output.

In the active logic "1" or "0" mode, three-state outputs have the same electrical equivalent as non three-state outputs. As shown in Figure 2-33(a), the output network for CMOS consists of capacitors connected to both power supplies. In parallel, diode structures serve to restrict logic levels to within the operating voltage supply range.

When switched to the three-state (high impedance) mode, as shown in Figure 2-33(b), the source-sink drive resistances increase to the 150-200 megohm range, effectively by an open circuit. For data sheet specifications, this open circuit resistance is defined by a three-state leakage current measured with respect to either voltage supply bus.

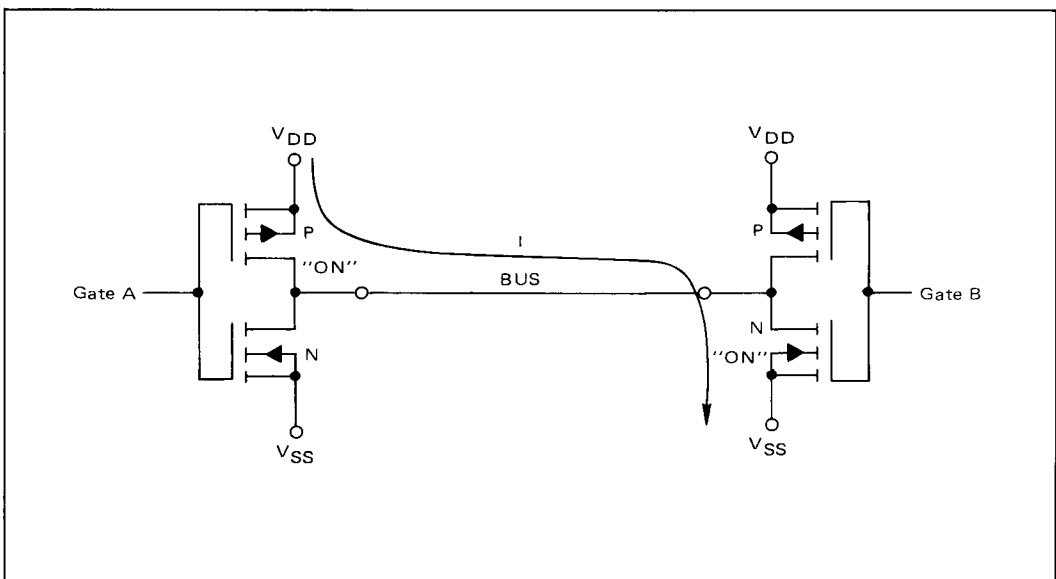


FIGURE 2-32 – CMOS GATES WITH OUTPUTS CONNECTED

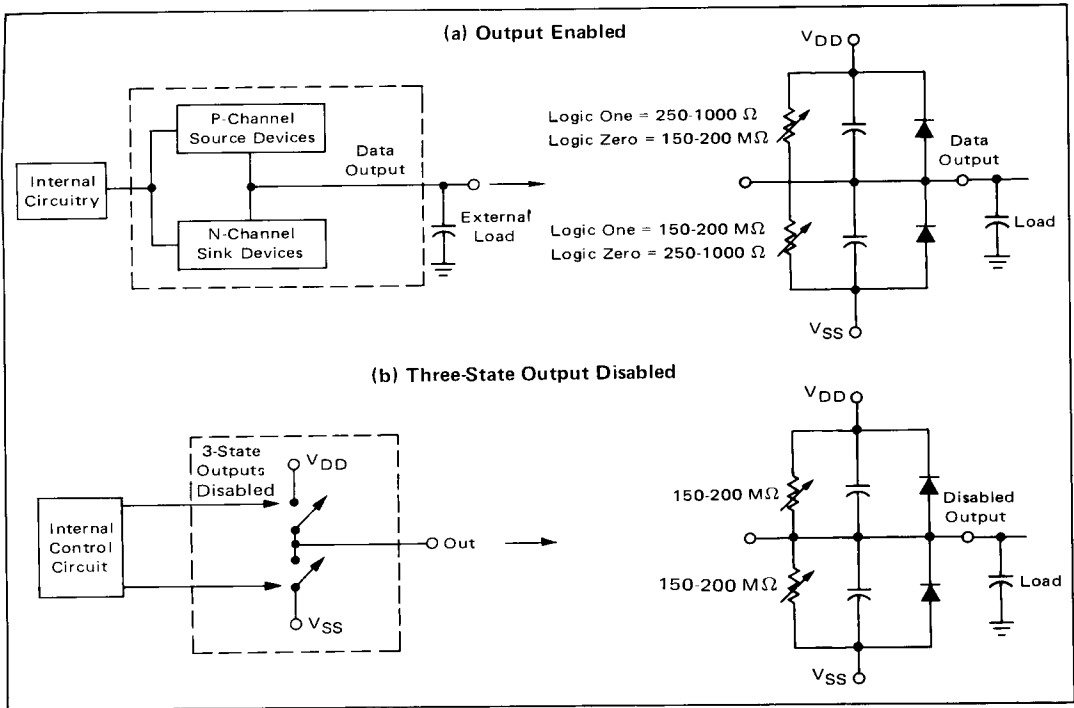


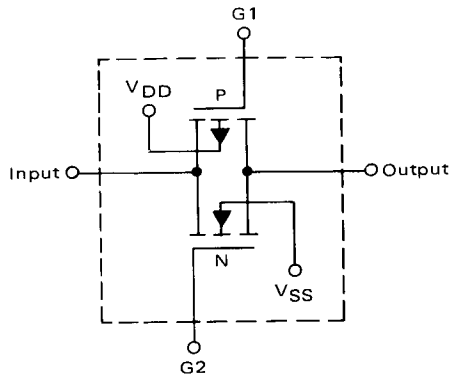
FIGURE 2-33 – CMOS OUTPUT EQUIVALENTS

THREE-STATE LOGIC IMPLEMENTATION

The prime objective in a three-state device design is to disconnect the output terminal from the active logic driving sources. There are two basic methods to achieve this objective: either a transmission gate or a disabling function may be implemented. The first method uses a transmission gate in series with the output signal line. The transmission gate is an important building block for the construction of CMOS integrated circuits; its characteristics which are easily provided in CMOS would be difficult to duplicate in any other IC technology available today. The circuit of the basic McMOS transmission gate is shown in Figure 2-34. When

the transmission gate is enabled, a low resistance exists between the input and the output which allows current flow through the gate in either direction. The voltage on the input line must always be positive with respect to the substrate (V_{SS}) of the N-channel device, and negative with respect to the substrate (V_{DD}) of the P-channel device. The gate is enabled when the gate (G1) of the P-channel device is at V_{SS} and the gate (G2) of the N-channel device is at V_{DD} . When G2 is at V_{SS} and G1 is at V_{DD} , the transmission gate is disabled and a resistance greater than 10^9 ohms exists between input and output.

FIGURE 2-34 – BASIC McMOS TRANSMISSION GATE



The diagram of a three-state element using a transmission gate to provide the output disable is shown in Figure 2-35(a). Figure 2-35(b) shows the logic symbol and definition of a transmission gate. The second method of design of a three-state output disables or disconnects both the sourcing and sinking driving devices from the V_{DD} and V_{SS} power supply rails. The circuit for this method is shown in Figure 2-35(c). In this figure segment, the center P- and N-channel MOSFETs are connected as a standard CMOS inverter. In series with the inverter are an additional P-channel device to V_{DD}

and an N-channel device to V_{SS} . By using a second inverter to provide the two phase signals from an input disable signal, both P- and N-channel series MOSFET devices can be simultaneously enabled or disabled. When the series devices are enabled (ON), the output functions as a normal CMOS inverter. When they are disabled (OFF), the three-state logic inverter is a "don't care" state since the output is disabled. The logic symbol and truth table of the described three-state circuit is shown in Figure 2-35(d).

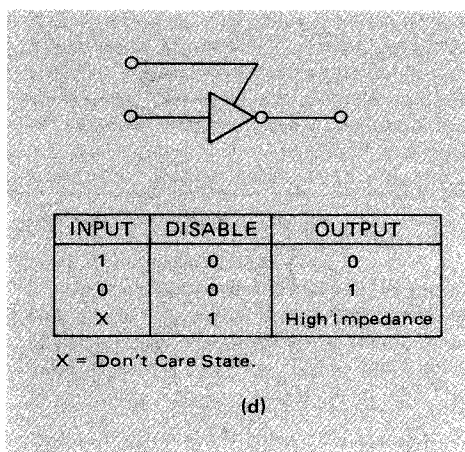
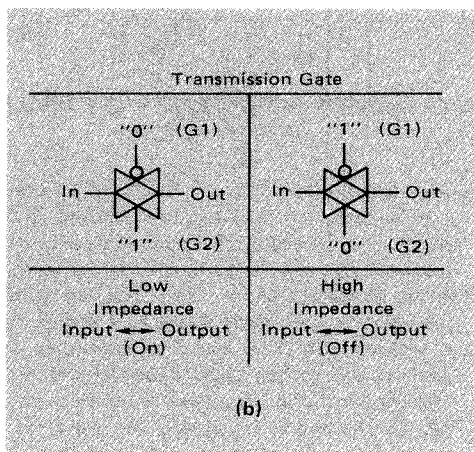
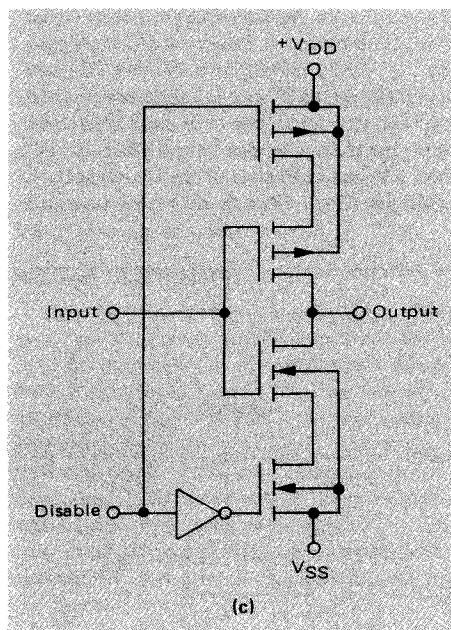
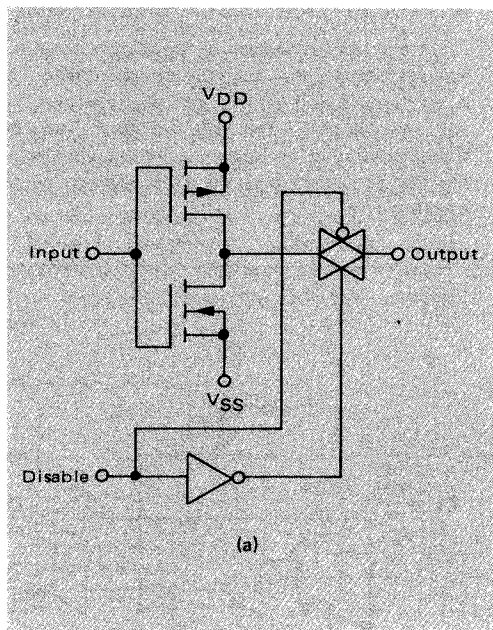


FIGURE 2-35 – BASIC THREE-STATE OUTPUTS

INTERNAL LOGIC TRANSMISSION GATES

The transmission gate is a valuable tool used for accomplishing many CMOS technology MSI and LSI designs. An illustration of using the basic transmission gate is provided in the CMOS MC14013, Type-D flip-flop as shown in Figure 2-36. The flip-flop works on the Master/Slave principle and consists of four transmission gates (TG). Four NOR gates, two inverters, and a clock buffer/inverter, comprise the configuration. When the clock is a logic "0", transmission gates TG2 and TG3 are OFF and 1 and 4 are ON. In this condition, the Master is logically disconnected from the Slave. With TG4 ON, gates G3 and G4 are cross-coupled and latched in a stable state. Assuming that the Set and Reset inputs are low, the logic states of gates G1 and G2 are determined by the logic signal applied to the Data input. When the clock changes to a logic "1", TG2 and TG3 turn ON and TG1 and TG4 turn OFF. Gates G1 and G2 are cross-coupled through TG2 and latch into the state they held at the time the clock changed from a "0" to a "1". With TG3 ON, the logic state of the Master section (output of gate G1) is fed through an inverter to

the Q output and G3 through an inverter and finally to the \bar{Q} output. When the clock returns to a "0", TG3 turns OFF, and TG4 turns ON. This disconnects the Slave from the Master and latches the Slave into the state existing in the Master when the clock changed from a "1" to a "0". Thus, data is entered into the Master on the positive edge of the clock pulse. When the clock is logical high, the output of the Master is transmitted directly through the Slave to Q and \bar{Q} . When the clock transfers to a logical low state, the Master logical state is stored by the Slave which then provides the outputs. Transmission gates and flip-flops are commonly used in system counter and shift register designs.

ANALOG APPLICATION CONSIDERATIONS

In addition to generating three-state outputs or internal digital signal steering, the transmission gate is very useful as a gate for analog signal switching and multiplexing. Two of the most important characteristics of an analog switching element are the ON resistance and the OFF leakage current specifications.

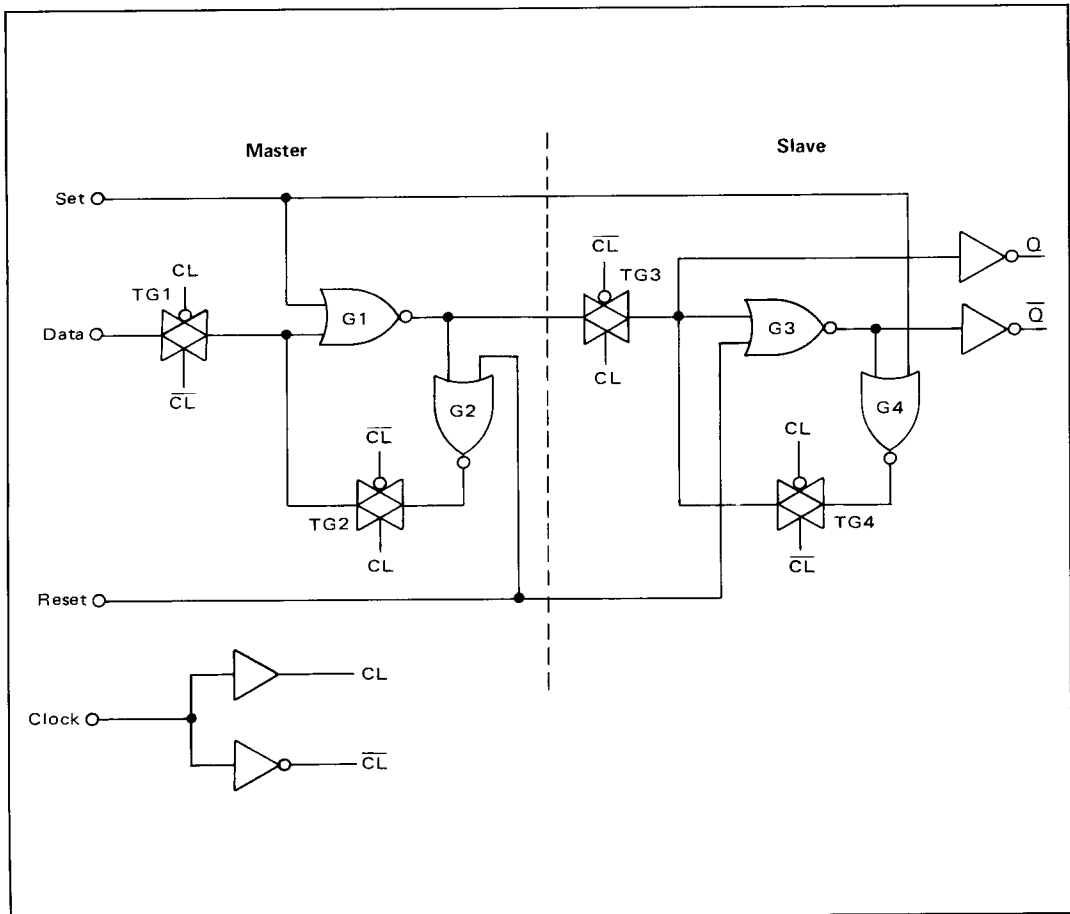


FIGURE 2-36 – CMOS TYPE D FLIP-FLOP

ON RESISTANCE

The resistance between the input and output of a basic transmission gate in the ON condition is dependent upon the voltage applied at the input, the potential difference between the two substrates ($V_{DD} - V_{SS}$), and the load on the output. R_{ON} is defined as the input-to-output resistance with a 10 k ohm load resistor connected from the output to ground. Figure 2-37 illustrates an interesting peaking effect which occurs in the R_{ON} versus V_{in} curves of the basic transmission gate in Figure 2-34. When V_{in} is at or near V_{DD} , the P-channel device provides the low resistance. The N-channel device is OFF since the potential difference between G2 and the drain or source of the N-channel device is less than the threshold voltage. When V_{in} is at or near V_{SS} , the N-channel device is conducting and the P-channel device is OFF. At voltages between the two extremes, both devices are partially ON and the value of R_{ON} is due to the parallel resistance of the P-channel and N-channel devices. The different slope of the curve on either side of the peak is due to the greater sensitivity of the N-channel resistance to the substrate degeneration (or substrate bias). Thus, the rate of increase in R_{ON} with respect to V_{in} is greater for input voltages between V_{SS} and the "peaking voltage" than for input voltages greater than the "peaking voltage".

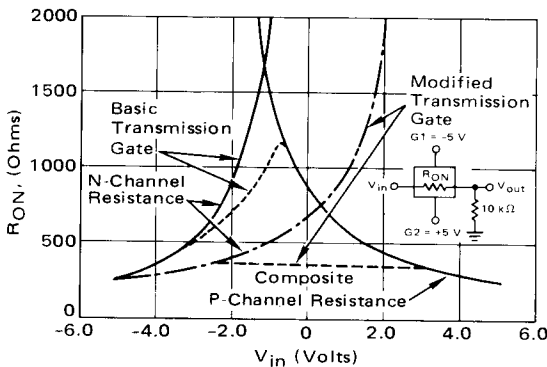


FIGURE 2-37 — CMOS TRANSMISSION GATES
 R_{ON} versus V_{in}

Figure 2-38 shows a modification to the basic CMOS transmission gate with the addition of a third device to control the substrate bias of the N-channel device. The effect of this third device is to delay the turn OFF of the N-channel device which results in a much flatter R_{ON} versus V_{in} curve, as shown in Figure 2-37. This concept is used in the MC14016 Quad Analog Switch. Even with the addition of devices to control the substrate bias, R_{ON} will still vary as a function of the input signal amplitude. This variation will always be the greatest at the lower power supply ($V_{DD} - V_{SS}$) voltages and decrease as the power supply voltage is increased to the maximum value. With a 10 volt

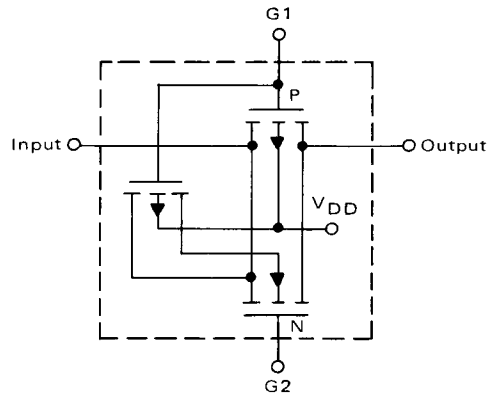


FIGURE 2-38 — MODIFIED CMOS TRANSMISSION GATE

supply, the change in R_{ON} will typically vary less than $\pm 15\%$ from the nominal resistance — over the specified range of input voltages ($V_{SS} < V_{in} < V_{DD}$). The change in R_{ON} between any two gates in an analog gate package will typically be less than 5% of the nominal value.

SIGNAL DISTORTION

The variation of the gate resistance versus input level causes analog signal distortion. Distortion may be minimized if the analog gate is operated from a split power supply. To illustrate, if $V_{DD} = +5$ volts and $V_{SS} = -5$ volts, the input analog signal will swing from $-V_{sig}$ to $+V_{sig}$, where V_{sig} is the peak amplitude of the analog signal with reference to ground. Note that the V_{sig} component must be restricted to the range of $V_{SS} < V_{sig} < V_{DD}$. If this condition is not held, destruction will occur because of the internal forward biasing of P-N junctions.

In the case of the MC14016 Quad Analog Switch, the signal distortion is measured using $V_{DD} = +5$, $V_{SS} = -5$, $R_{load} = 10$ k ohms and a V_{in} swing of ± 5 volts ($1.77 V_{RMS}$) at 1 kHz. The specified total harmonic distortion is typically less than 0.16%. Obviously, the distortion will increase as the power supply voltage is lowered. Distortion will also increase as the load resistance is decreased from 10 k ohms because of the voltage division relationship. The equation, $\frac{R_L}{R_L + R_{ON} + \Delta R_{ON}}$, illustrates this relationship.

Insertion loss is also a measure of the magnitude of the R_{ON} value. This parameter is measured using an input frequency of 1 MHz and various loads R_L . The insertion loss in dB = $20 \log_{10} (V_{out} / V_{in})$. At low values of R_L (i.e., < 10 k ohms), $V_{out} \approx \frac{R_L V_{in}}{R_L + R_{ON}}$. This equation is valid only for low load impedances and relatively low signal frequencies. With a frequency of 1 MHz or higher and load impedances greater than 100 k

ohms, the insertion loss begins to be dominated by the output capacitance parallel to the load.

INPUT/OUTPUT LEAKAGE

In the OFF state, the transmission gate has a very high resistance (in the order of 10^9 ohms) and is specified in CMOS device data sheets by an input/output leakage current value. This parameter is measured by using a positive and negative power supply (V_{DD} and V_{SS} , respectively), disabling the transmission gate, applying a signal input forced to V_{DD} or V_{SS} (two measurements), and the output leakage current being measured with respect to ground. This is the reason for the plus and minus specification on the data sheets. The leakage currents at 25°C will be typically in the order of nanoamperes with several orders of magnitude difference between the typical and maximum values. The leakage currents components and the variation over temperature is the same as that previously discussed in the section entitled Thermal Considerations.

DEVICE CAPACITANCE

A simplified ac model of a transmission gate including the gate ON/OFF impedances and associated capacitances are shown in Figure 2-39. The definitions of the circuit elements are:

- $C_{CS1,2}$ – control to switch capacitance
- C_{in} – control input capacitance
- C_{IOS} – switch feedthrough capacitance
- C_{IS} – switch input capacitance
- C_{OS} – switch output capacitance
- $C_{SS1,2}$ – switch to switch capacitance
- R_L – leakage impedance
- R_{OFF} – gate OFF resistance
- R_{ON} – gate ON resistance

coupling capacitance (control-to-switch) C_{CS} . This test is performed by loading the input and output of the analog switch and driving the control line with a signal having a specific rise/fall time and pulse width. The "noise" pulse amplitude coupled from the control logic to the switch is measured and specified in millivolts.

The effect of the coupling capacitance C_{SS} between switches is characterized by the crosstalk specification between any two switches within a single package. This crosstalk is measured by loading both analog switches with one statically turned ON and the other OFF. The ON switch is driven with a 1 MHz sine wave and the output of the OFF switch is measured in dB with reference to the drive. A typical value for the MC14016 Quad Analog Switch is -80 dB and represents a coupling capacitance of less than 0.02 picofarads.

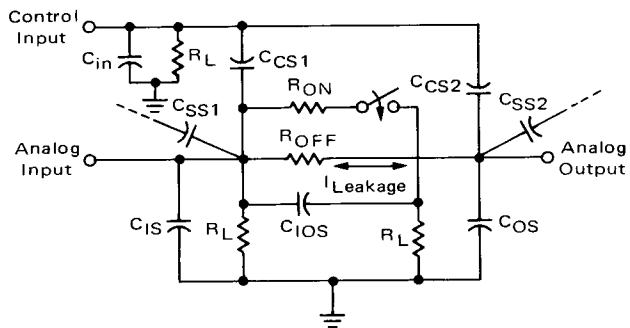
The feedthrough capacitance C_{IOS} is the capacitance (input-to-output) of the analog switch parallel to the ON/OFF resistances. The effect of this capacitance is signal feedthrough from input-to-output when the switch is OFF. One method of measuring this effect is to drive an OFF switch with a sine wave oscillator and increase the frequency until the feedthrough reaches a predetermined value (such as -50 dB) and record the driving frequency.

The capacitance C_{IOS} is typically 0.2 pF, and with a load impedance of 1 k ohms, the frequency for the -50 dB level will be greater than 1 MHz. This -50 dB frequency will decrease as the load impedance is increased because of the following mathematical relationship.

$$-50 \text{ dB} = 20 \log_{10} (V_{out} \div V_{in}),$$

$$\text{where } V_{out} = V_{in} \cdot \frac{Z_L}{Z_L + Z_F},$$

FIGURE 2-39 – AC MODEL OF SIMPLE TRANSMISSION GATE



Of all the internal capacitances of an analog switch, only four are specifically given in the data sheet: both inputs, the output, and the switch feedthrough capacitances. However, the elements not listed specifically are either the causes or effects for other electrical parameters contained in the data sheet.

The control-to-output crosstalk, measured in millivolts, is a measure of the amount of internal

and Z_L = load impedance,

and Z_F = feedthrough impedance.

With a load of one megohm, the frequency for the -50 dB level will be only a few kilohertz.

The output capacitance C_{OS} is the limiting factor of an analog switch bandwidth. The bandwidth is the frequency at which the output signal is 3 dB below the output level at the midband

frequency and is measured with a sine wave input and various loads. The 3 dB point is the frequency at which the output capacitance is determined from the following equation:

$$X_C = \frac{.707}{1-.707} \frac{R_{ON}R_L}{R_{ON} + R_L}$$

The output capacitance is typically 5 pF and with a 1 k ohm load, the bandwidth is greater than 50 MHz. As the load R_L increases in impedance the bandwidth decreases. With loads greater than 100 k ohms, the value of $\frac{R_L}{R_{ON} + R_L}$ approaches 1 in the relationship of X_C to R_{ON} .

The switch input capacitance C_{IS} is typically 5 pF as was the output capacitance C_{OS} . The analog switches are bidirectional and their characteristics in both the input or output ports are identical. If the switch is driven from a low impedance source, the input capacitance may be neglected. However, with a high impedance source or with the cascading or treeing of switches in multiplexing, the capacitance must be considered since the signal frequencies may be attenuated and/or shifted in phase.

As analog switch outputs are paralleled to form multiplexers, the output capacitance increases proportionally to the number of outputs that are common. When systems require a large number of high frequency signal lines to be multiplexed, it is recommended that multiplexing be accomplished in several levels (tree fashion) with a smaller number of switches on each branch. This method will somewhat increase the complexity of the digital control logic and add to the signal delay; however, the system design goals will be more easily achieved.

SWITCHING SPEED

Besides the signal speed which was previously discussed with switch bandwidth, the switching speed must also be considered. The control input frequency is limited by the time required to turn the switch ON and OFF. The time required for the switch to change states will be typically less than 25 nanoseconds and will turn OFF faster than it turns ON. In relay terminology, a "break-before-make" action is necessary to prevent faults in multiplexing applications where several outputs are connected together.

In MSI or LSI parts designed for multiplexing, the delay from the control to the switch changing states will be longer than that previously mentioned. This delay time will be a function of the complexity of the required internal BCD or Binary decoding logic and must be considered when selecting a component to perform high frequency multiplexing. Obviously, as with CMOS speed in general, the maximum switching speeds are obtained at the highest $V_{DD} - V_{SS}$ power supply voltages.

DIGITAL APPLICATION CONSIDERATIONS

As previously described, there are several methods used to generate three-state outputs; however, regardless of the method, the same considerations in digital bussing apply. The major areas of concern to the designer are the number of devices that can be bussed and the frequency limitations.

DRIVING REQUIREMENTS

Calculations for a CMOS bus system generally focus on external bus current requirements since the dc fan-out due to device leakage current limitations is in the order of several hundred devices. Specifically, the number of devices (N) which may be connected to a bus line is calculated from the following equation:

$$N = \frac{I_{OD} - I_L}{I_L} + 1.$$

In the equation, the component I_{OD} is the active logic "1" or "0" output level of drive current available to supply the I_{TL} output leakage current of disabled or three-state devices connected to the line. The component I_L is the external load current required to drive the bus line. Component N must be calculated for both the high and low bus line logic states.

In a total CMOS system, dc fan-out considerations will allow approximately 94 devices (N) to be connected to the bus with a 5 V power supply and the worse case parameters of $T = 125^\circ\text{C}$, $I_{OD} \text{ min} = -0.28 \text{ mA}$, $I_L = 100 \text{ nA}$ and $I_{TL} = 3.0 \mu\text{A}$. With such large values, fan-out is normally determined from switching performance requirements such as load capacitance and the required operating speed.

OUTPUT AND LOAD CAPACITANCE

When a three-state logic element is disabled, the output is a very high impedance and has an associated capacitance characteristic. This capacitance can be measured with a suitable bridge, or by observing a time constant on an oscilloscope when the output is disabled and a known value external load resistor is used. Care must be exercised when measuring the output capacitance, and all test fixture and instrumentation capacitances must not be overlooked.

The three-state output capacitance will typically fall in the range of 10 to 15 picofarads. This capacitance acts as a load to the bus line driving device and has a definite effect on the rise, fall and propagation times of the driver. Therefore, the three-state output capacitance must be considered in determining the number of devices which can be bused for a given data frequency.

BUS LINE RISE AND FALL TIMES

As was previously described in the section entitled Operating Speed, the rise and fall time is equal to: $t = K_0 C_L + K_1$, where K_0 and K_1 are constants

dependent upon the CMOS device. All the capacitances of the three-state outputs (10 to 15 pF each), all inputs (5 pF each), and the bus wiring must be summed together to determine the rise and fall times of a bus-oriented system. For standard devices, at a supply voltage of 10 volts, the effect of the loading capacitance is typically 1.0 to 2.5 nanoseconds per picofarad increase in rise time and 0.5 to 1.5 nanoseconds per picofarad increase in fall time. In applications having a high bus capacitance, three-state bus drivers such as the MC14502 should be used. When using high bus capacitance drivers, the time increase is typically 0.6 nanoseconds per picofarad in rise time and 0.2 nanoseconds per picofarad in fall time. Propagation delays also increase as a function of the load capacitance C_L . This rate of increase is approximately half the rate increase in the rise and fall times.

MULTIPLEXING SPEED

The factors that limit the multiplexing speed of a bus system are the times required to switch a device into and out of the three-state "high impedance" mode. These propagation delay times are referred to as $t''0''H$, $t_H''0''$, $t''1''H$ and $t_H''1''$. For the definition and test procedure used for determining these parameters refer to Chapter 5

entitled Family Data in this book.

The capacitive load effect on the delay times follows the same relationship ($t = K_0 C_L + K_1$) previously described regarding rise and fall times. The results of all the delays caused by bus line capacitance are shown in the timing diagram of Figure 2-40. In a three-state bus system, the data strobe of the receiver logic must be delayed a minimum time from the enable signal (which was applied to one of the bus drivers) to assure the accuracy of the data being received. This delay time is the summation of the maximum three-state delay time ($t_H''1''$ or $t_H''0''$), the maximum rise/fall time (t_r or t_f), the propagation delay of the bus lines, and the minimum setup time of the receiver logic.

A worst case three-state enable control pulse width would be the summation of the previously described minimum strobe delay, the minimum strobe pulse width, and the maximum receiver logic data hold time. The enable pulse width can actually be decreased from the worst case value because, as shown by the cross-hatched area of Figure 2-40, valid data is still present on the bus for the minimum delay time required of both the three-state output to go to the high impedance states and conversely from a high impedance state to a logic state.

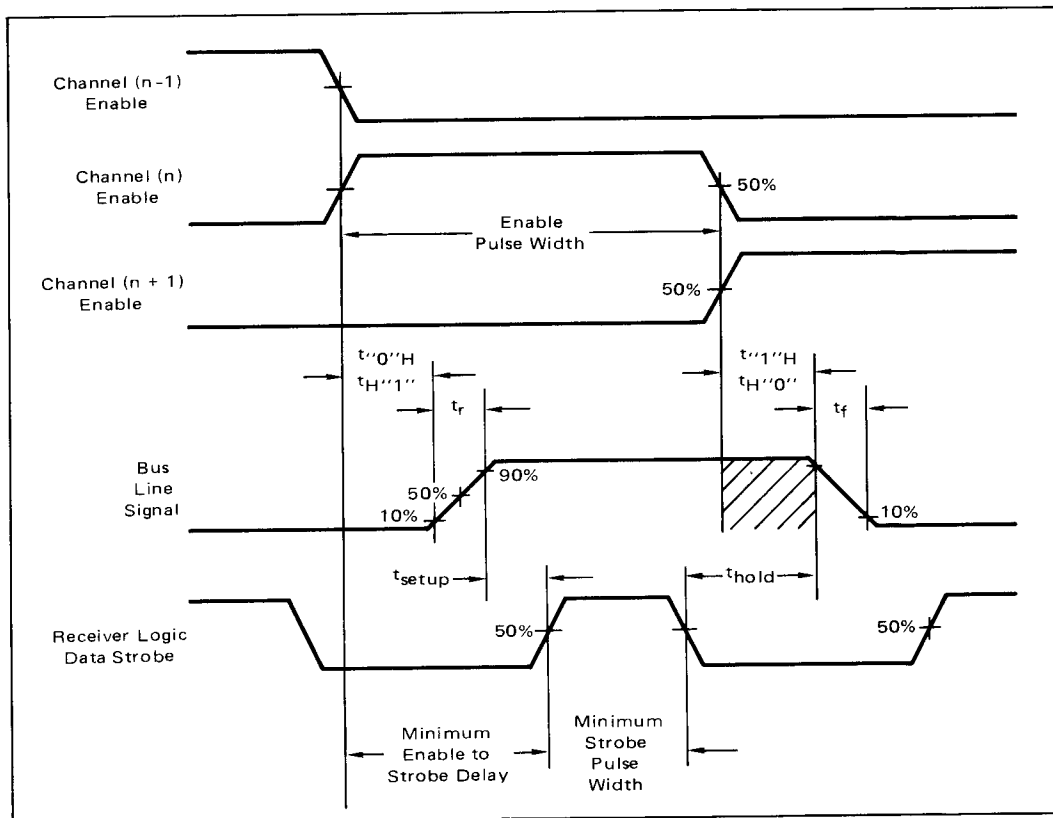


FIGURE 2-40 – THREE-STATE BUS TIMING DIAGRAM

BUS LINE PULL-UP/PULL-DOWN

The example used in the previous section illustrated that when the driver n was disabled, driver $n + 1$ was enabled to drive the bus line. Not all of the numerous three-state logic applications have a driver attached to the bus line at all times; these applications require special consideration.

If a bus system (at some period of time) has all drivers disabled, all outputs will be high impedance and the bus will be capacitive. The CMOS inputs of the bus receiver logic are also capacitive and will require very little drive current. In the totally disabled mode, high impedance bus lines make the receiver inputs very susceptible to both noise and oscillation, similar to open CMOS inputs. This situation can cause higher than normal receiver power dissipation and possible input destruction.

An obvious solution is to use pull-up/pull-down resistors on the bus lines. These resistors will have an associated rise time or fall time constant in relation to the total bus capacitance. This rise or fall time could present a problem; however, the use of resistors also limits the drive capability of the drivers when they are enabled.

An ideal solution is shown in Figure 2-41. In this application, the MC14016 Quad Analog Switch is used to dynamically pull-up or pull-down (depending on desired logic state) the bus lines when all of the driving devices are disabled. The

low ON resistance of the analog switch produces faster rise (and fall) times than the resistor technique since the resistor minimum value is limited by the driver capability. When any one of the drivers is enabled, the analog switch is disabled, thus minimizing the power dissipation consistently present with passive pull-up or pull-down elements.

POWER DISSIPATION

Power dissipation in three-state bus systems is a function of the load capacitance, input transition times, frequency, and power supply voltage, similar to the relationship found with any standard CMOS device. Refer to the section entitled Power Supply Considerations for power dissipation information.

Shorted bus lines may sometimes occur in a system. With the exception of CMOS drivers, standard device outputs (when operating at 5 volts) will not cause serious device damage. At higher voltages, excessive currents (design limits are 10 mA per output pin) will be realized if the outputs are shorted to V_{DD} or V_{SS} . For this important reason, the system designer must exercise care when using bus systems with lines vulnerable to shorts. Such systems should be carefully staged prior to the initial power-up. One method would be to use a variable power supply and apply power slowly during the staging phase.

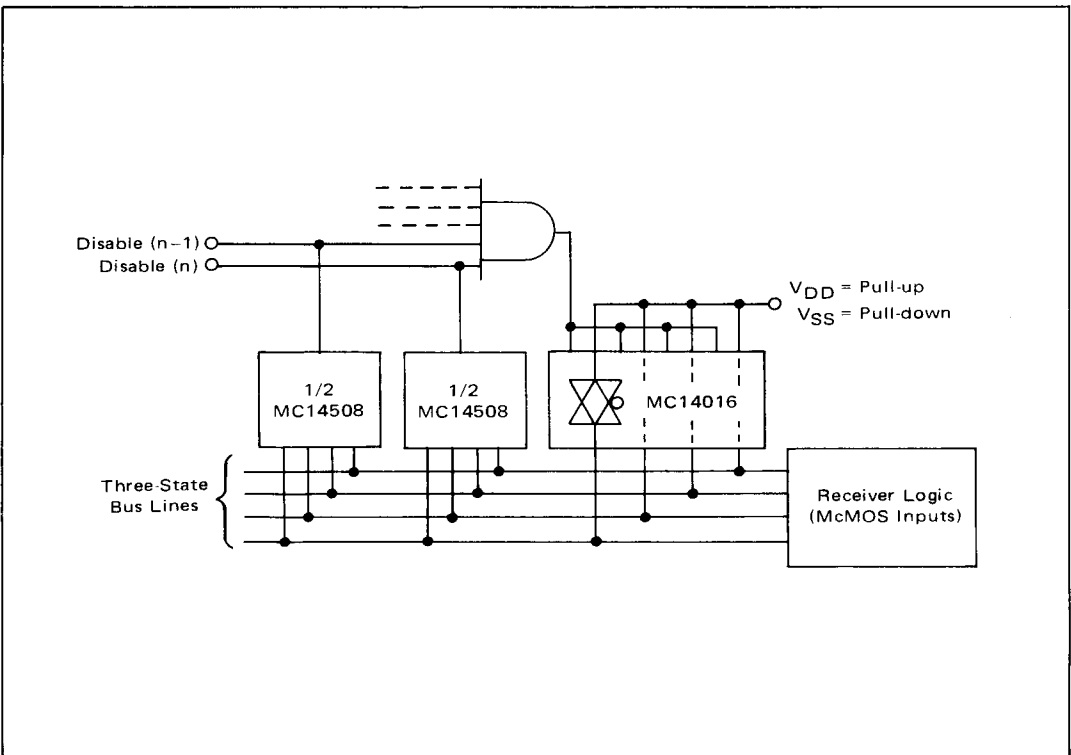


FIGURE 2-41 – THREE-STATE BUSING USING ACTIVE PULL-UP/PULL-DOWN