McMOS
INTEGRATED CIRCUITS
DATA BOOK

This book presents technical data for the broad line of McMOS integrated circuits. Complete specifications for the individual monolithic circuits are provided in the form of data sheets. Design information and family characteristic data provide the details necessary for successful use of McMOS circuits in system design. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

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McMOS

INTEGRATED CIRCUITS

Chapter 1
TECHNOLOGY OVERVIEW

INTRODUCTION

This McMOS Data Book has been prepared as a working tool for the system, logic, and layout designer. The organization and format of the book allows the designer to select the information based upon frequency of use. General introductory information and design data are grouped in the first sections of the book and provide a wealth of in-depth design and reference information. For day to day usage, the user may quickly bypass the Introductory, Design and Applications sections and proceed directly to the Index section, where an individual device in the family may be rapidly selected using either functional characteristics or alpha-numeric order.

Chapter 1 provides a technology overview of Complementary Metal Oxide Semiconductors, commonly referred to as CMOS. It serves as an introduction to CMOS for the new user or as a brief refresher for the seasoned designer. This section also introduces Motorola's McMOS family as well as providing a list of symbols and abbreviations related to this semiconductor technology.

Chapter 2 presents McMOS design information. Included in this section are the details necessary to successfully implement a system of logic which utilizes only CMOS or a mixture of CMOS with various bipolar logic types. Critical parameters such as power supply requirements, fan-out, noise immunity and interfacing with other logic forms are given special attention.

Chapter 3 is the application oriented portion of the Data Book. Specific applications of McMOS are presented as well as an applications index for device types. To enable the designer to gain a broader perspective of CMOS technology, a published article reference section is also provided.

Chapter 4 provides two functional indexes; one index presents the data in tabular form, and a second presents the devices in block diagram form. In addition, this chapter provides previews of devices soon to be announced.

For most efficient use of the detailed information presented in the data sheets, Chapter 5 provides McMOS family characteristics. This section provides ready references for key device parameters to be considered during the design, layout and fabrication of systems using the McMOS family of devices.

Package data is presented in Chapter 6 and includes appropriate mechanical and pictoral information. To assist the layout design effort, a portion of this section has been devoted to package outline diagrams which also include functional outputs.

Concluding the Data Book is Chapter 7 — a compilation of the McMOS data sheets. For ease of use, the sheets have been arranged in alpha-numeric order.

McMOS FUNDAMENTALS

Until recently, a system designer seeking a suitable system logic family had only two choices of technology; random system logic functions were bounded by either the saturated or non-saturated bipolar technologies. A choice of saturated logic offered high speed but non-saturated logic provided a range from high to low speed.

With the advent of CMOS, a new and economical choice was presented to the system designer. Not only does the McMOS family offer very low-power dissipation at medium speeds but additional benefits are obtained, such as freedom from precision power supplies, high noise immunity and large fan-outs. These advantages are offered in a wide variety of basic and complex logic functions allowing the designer complete system design freedom.

To better understand this new family and its use, the following paragraphs explore the basic MOS elements and their combination to form CMOS.

MOS DEVICES

The starting point for any investigation into MOS devices is the enhancement mode Field Effect Transistor. The first FET devices were fabricated using N-type substrate with two diffused regions of P-type material, the source and drain. A metalized layer separated from the substrate by a diffused layer of silicon dioxide formed the gate or control element. Figure 1-1 is a cross-section of the P-channel element and the schematic symbol.

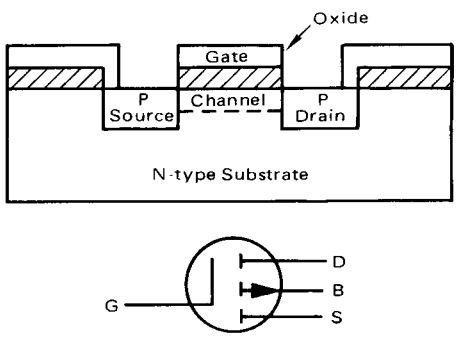

FIGURE 1-1 — P-CHANNEL TRANSISTOR (PMOS)

A voltage applied to the gate establishes a path for hole conduction (P-channel) between the source and drain. Similarly, using a P-substrate with N-doping for the source and drain results in an element utilizing electron conduction after gate turn-on (N-channel). Figure 1-2 is a cross-section of an N-channel element and the schematic symbol.

Either of these FET devices can be implemented into logic elements. Figure 1-3 is an inverter constructed using two N-channel devices.

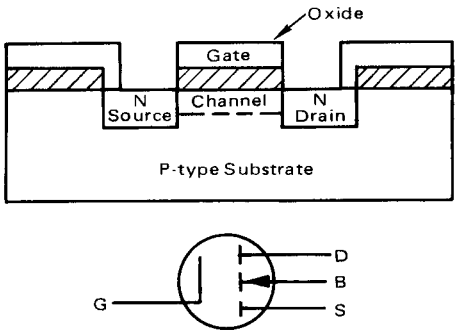

FIGURE 1-2 – N-CHANNEL TRANSISTOR (NMOS)

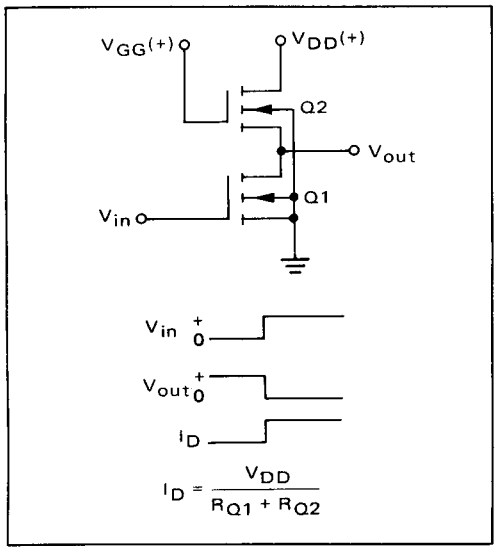

FIGURE 1-3 – TYPICAL N-CHANNEL INVERTER

In the circuit, Q2 serves as a fixed load resistor while transistor Q1 is switched. When Q1 is turned-on by the input signal, current is drawn from V_{DD} dissipating power in Q2. Circuits similar to these are currently in use in devices known as NMOS and PMOS.

CMOS DEVICES

A third configuration can also be implemented which makes use of both the N-channel and the P-channel devices. As shown in Figure 1-4, a complementary inverter may be formed by applying the input signal to the gates of two opposite polarity transistors.

In this circuit a low input signal means the N-channel transistor Q1 is OFF and the P-channel device is ON. The output is shorted to the positive supply, but virtually no load current is drawn if a similar high impedance MOS gate input is assumed as the load. When the input signal goes high, Q1 is turned-on and Q2 is turned-off. The output is pulled to ground, but no steady-state current is drawn. Power dissipation in the complementary MOS circuit (CMOS) is thus limited to the crossover conditions existing as the transition occurs from state to state. Proper device design for rapid turn-on and turn-off results in a dissipation factor as low as 2 nW per gate. The high noise immunity is also a direct result of the complementary configuration, since two separate thresholds must be crossed. This threshold is a direct function of power supply voltage, and is typically 45% of the supply voltage.

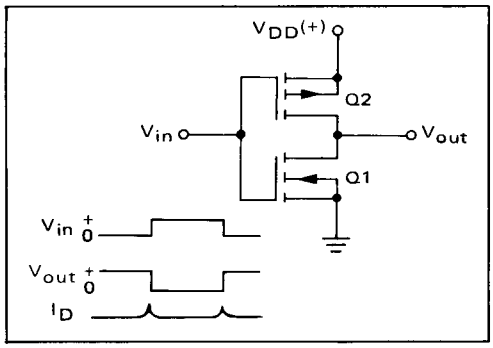

FIGURE 1-4 – TYPICAL COMPLEMENTARY INVERTER

The CMOS circuit results in a more complex fabrication process. Figure 1-5 shows a cross section of the CMOS integrated circuit. The P-channel device remains directly within the N-substrate. To form the N-channel device, however, a P-doped "tub" must be created into which the device is placed. In addition, channel stops must be placed between the "tub" and the P-drain to prevent parasitic channeling effects.

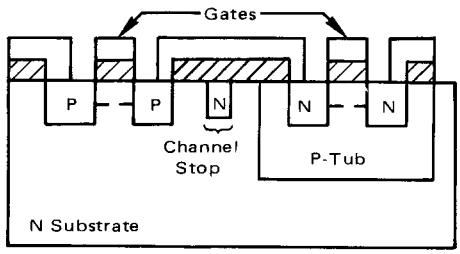

FIGURE 1-5 – TYPICAL CROSS SECTION OF COMPLEMENTARY MOS ELEMENTS (CMOS)

McMOS DEVICES

Using the basic CMOS technique, Motorola has developed the McMOS family of logic elements. A basic building block of logic elements has been designed and designated the MC14000 series. Examples of devices in this series are quad 2-input NOR gates and dual J-K flip-flops. Family expansion into more complex and specialized circuits has resulted in the MC14500 series. Included here are such devices as the dual 4-bit latch and a dual retriggerable/resettable monostable multivibrator. Memories constructed for the McMOS family are listed in the MCM14000 series.

SYMBOL GLOSSARY

BW	Bandwidth
C_{in}	Input Capacitance
C_L	Load Capacitance
f	Frequency (highest system rate)
I	Maximum Current Per Pin
I_{DD}	V_{DD} Supply Current
I_{in}	Input Current
I_{OH}	Output Source Current (high level state)
I_{OL}	Output Sink Current (low level state)
I_{out}	Output Current
I_{SS}	V_{SS} Supply Current
I_{TC}	Through-Current of McMOS Devices per Package
I_{TL}	Three-State Output Leakage Current
P_D	Power Dissipation
$P_{DD}max$	Maximum Power Dissipation per Package
P_L	Power Dissipation Due to Charge and Discharge of Internal and External Capacitance per Package.
$P_{OH}max$	Maximum Power Dissipation per Output Pin (high level output state)
$P_{OL}max$	Maximum Power Dissipation per Output Pin (low level output state)
P_Q	Quiescent Power Dissipation per Package
PRF	Pulse Rate Frequency (clock)
P_T	*Total (dynamic plus quiescent) power Dissipation per Package
P_{TC}	Power Dissipation Due to Switching Through-Current per Package
PW	Pulse Width
R_{ON}	On Resistance
T_A	Ambient Operating Temperature
T_{stg}	Storage Temperature
t_{acc}	Access Time
t_{cyc}	Cycle Time
t_f	Falling Transition Time (high to low)
t_{hold}	Hold Time
T_J	Junction Temperature
t_{PLH}	Propagation Delay Time (low to high output state)
t_{PHL}	Propagation Delay Time (high to low output state)
t_r	Rising Transition Time (low to high)
t_{rem}	Removal Time
t_{rel}	Release Time
t_{setup}	Setup Time
$t_{"0"H}$	Three-State Propagation Delay Time (low to high impedance output state)
$t_{H"0"}$	Three-State Propagation Delay Time (high impedance to low output state)
$t_{"1"H}$	Three-State Propagation Delay Time (high to high impedance output state)
$t_{H"1"}$	Three-State Propagation Delay Time (high impedance to high output state)
V_{DD}	Most Positive dc Supply Voltage
V_{in}	Input Voltage
V_{NH}	Noise Immunity Voltage Range (high level)
V_{NL}	Noise Immunity Voltage Range (low level)
V_{OH}	Output Voltage Level (high level output state)
V_{OL}	Output Voltage Level (low level output state)
V_{out}	Output Voltage Level (general)
V_S	Source Voltage
V_{SS}	Most Negative dc Supply Voltage
"0" or L	**Zero, Low, or False Logic State (most negative level)
"1" or H	**One, High, or True Logic State (most positive level)

*Some IC's may be on a per gate basis.
**Positive logic assumed.

ACRONYM GLOSSARY

ALU	Arithmetic Logic Unit
ASCII	American Standard Code for Information Interchange
BCD	Binary Coded Decimal
BCDIC	Binary Coded Decimal Information Code
CMOS	Complementary MOS
DIP	Dual In-Line Package
DTL	Diode-Transistor Logic
EBCDIC	Extended Binary Coded Decimal Interchange Code
ECL	Emitter-Coupled Logic
FET	Field-Effect Transistor
HTL	High-Threshold Logic
IC	Integrated Circuit
LED	Light Emitting Diode
LCD	Liquid Crystal Display
LTTL	Low Power TTL
LSI	Large-Scale Integration
MOS	Metal-Oxide-Semiconductor
MPU	Micro-Processing Unit
MSI	Medium-Scale Integration
PROM	Programmable ROM
RAM	Random Access Memory
ROM	Read Only Memory
RTL	Resistor-Transistor Logic
SCR	Silicon Controlled Rectifier
SSI	Small-Scale Integration
STRL	Schottky Transistor-Resistor Logic
TTL	Transistor-Transistor Logic