NT511740C5J

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Data Sheet

NT511740C5J

1. DESCRIPTION

The NT511740C5J is a 4,194,304-word x 4-bit dynamic RAM fabricated in NTC's CMOS silicon gate technology. The NT511740C5J achieves high integration , high-speed operation , and low-power consumption due to quadruple polysilicon double metal CMOS. The NT511740C5J is available in a 26/24-pin plastic SOJ.

2. FEATURES

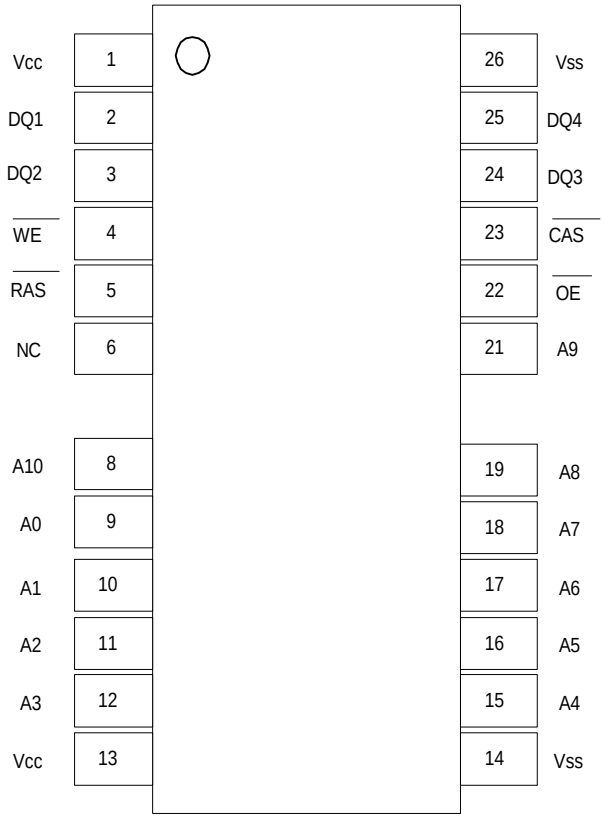
- 4,194,304-word x 4-bit configuration
- Single 5V power supply,±10% tolerance
- Input :TTL compatible , low input capacitance
- Output :TTL compatible , 3-state
- Refresh :2048 cycles/32 ms
- Fast page mode with EDO, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$-only refresh capability
- Multi-bit test mode capability
- Package options:

26/24-Pin 300 mil plastic SOJ (SOJ26/24-P300) (Product:NT511740C5J-XX)
XX indicates speed rank.

3. PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}	(Min.)	Operation(Max.)	Standby(Max.)
NT511740C5J-50	50ns	25ns	13ns	13ns	84ns	660mW	5.5 mW
NT511740C5J-60	60 ns	30 ns	15 ns	15 ns	104 ns	605mW	
NT511740C5J-70	70 ns	35 ns	20 ns	20 ns	124 ns	550 mW	

4. PIN CONFIGURATION (TOPVIEW)

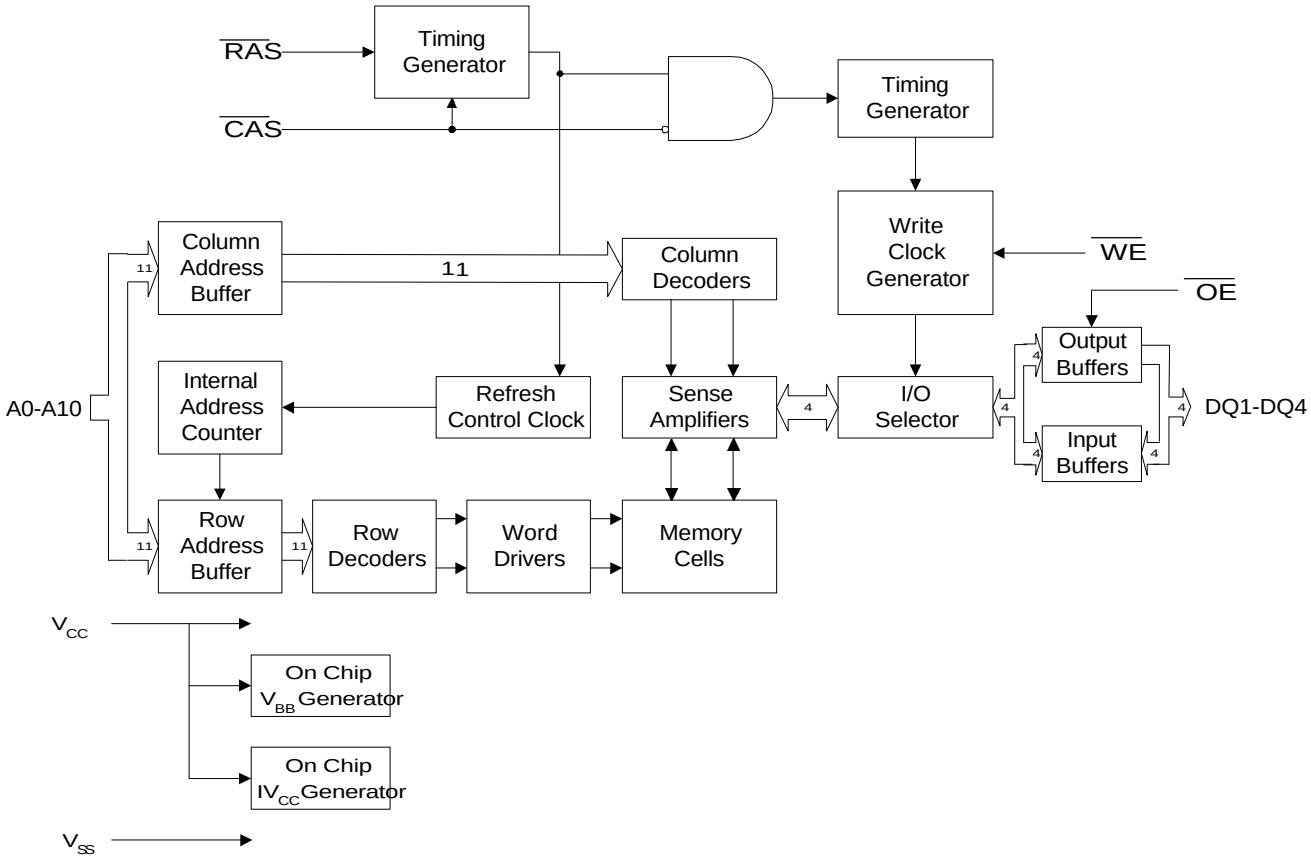


26/24-Pin Plastic SOJ

Pin Name	Function
A0-A10	Adress input
$\overline{RAS}$	Row Adress Strobe
$\overline{CAS}$	Column Adress Strobe
DQ1-DQ4	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	Power Supply (5v)
Vss	Ground(0V)
NC	No Connection

Note:The same power supply voltage must be provided to every Vcc pin , and the same GND voltage level must be provided to every Vss pin.

5. BLOCK DIAGRAM



6. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7	V
Short Circuit Output Cuttent	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operation Temperature	T_{opr}	0 to 70	
Storage Temperature	T_{stg}	-55 to 150	

*:Ta = 25

Recommended Operating Conditions

(Ta=0 to70)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

Capacitance

(Vcc = 5V±10%,Ta=25 ,f=1 MHZ)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0-A10)	C_{IN1}	-	5	pF
Input Capacitance ($\overline{RAS}$,$\overline{CAS}$,$\overline{WE}$,$\overline{OE}$)	C_{IN2}	-	7	pF
Output Capacitance (DQ1-DQ4)	$C_{I/O}$	-	7	pF

7. DC Characteristics

(Vcc=5V±10% ,Ta=0 to 70)

Parameter	Symbol	Condition	NT511740C 5J-50		NT511740C 5J-60		NT511740C 5J-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} =-5.0 mA	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	
Output LOW Voltage	V_{OL}	I_{OL} =4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{L1}	0V V_I 6.5V; All other pins not under test = 0V	-10	10	-10	10	-10	10	µA	
Output Leakage Current	I_{L0}	DQ disable 0V V_o 5.5V	-10	10	-10	10	-10	10	µA	
Average Power Supply Current (Operating)	I_{cc1}	$\overline{RAS}$,$\overline{CAC}$ cycling, t_{RC} = Min.	-	120	-	110	-	100	mA	1,2
Power Supply Current (Standby)	I_{cc2}	$\overline{RAS}$, $\overline{CAS}$=VIH	-	2	-	2	-	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$ Vcc-0.2V	-	1	-	1	-	1		
Average Power Supply Current (RAS-only Refresh)	I_{cc3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = VIH, tRC=Min.	-	120	-	110	-	110	mA	1,2
Power Supply Current (Standby)	I_{cc5}	$\overline{RAS}$= VIH, $\overline{CAS}$= VIL, DQ = enable	-	5	-	5	-	5	mA	1
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{cc6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	-	110	-	100	-	90	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{cc7}	$\overline{RAS}$=VIL, $\overline{CAS}$ cycling tpc=Min.	-	110	-	100	-	90	mA	1,3

Notes 1. ICC Max. is specified as Icc for output open condition.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
~~2.~~ 3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

8. AC Characteristics (1/3)

(Vcc=5V±10% ,Ta=0 to 70) Note:1,2,3,12,13

Parameter	Symbol	NT511740C5J-50		NT511740C5J-60		NT511740C5J-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	84	-	104	-	124	-	ns	
Read Modify Write Cycle Time	t_{RWC}	110	-	135	-	160	-	ns	
Fast Page Mode Cycle Time	t_{HPC}	20	-	25	-	30	-	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	58	-	68	-	78	-	ns	
Access Time form $\overline{RAS}$	t_{RAC}	-	50	-	60	-	70	ns	4,5,6
Access Time form $\overline{CAS}$	t_{CAC}	-	13	-	15	-	20	ns	4,5
Access Time form Column Address	t_{AA}	-	25	-	30	-	35	ns	4,6
Access Time form $\overline{CAS}$ Precharge	t_{CPA}	-	30	-	35	-	40	ns	4
Access Time form $\overline{OE}$	t_{OEA}	-	13	-	15	-	20	ns	4
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	-	0	-	0	-	ns	4
Data Output Hold After $\overline{CAS}$ Low	t_{DOH}	5	-	5	-	5	-	ns	
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{CEZ}	0	13	0	15	0	20	ns	7,8
$\overline{RAS}$ to Data Output Buffer Turn-off Delay Time	t_{REZ}	0	13	0	15	0	20	ns	7,8
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	13	0	15	0	20	ns	7
$\overline{WE}$ to Data Output Buffer Turn-off Delay Time	t_{WEZ}	0	13	0	15	0	20	ns	7
Transition Time	t_T	1	50	1	50	1	50	ns	3
Refresh Period	t_{REF}	-	32	-	32	-	32	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	30	-	40	-	50	-	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode with EDO)	t_{RASP}	50	100,000	60	100,000	70	100,000	ns	

AC Characteristics (2/3)

Parameter	Symbol	NT10511740C5J-50		NT511740C5J-60		NT511740C5J-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
$\overline{RAS}$ Hold Time	t_{RSH}	7	-	10	-	13	-	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	7	-	10	-	13	-	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode with EDO)	t_{CP}	7	-	10	-	13	-	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	7	10,000	10	10,000	13	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	35	-	40	-	45	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	-	5	-	5	-	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge Time	t_{RHCP}	30	-	35	-	40	-	ns	
$\overline{OE}$ Hold Time from $\overline{CAS}$ (DQ Disable)	t_{CHO}	5	-	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	11	37	14	45	14	50	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	9	25	12	30	12	35	ns	6
Row Address Set-up Time	t_{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	7	-	10	-	13	-	ns	
Column Address Set-up Time	t_{ASC}	0	-	0	-	0	-	ns	
Column Address Hold Time	t_{CAH}	7	-	10	-	13	-	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	25	-	30	-	35	-	ns	
Read Command Set-up Time	t_{RCS}	0	-	0	-	0	-	ns	
Read Command Hold Time	t_{RCH}	0	-	0	-	0	-	ns	9
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	ns	9
Write Command Set-up Time	t_{WCS}	0	-	0	-	0	-	ns	10

AC Characteristics (3/3)

(Vcc=5V±10% ,Ta=0 to 70) Note 1,2,3,12,13

Parameter	Symbol	NT511740C5J-50		NT511740C5J-60		NT511740A5J-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Hold Time	t_{WCH}	7	-	10	-	13	-	ns	
Write Command Pulse Width	t_{WP}	7	-	10	-	10	-	ns	
$\overline{WE}$ Pulse Width (DQ Disable)	t_{WPE}	7	-	10	-	10	-	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	7	-	10	-	13	-	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	7	-	10	-	10	-	ns	
$\overline{OE}$ Command Hold Time	t_{OCH}	7	-	10	-	10	-	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	7	-	10	-	13	-	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	7	-	10	-	13	-	ns	
Data-in Set-up Time	t_{DS}	0	-	0	-	0	-	ns	11
Data-in Hold Time	t_{DH}	7	-	10	-	13	-	ns	11
$\overline{OE}$ to Data-in Delay Time	t_{OED}	13	-	15	-	20	-	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	30	-	34	-	44	-	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	42	-	49	-	59	-	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	67	-	79	-	94	-	ns	10
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t_{CPWD}	47	-	54	-	64	-	ns	10
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	5	-	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	-	5	-	5	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	-	10	-	10	-	ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	-	10	-	10	-	ns	
$\overline{WE}$ Hold Time $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{WE}$ Set-up Time (Test Mode)	t_{WTS}	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{WE}$ Hold Time (Test Mode)	t_{WTH}	10	-	10	-	10	-	ns	

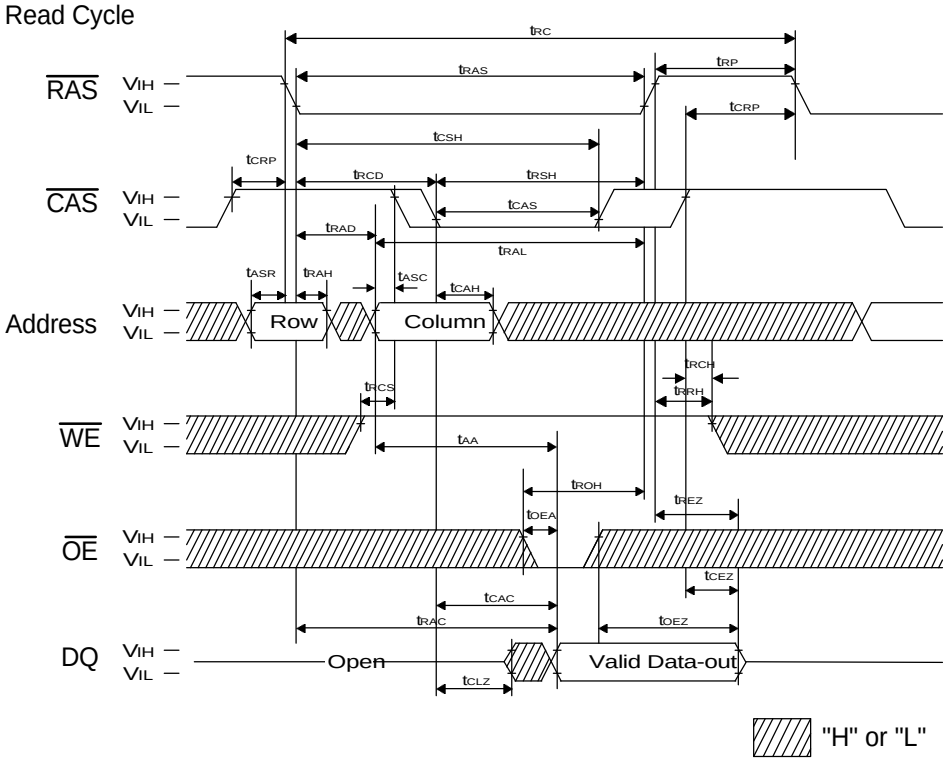
Notes:

1. A start-up delay of 200 μs is required after power-up,followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.
2. The AC characteristics assume t_T=2 ns.
3. V_{IH}(Min.) and V_{IL}(Max.) are reference levels for measuring input timing signals. Transition time (t_T) are measured between V_{IH} and V_{IL}.
4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.
5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only . If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only . If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, access time is controlled by t_{AA}.
7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
8. t_{CEZ} and t_{REZ} must be satisfied for open circuit condition .
9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only . If t_{WCS} t_{WCS}(Min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If t_{CWD} t_{CWD}(Min.) , t_{RWD} t_{RWD}(Min.) , t_{AWD} t_{AWD}(Min.) and t_{CPWD} t_{CPWD}(Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to CAS leading edge in an early write cycle, and to WE leading edge in an OE control write cycle or a read modify write cycle .
12. The test mode is initiated by performing a WE and CAS before RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test mode CA0 and CA1 are not used and each DQ pin now accesses 8-bit locations .Since all 4 DQ pins are used, a total of 32 data bits can be written in parallel into the memory array. In a read cycle, if 8 data bits are equal the DQ pin will indicate a high level. If the 8 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a RAS-only refresh cycle or a CAS before RAS refresh cycle.
13. In a test mode read cycle , the value of access time parameters is delayed for 5 ns for the specified value . These parameters should be specified in test mode cycle by adding the above value

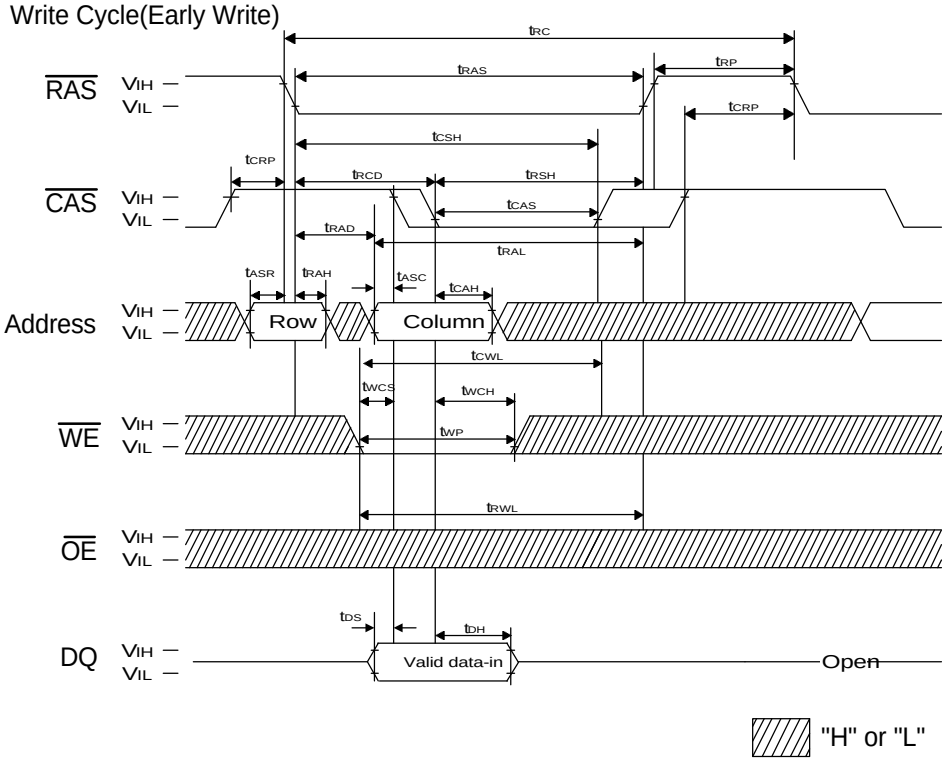
to the specified value in this data sheet.

9. DRAM AC Timing Waveforms

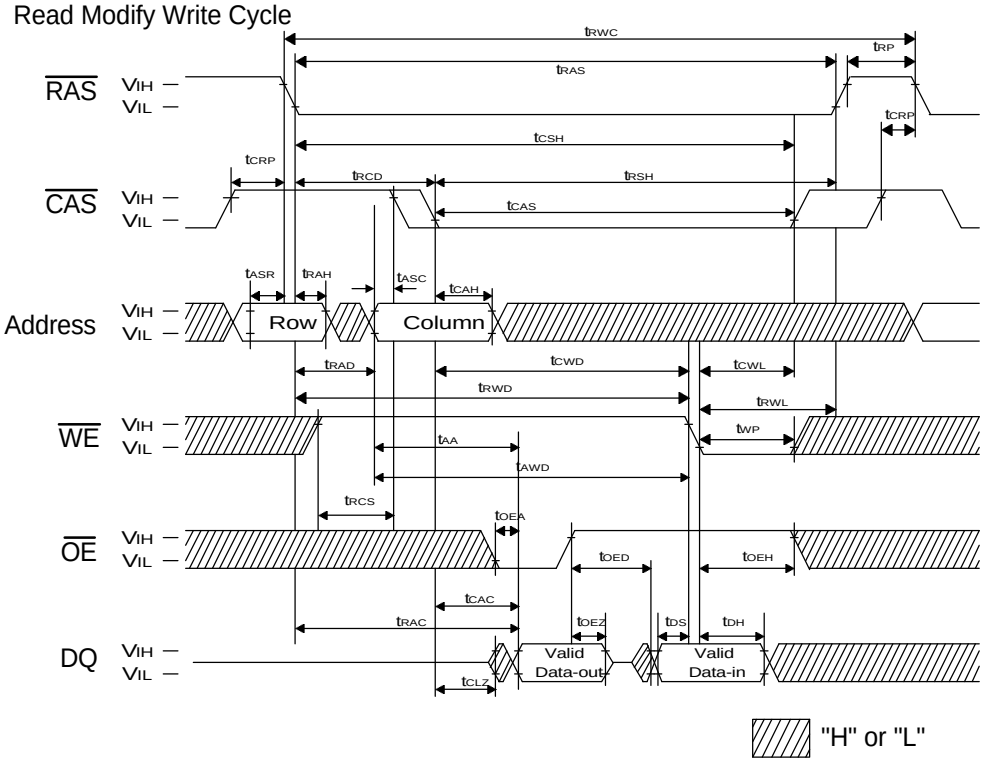
Read Cycle



Write Cycle(Early Write)



Read Modify Write Cycle



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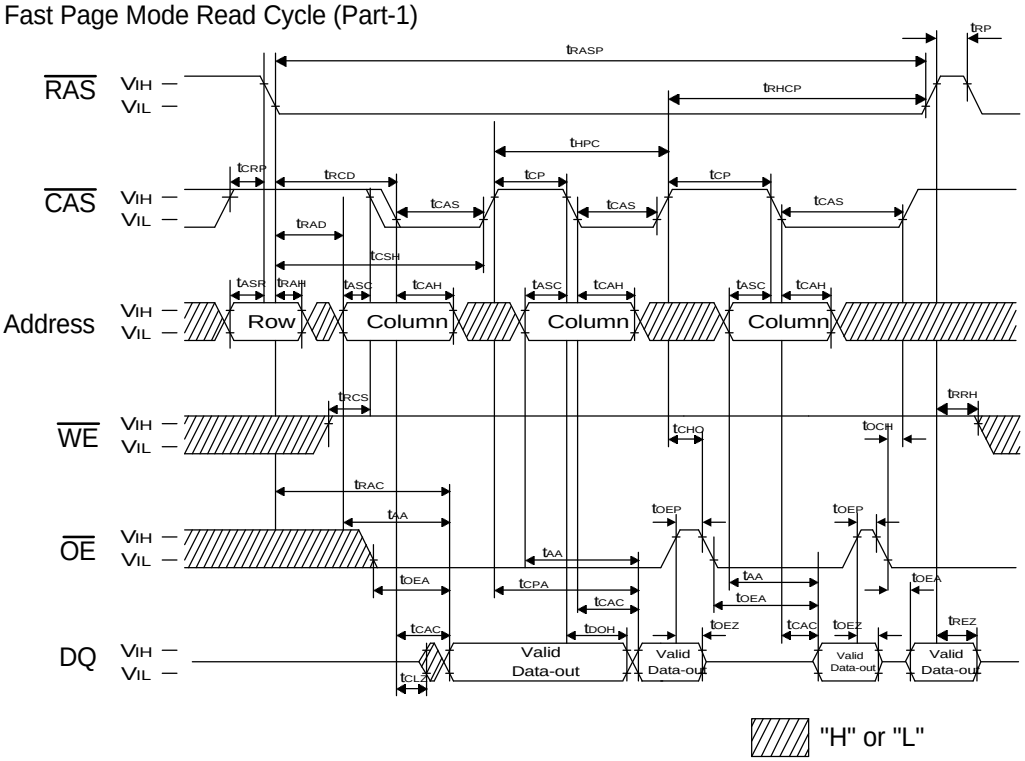
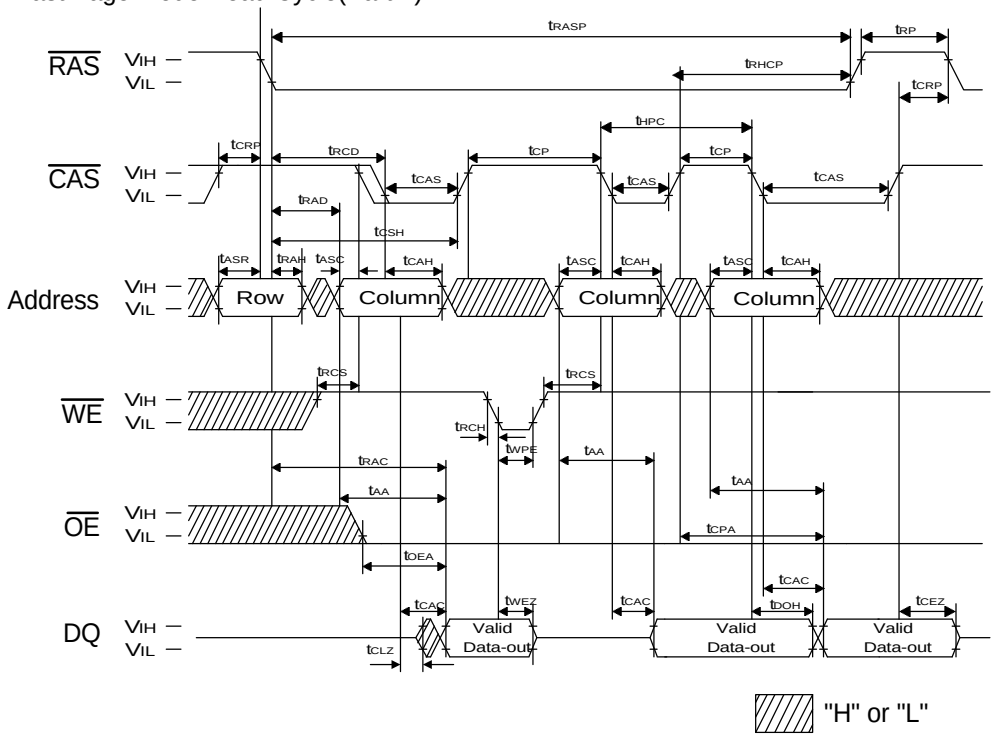
Fast Page Mode Read Cycle (Part-1)



Fast Page Mode Read Cycle(Part-2)



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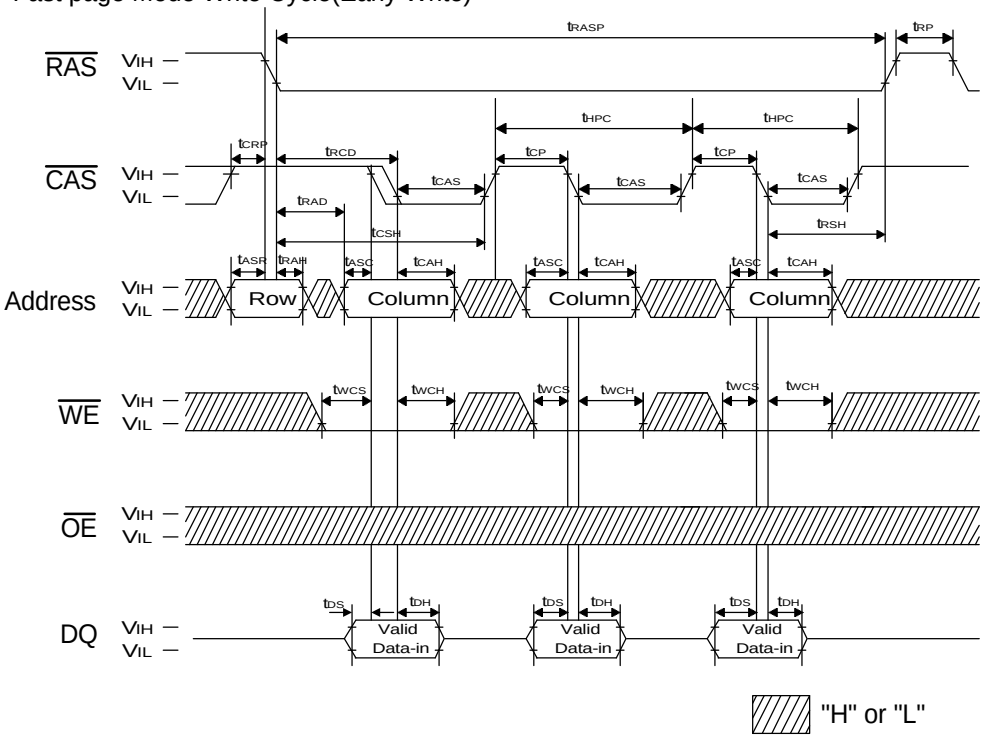
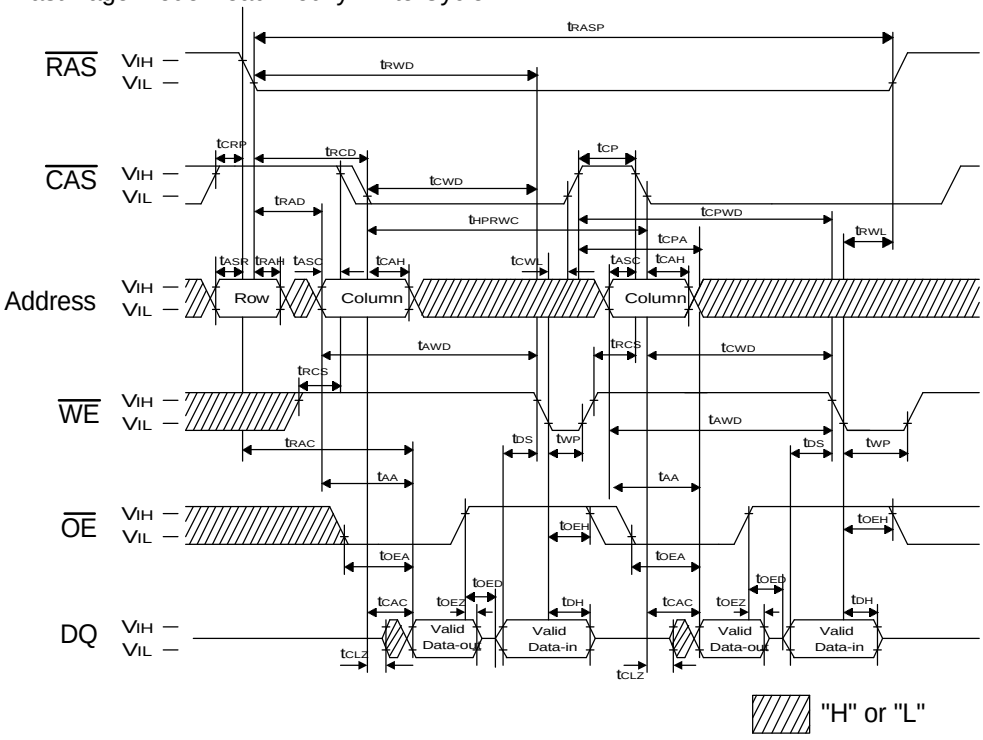
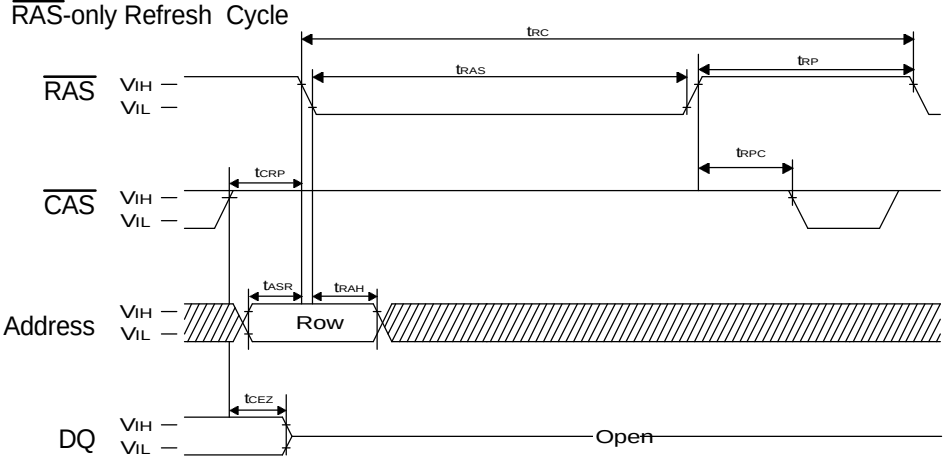
Fast page Mode Write Cycle(Early Write)



Fast Page Mode Read Modify Write Cycle

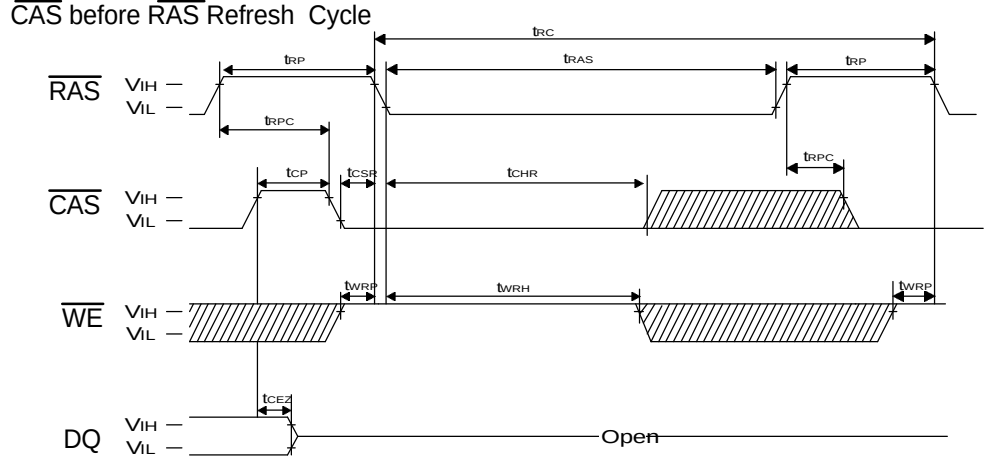


RAS-only Refresh Cycle



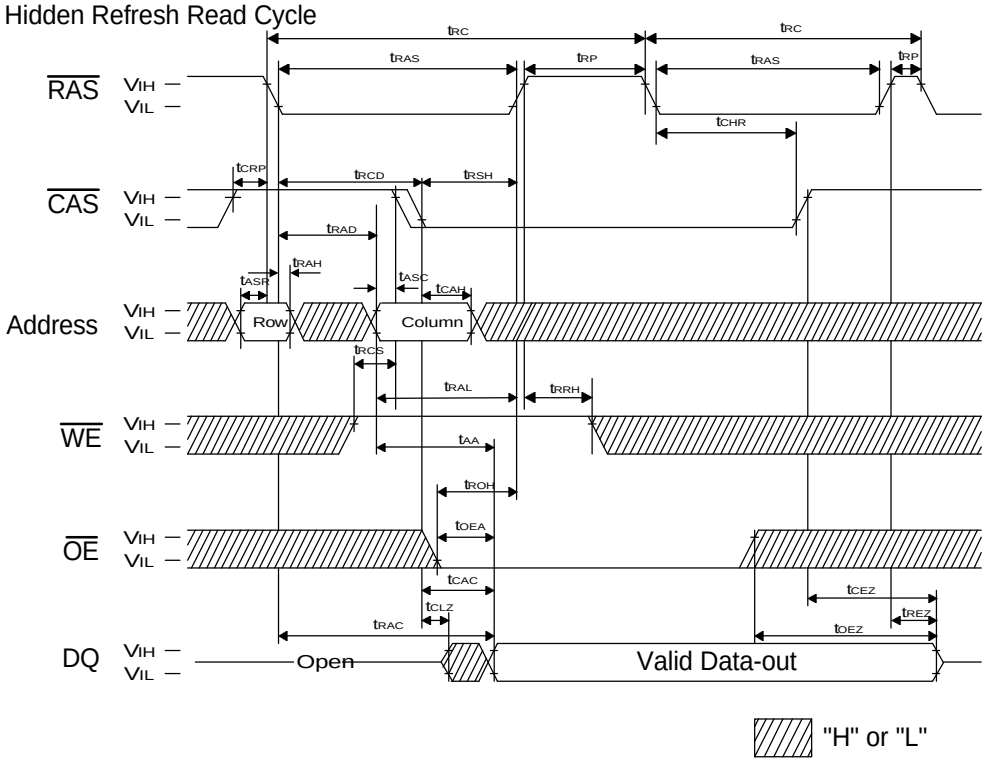
Note:$\overline{WE}$,$\overline{OE}$="H" or "L" "H" or "L"

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

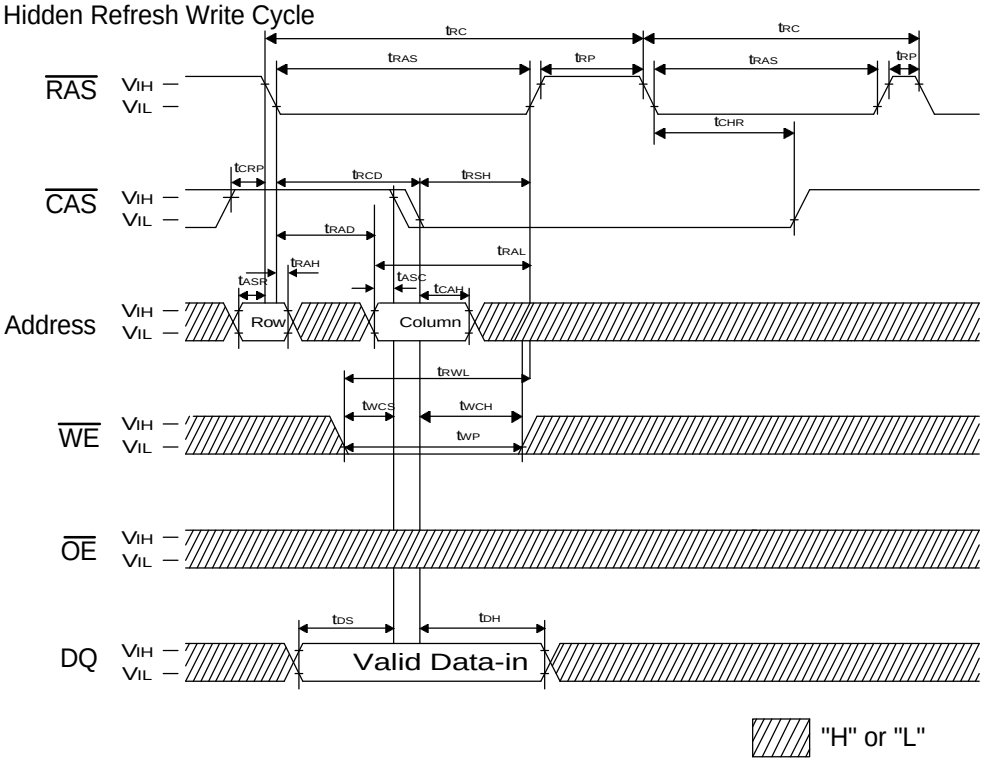


Note:$\overline{OE}$,Address="H" or "L" "H" or "L"

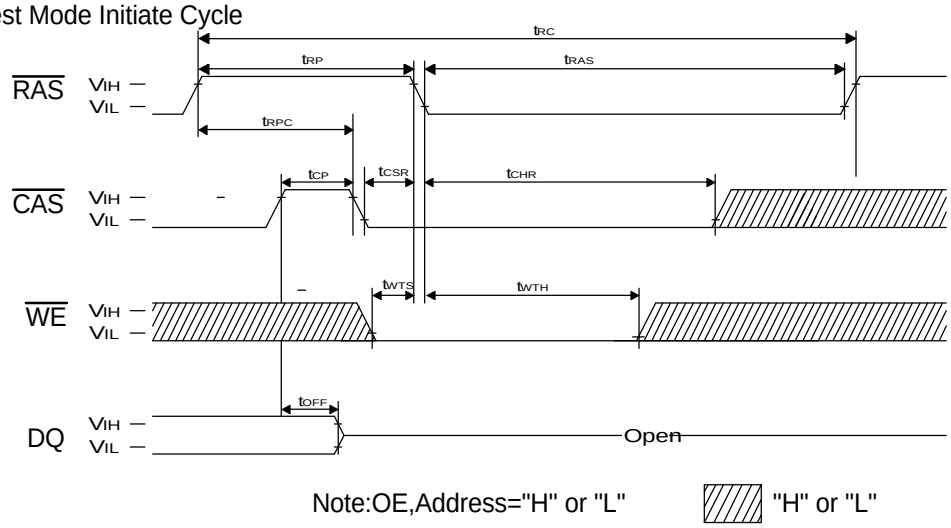
Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



Test Mode Initiate Cycle



Note:OE,Address="H" or "L" "H" or "L"