National

NOVEMBER 1973

DATA UPDATE 6

A continuing service from National . . .

DATA UPDATE makes it easier for you to keep abreast of new products from National. It's a collection of our latest data sheets and applications literature.

DATE UPDATE is separated into discrete and integrated circuit sections. Within each section the first page of each data sheet appears alphanumerically by product family. If a product interests you, just circle the appropriate update number on the business reply card to receive the complete data sheet.

6

This edition of DATA UPDATE covers the following devices:

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DATA UPDATE 5
included the following products:

5

SEMICONDUCTOR PRODUCTS/ HYBRID PRODUCTS

4

DATA UPDATE 4 included the following products:

INTEGRATED CIRCUITS

3

DATA UPDATE 3
included the following products:

2

DATA UPDATE 2
included the following products:

INTEGRATED CIRCUITS, ANALOG SWITCHES

1

DATA UPDATE 1
included the following products:

DIGITAL

DM5423/DM7423 expandable dual 4-input NOR gate with strobe
DM5425/DM7425 dual 4-input NOR gate with strobe
DM5427/DM7427 triple 3-input NOR gate

general description

The three NOR gates described here were designed to provide additional versatility to the line of Series 54/74 functions.

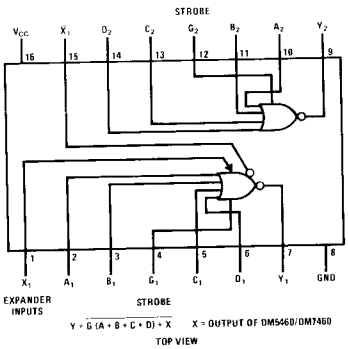
The DM5423/DM7423 has the added features of a Strobe input which is AND'ed with the four normal inputs, and a pair of expandable inputs which can accept logic levels from the DM5460/DM7460, dual 4-input expander gate, resulting in a larger number of OR'ed terms.

The DM5425/DM7425 is similar to the DM5423/DM7423 except that it has no expandable inputs.

The DM5427/DM7427 has neither expandable inputs nor Strobe.

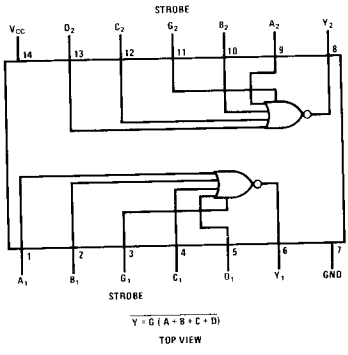
logic and connection diagrams

Dual-In-Line and Flat Package



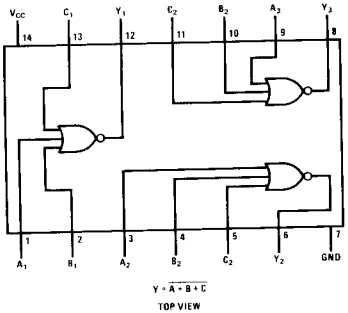
DM5423/DM7423

Dual-In-Line and Flat Package



DM5425/DM7425

Dual-In-Line and Flat Package



DM5427/DM7427

Circle DATA UPDATE No. 253

DM54196/DM74196, DM54197/DM74197
40 MHz presettable decade and binary counters/latches

general description

These high-speed monolithic counters consist of four dc coupled master/slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (DM54196/DM74196) or a divide-by-two and a divide-by-eight counter DM54197/DM74197. These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 40 MHz at the clock 1 input and 0 to 20 MHz at the clock 2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

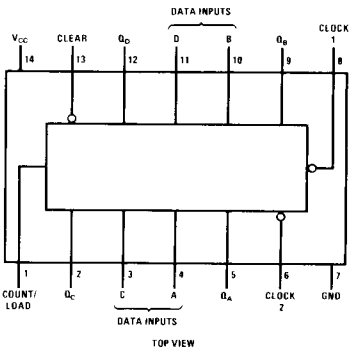
All inputs are diode-clamped to minimize transmission line effects and simplify system design. The circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 150 mW. The DM54196 and DM54197 circuits are characterized for operation over the full military temperature range of −55°C to +125°C; the DM74196 and DM74197 circuits are characterized for operation from 0°C to +70°C.

features

- DC coupled counters designed to replace Signetics 8280, 8281, 8290, and 8291 counters in most applications
- Performs BCD, bi-quinary, or binary counting
- Fully independent clear input
- Guaranteed to count at input frequencies from 0 to 40 MHz
- Input clamping diodes simplify system design

connection diagram

Dual-In-Line Package



TOP VIEW

Circle DATA UPDATE No. 254

DM7511/DM8511 dual gated D flip-flop
DM7512/DM8512 dual gated master/slave JK/D flip-flop
DM7613/DM8613 quad gated D flip-flop

general description

The DM7511/DM8511 is a dual gated D flip-flop. Each flip-flop has its own clock, clear and two gated inputs. Both gate inputs must be low to enable data transfer to the output.

The DM7512/DM8512 is a dual flip-flop which can operate in either a J, K mode or in a D-type mode. Both flip-flops operate from a common clock and a common asynchronous clear but have separate mode inputs so that one can operate as a J, K flip-flop while the other is operating as a D-type flip-flop. (See truth table.)

The DM7613/DM8613 is a quad gated D flip-flop with direct clear and gated inputs. The latter if set to a logical "1" level will inhibit data entry from the data input.

features

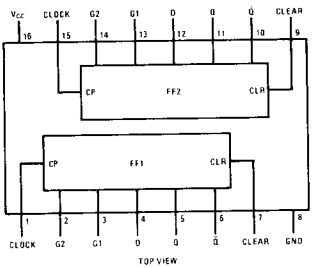
- Additional "do-nothing" state
- Positive edge triggering
- Guaranteed operation

DM7511/DM8511	30 MHz
DM7512/DM8512	20 MHz
DM7613/DM8613	20 MHz

- DM7512/DM8512 pin compatible with DM75L12/DM85L12
- DM7613/DM8613 common clock and clear

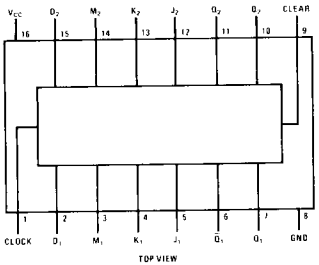
connection diagrams

DM7511/DM8511
Dual-In-Line and Flat Packages



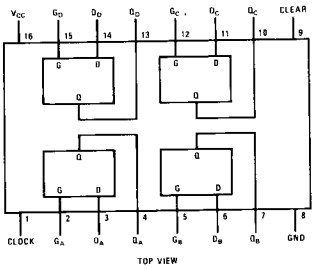
TOP VIEW

DM7512/DM8512
Dual-In-Line and Flat Packages



TOP VIEW

DM7613/DM8613
Dual-In-Line and Flat Packages



TOP VIEW

Circle DATA UPDATE No. 255

DM76L13/DM86L13 quad gated D flip-flop

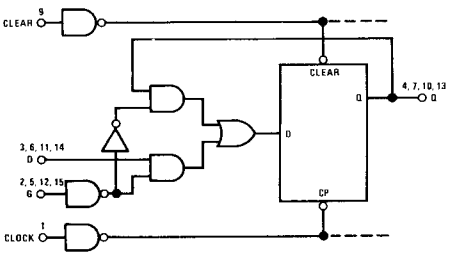
general description

The DM76L13/DM86L13 is a low power TTL quad gated D flip-flop with direct clear and gated inputs. The gate, if set to a logical "1" level, will inhibit data entry from the data input.

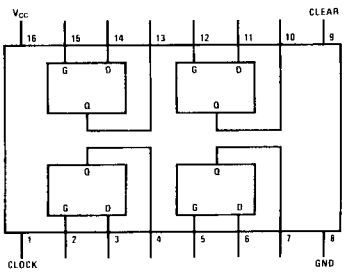
features

- Positive-edge-triggered, buffered clock
- Typical power dissipation 25 mW
- Typical propagation delay 70 ns
- Pin compatible with std. TTL DM7613/DM8613

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

Circle DATA UPDATE No. 256

DM7802/DM8802, DM7806/DM8806
high speed MOS to TTL level converters

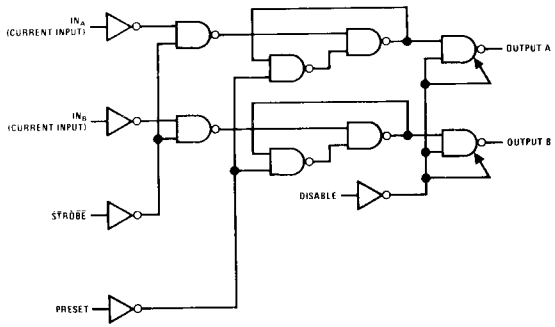
general description

The DM7802/DM8802, DM7806/DM8806 are high speed MOS to TTL level converters. These circuits act as an interface level converter between MOS and TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE® output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

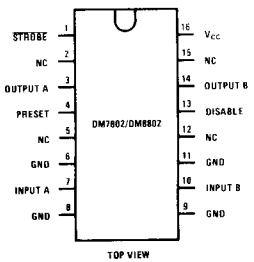
features

- Very low output impedance — high drive ability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter

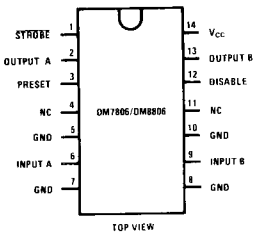
logic and connection diagrams



Dual-In-Line Package



Dual-In-Line and Flat Package



Circle DATA UPDATE No. 257

DM7853/DM8853 dual retriggerable resettable monostable multivibrator

general description

The DM7853/DM8853 is a dual retriggerable, resettable monostable multivibrator similar to the DM9602/DM8602 but with a unique input triggering logic.

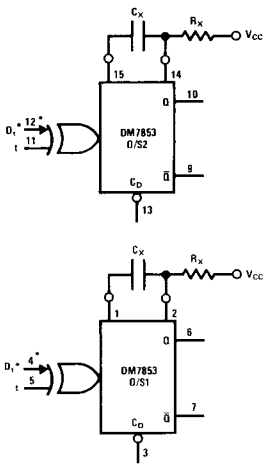
This device has two trigger inputs—a standard input and a delayed input—which are Exclusive OR'ed together. In the dual-edge triggering mode, the two inputs are tied together. On either a positive or negative transition the Exclusive-OR logic is satisfied for a length of time equal to the delay on the delayed input—approximately 15 ns—thus triggering or retriggering the one-shot.

Once fired, the accuracy and performance of the DM7853/DM8853 is identical to that of the DM9602/DM8602.

features

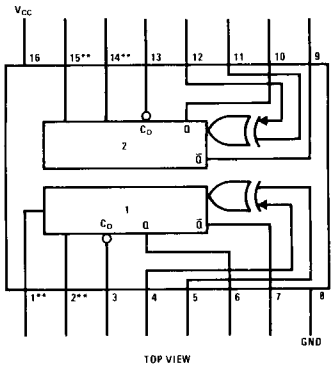
- 72 ns to ∞ output width range
- Retriggerable 0 to 100% duty cycle
- TTL input gating—leading AND/OR trailing edge triggering
- Complementary TTL outputs
- Pulse width compensated for V_{CC} and temperature variations
- Resettable

logic and connection diagrams



*A NON-INVERTING BUFFER WITH DELAY

Dual-In-Line and Flat Package



TOP VIEW

**PINS FOR EXTERNAL TIMING.

truth tables

Triggering Truth Table

t	Dt	CD	OPERATION
L → H	L	H	Trigger
H	H → L	H	Trigger
H → L	H	H	Trigger
L	L → H	H	Trigger
H → L	Same as t	H	Trigger
L → H	Same as t	H	Trigger
X	X	L	Reset

Loading Rules

INPUTS	LOAD	
	HIGH	LOW
3, 4, 5, 11, 12, 13	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6, 7, 9, 10	16 U.L.	8 U.L.

Circle DATA UPDATE No. 258

DM9334/DM8334 8-bit addressable latch

general description

The DM9334/DM8334 is a high speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level High outputs. The device also incorporates an active level Low common clear for resetting all latches, as well as, an active level Low enable.

The DM9334/DM8334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the Low state. In the clear mode all outputs are Low and unaffected by the address and data inputs.

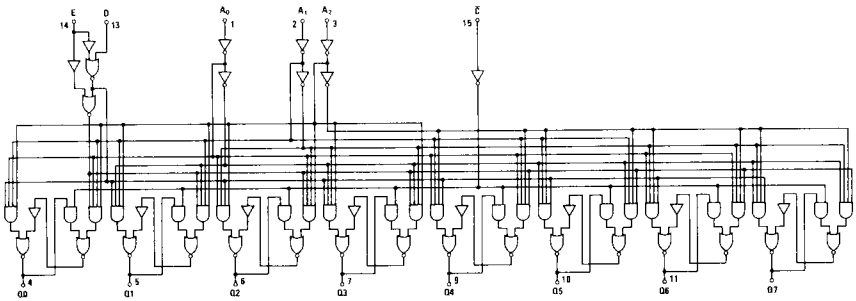
When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operation of the product.

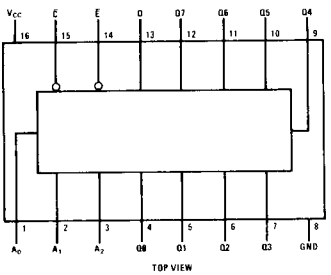
features

- Serial to parallel capability
- 8-bits of storage with output of each bit available
- Random (addressable) data entry
- Active high demultiplexing or decoding capability
- Easily expandable
- Common clear
- Input clamp diodes limit high speed termination effects

logic and connection diagrams



Dual-In-Line and Flat Packages



TOP VIEW

Circle DATA UPDATE No. 259

MOS

MM4229/MM5229 3072-bit read only memory (open drain)

general description

The MM4229/MM5229 is a 3072-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized in a 256 x 12 bit word configuration.

Customer programs may be supplied on Hollerith coded punched cards.

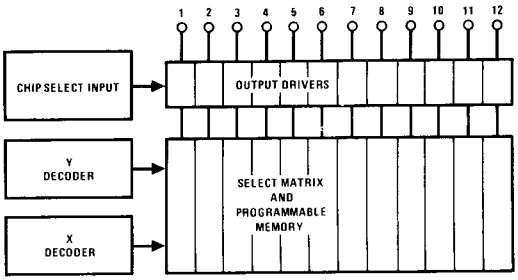
features

- TTL compatible
- Low standby power
- Programmable chip select inputs
- Typical 1.0μs access time
- Open drain outputs allow wire-OR of up to 8 devices

applications

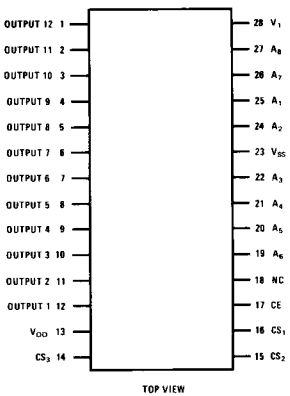
- Code conversion
- Random logic synthesis
- Table look-up
- Micro-programming

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Circle DATA UPDATE No. 260

MM4261/MM5261 1024-bit fully decoded dynamic random access memory

general description

The MM4261/MM5261 fully decoded dynamic 1024 word x 1-bit word read/write Random Access Memory is a monolithic MOS integrated circuit using silicon gate low threshold technology to achieve bipolar compatibility on all I/O lines except the precharge and read/write lines. This provides an efficient approach to memory design using these systems oriented devices. The MM4261/MM5261 is used for main memory applications where large bit storage and improved operating performance are important. A TRI-STATE® output is utilized to allow wired "OR" capability and common I/O data busing in memory applications.

features

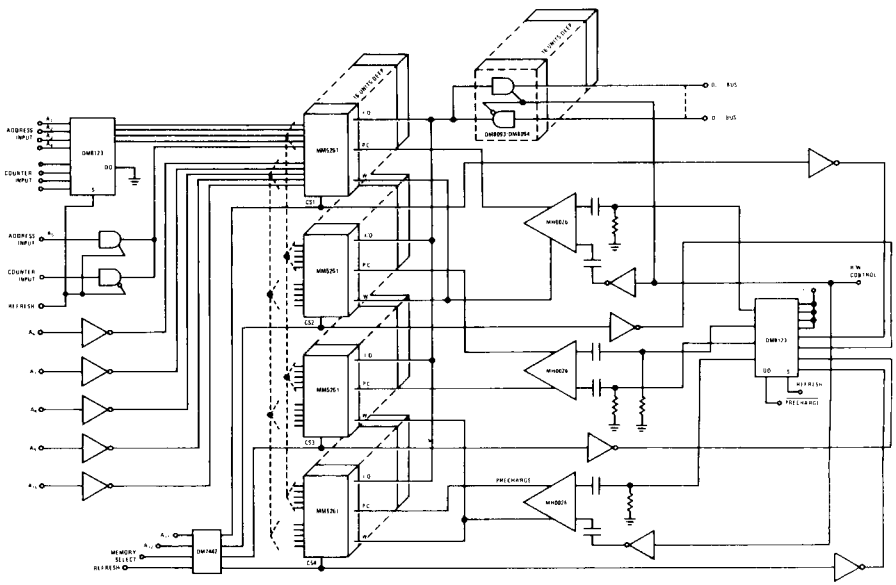
- Fast access time 300 typ
- Fast cycle time MM4261 600 ns read cycle min
  MM5261 500 ns read cycle min
  MM4261 750 ns write cycle min
  MM5261 625 ns write cycle min
- Low overhead circuit count Fully decoded
- Systems-oriented design
  Bipolar compatible (address lines, chip enable data I/O)
  Common data I/O line
  TRI-STATE output
- Refresh cycle 2.0 ms
- Easy memory expansion Chip enable
- Device protection All I/O lines have protection against static charge
- Low power dissipation 400 mW
- Small package size 18 pin dual-in-line package

applications

- High speed mainframe memory
- Mass memory storage

typical application

Main Memory Module Storing 4096 16-Bit Words



Circle DATA UPDATE No. 261

MM4262/MM5262 2048-bit fully decoded dynamic random access read/write memory

general description

The MM4262/MM5262 is a fully decoded 2048 word by 1 bit dynamic read/write random access memory fabricated using National Semiconductor's proprietary silicon gate low threshold technology. All inputs except the clocks are TTL compatible. The output provides a current pulse allowing a large number of devices to be bussed together without compromising system performance due to capacitive loading. The current pulse output is converted to TTL levels by means of a sense amplifier.

features

	MM4262	MM5262
■ Fast access time	470 ns (max)	365 ns (max)
■ Fast cycle time		
Short Read	565 ns (min)	475 ns (min)
Read/Write	750 ns (min)	635 ns (min)
Write	750 ns (min)	635 ns (min)
■ Refresh cycle	1.0 ms	2.0 ms

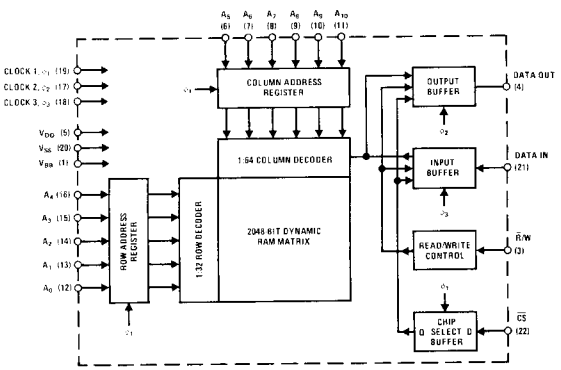
	MM4262	MM5262
■ Low power		
Operating	360 mW (max)	400 mW (max)
Standby	2.5 mW (max)	2.5 mW (max)

- Power supplies +5.0V, +8.5V, −15V
- Low overhead circuits: Fully decoded with internal memory address register
- System oriented design
  - Bipolar compatible except for clocks
  - Current sense output
  - $\overline{\text{Chip Select}}$ for easy memory expansion
- Package: 22 pin DIP (Cavity and Molded)
- Device protection: All inputs and outputs protected against static charge

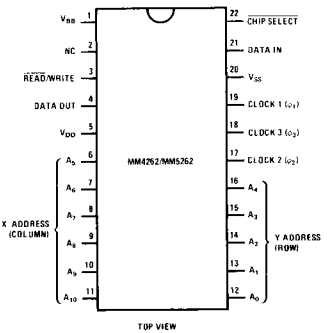
applications

- Core memory replacement
- Mainframe memory
- Buffer storage
- Non-volatile memory using battery back up

block and connection diagrams



Dual-In-Line Package



ordering information

ORDER NUMBER	PACKAGE	TEMPERATURE RANGE
MM4262D	22 Pin Cavity DIP (D)	55°C to +125°C
MM5262D	22 Pin Cavity DIP (D)	0°C to +70°C
MM5262N	22 Pin Molded DIP (N)	0°C to +70°C

recommended interface circuits

CLOCK DRIVERS: MH0026, MH8808

SENSE AMPLIFIERS: LM167, LM168, DM7806/DM8806

Circle DATA UPDATE No. 262

National National 74C Times Semiconductor

VOLUME 1, NUMBER 1 DECEMBER 1973

NATIONAL 74C TIMES

The 74C TIMES is a semi-monthly publication dedicated to keeping the engineers informed of new products and design techniques using 74C. Each edition will feature an article on various subjects such as CMOS applications, production techniques, power saving tips, etc. A second article will be from one of our readers who has sent in application ideas and will receive $50.00 if we select the application for publication. Send your application ideas to: Bob Bennett, CMOS Product Marketing Manager, National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, California 95051.

TELEDYNE A 74C SECOND SOURCE

Teledyne Semiconductor will be making twelve 74C Second Source parts available in the next 4 months. Their plans are to second source the entire line by second quarter 1974. National welcomes Teledyne aboard the 74C Band Wagon.

The initial 74C parts that Teledyne will build are as follows:

- 74C00 quad 2-input NAND gate
- 74C04 hex inverter
- 74C42 BCD to decimal decoder
- 74C74 dual D flip-flop
- 74C107 dual J-K flip-flop
- 74C160 decade counter with asynchronous clear
- 74C161 binary counter with asynchronous clear
- 74C162 decade counter with synchronous clear
- 74C163 binary counter with synchronous clear
- 74C192 synchronous 4-bit up/down decade counter
- 74C193 synchronous 4-bit up/down binary counter
- 74C195 4-bit shift register

NEW PRODUCTS MM54C89/MM74C89 64-BIT RAM

The MM54C89/MM74C89 is a TRI-STATE® static CMOS RAM. It is organized in a matrix to provide 16 words of 4-bits each. Each of the 16 words is addressed in straight binary with full on chip decoding. The access time will be 120ns typ. at 10V V_{CC} with a 50pF load. The power will be a low 100mW typ.

In an effort to bring out the best CMOS equivalent 7400 function we have chosen to build the following products instead of the previously announced future products.

OLD SELECTION

- MM74C13, Dual Schmitt Trigger
- MM74C123, Dual Monostable Multivibrator

NEW SELECTION

- MM74C14, Hex Schmitt Trigger
- MM74C221, Dual Monostable Multivibrator

HANDLING PROCEDURES FOR CMOS INTEGRATED CIRCUITS

BY FRANK BARONE
CMOS PRODUCTION MANAGER
NATIONAL SEMICONDUCTOR

All MOS devices are susceptible to damage by the electrostatic discharge of energy through the devices. This is due to the fact that the gate oxide thickness of these devices is generally in the range of 1000Å to 1500Å which limits the maximum voltage that can be applied to the input of a device to 60V with a reasonable safety factor. Although all MOS devices have input protection networks which are effective in a large number of device handling situations, they are not effective in 100% of the cases. To make them so would obviously affect the performance of the devices.

In order to be totally safe, proper handling procedures must be used to eliminate damage and subsequent yield loss due to static electrical charges. It is the purpose of this article to outline proper handling procedures for MOS devices.

GENERAL OPERATING PROCEDURES

1. The leads of MOS devices should be in contact with conductive material to avoid build-up of static charge. Containers used for transporting or storing MOS devices should be made of conductive material or lined with conductive material. Rails for handling and shipping MOS devices should be made of conductive material or coated with anti-static material. In no case should MOS devices be inserted into polystyrene foam or other high dielectric materials.
2. MOS devices and/or circuit boards containing MOS devices should not be inserted into or removed from Test Circuits and/or Burn-In Circuits with power on because transient voltages may cause permanent damage.
3. Signals should not be applied to the inputs of MOS devices while power supplies are in the off condition or disconnected.
4. All unused inputs must be connected to either the power supply (V_{DD}) or ground (V_{SS}).
5. All electrical equipment should be hard-wired to ground. Soldering iron tips, metal parts of fixtures and tools, and handling systems should be grounded.
6. In the case of any mechanical operation or equipment which is capable of generating static electrical charges and cannot be hard wired to the electrical ground system, an ionized air blower should be used to neutralize any static charge generated.
7. Manufacturing operating personnel should wear anti-static smocks and gloves. When handling individual MOS devices personnel should be grounded using conductive wrist straps. In no case should an operator be attached to a hard ground. There should always be at least a 1 megohms series resistor between the operator and ground.
8. All work stations should have conductive material work surfaces and conductive material floor mats connected to a common ground system.

Chairs and stools should be made of metal or covered with anti-static material to prevent static charge generation.

HANDLING MOS DICE

Carriers used for transporting and storing MOS dice should be made of conductive material or contain a conductive material overly to prevent static charge build-up.

All assembly equipment should be hard wired to ground. This includes die bonders, wire bonders, sealing stations, test equipment and fixtures.

Bonding Sequence – always connect gate input protection circuitry first. This means connecting the most positive pad first (V^+, V_{CC}, or V_{DD}), then most negative supply (V^-, GND, or V_{SS}). The remaining pads can be connected in any sequence.

HANDLING OF SUBASSEMBLIES

Subassembled modules and printed circuit boards should be manufactured and handled using the same procedures as described above for individual MOS devices.

Circuit boards containing MOS devices which are being transported between work stations, and assembly and test areas should be contained within anti-static material or have all board terminals shorted together using a conductive shorting bar. These precautions should be taken until the subassembly is inserted into the complete system in which the proper voltages are applied.

In no cases should subassemblies be constructed, fixtured, stored, or transported in polystyrene material or any other high dielectric materials.

ELECTRICAL FAILURE MODES DUE TO IMPROPER HANDLING

If proper handling techniques are not followed it is likely that the generation of static electrical charges will damage the MOS devices resulting in inoperable or degraded units. Typical failure modes are listed below:

1. Shorted or leaky input protection diodes,
2. Shorted or open gates,
3. Open metal paths in the device input circuitry,
4. Degraded device characteristics especially g_m (mutual transconductance or "gain").

The presence of these failure modes can easily be detected using a transistor curve-tracer.

CMOS SHIPS IN ANTI-STATIC TUBES

In August 1972 National started to ship its CMOS in plastic rails with an anti-static coating on the inside. This coating prevents static build-up inside the tube, thus preventing damage to the enclosed CMOS parts. The year-and-a-half history of this new tube has found it to be very successful. Thus far there has been no returns of unit failures because the parts were electrically damaged during shipment.

CMOS STATUS

PRODUCT	DESCRIPTION	STATUS
MM74C00	Quad 2-input NAND Gate	Announced
MM74C02	Quad 2-input NOR Gate	Announced
MM74C04	Hex Inverter	Announced
MM74C08	Quad 2-input AND Gate	December
MM74C10	Triple 3-input AND Gate	Announced
MM74C14	Quad Schmitt Trigger	2nd Qtr. '74
MM74C20	Dual 4-input NAND Gate	Announced
MM74C30	8-input NAND Gate	December
MM74C32	Quad 2-input OR Gate	2nd Qtr. '74
MM74C42	BCB-to-Decimal Decoder	Announced
MM74C48	BCB-to-7 Segment Decoder	2nd Qtr. '74
MM74C73	Dual J-K F/F	Announced
MM74C74	Dual D F/F	Announced
MM74C76	Dual J-K F/F	Announced
MM74C83	4-bit Binary Full Adder	1st Qtr. '74
MM74C85	4-bit Comparator	December
MM74C86	Quad Exclusive OR Gate	December
MM74C89	64-bit RAM	December
MM74C95	4-bit R-S L-S Register	Announced
MM74C107	Dual J-K F/F	Announced
MM74C221	Dual Monostable Multivibrator	2nd Qtr. '74
MM74C151	8 Channel Digital Multiplexer	Announced
MM74C154	4 to 16 Decoder/Demultiplexer	Announced
MM74C157	Quad 2-input Multiplexer	Announced
MM74C160	Sync Decode Counter	Announced
MM74C161	Sync Binary Counter	Announced
MM74C162	Fully Sync Decode Counter	Announced
MM74C163	Fully Sync Binary Counter	Announced
MM74C164	8-bit S-in P-out S/R	Announced
MM74C165	8-bit P-in S-out S/R	December
MM74C173	TRI-STATE Quad D F/F	Announced
MM74C174	Hex D F/F	1st Qtr. '74
MM74C175	Quad D F/F	3rd Qtr. '74
MM74C192	Sync. Up/Down Decade Counter	Announced
MM74C193	Sync. Up/Down Binary Counter	Announced
MM74C195	4-bit Parallel S/R	Announced
MM74C900	Quad Bilateral Switch	3rd Qtr. '74
MM74C901	Hex Inverting Buffer (T^2L Interface)	December
MM74C902	Hex Buffer (T^2L Interface)	December
MM74C903	Hex Inverting Buffer (MOS Interface)	December
MM74C904	Hex Buffer (MOS Interface)	December
MM74C905	Successive Approximation Register	3rd Qtr. '74
MM80C95	TRI-STATE Hex Buffer	Announced
MM80C96	TRI-STATE Hex Inverting Buffer	4th Qtr. '74
MM80C97	TRI-STATE Hex Buffer	Announced
MM80C98	TRI-STATE Hex Inverting Buffer	4th Qtr. '74
MM85C55	TRI-STATE Decade Counter	4th Qtr. '74
MM85C56	TRI-STATE Binary Counter	4th Qtr. '74

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, California 95051 (408) 732-5000 TWX (910) 339-9240

MM4617A/MM5617A divide-by-10 counter/divider with 10 decoded outputs

general description

The MM4617A/MM5617A is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit. The counter is cleared to its zero count by a logical "1" on its reset line. The counter is advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the MM4617A/MM5617A permits medium speed operation and assures a hazard free counting sequence. The 10 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10 clock input cycles and is used as a ripple carry signal to any succeeding stages.

features

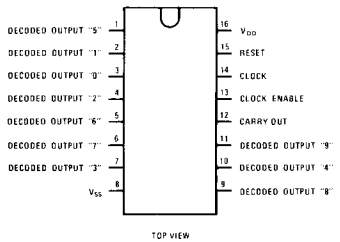
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Medium speed operation	5.0 MHz typ with 10V V_{DD}
■ Low power	10μW typ
■ Fully static operation	

applications

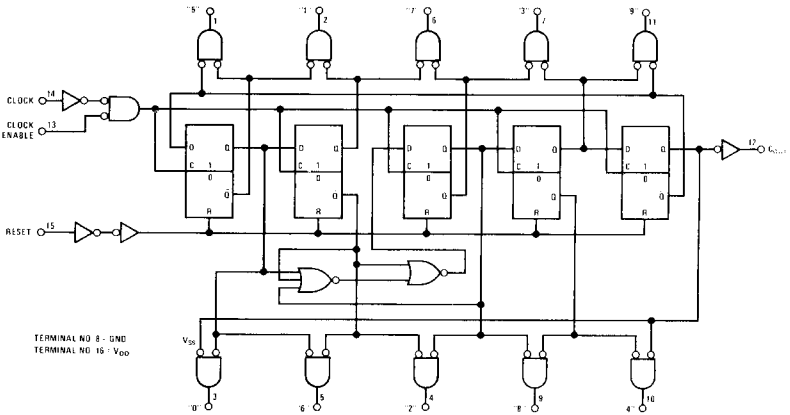
- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

connection and logic diagrams

Dual-In-Line and Flat Package



TOP VIEW



Circle DATA UPDATE No. 263

MM4625A/MM5625A triple three-input NOR gate

general description

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

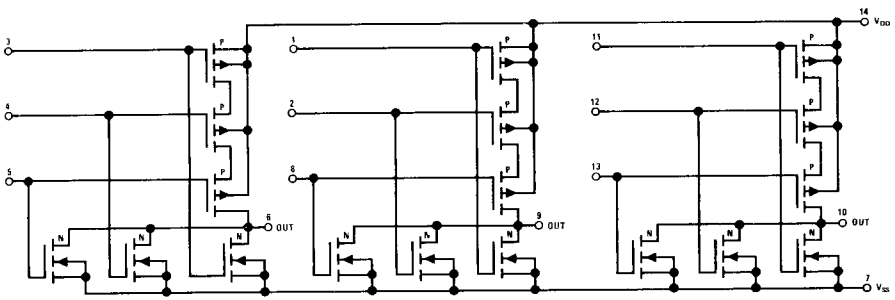
features

- Wide supply voltage range 3.0V to 15V
- Low power 10 nW (typ.)
- High noise immunity 0.45 V_{DD} (typ.)
- Medium speed operation $t_{PHL} = t_{PLH}$ = 25 ns (typ.) at C_L = 15 pF

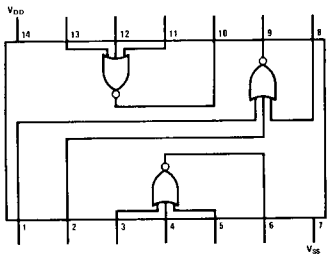
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

MM4627A/MM5627A dual JK master/slave flip-flop with set and reset

general description

These dual JK flip-flops are monolithic Complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset and clock inputs and buffered Q and $\overline{Q}$ outputs. These flip-flops are edge sensitive to the clock input and change state on the positive going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

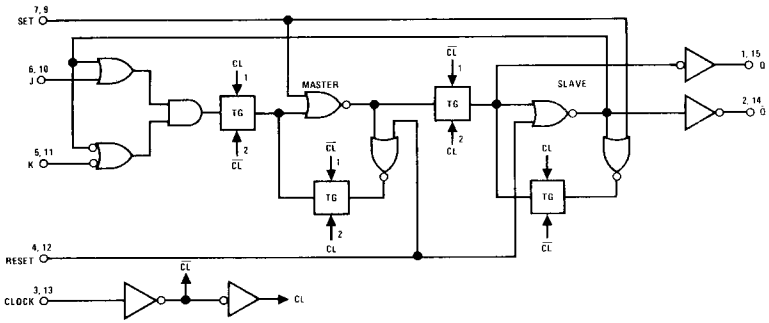
features

- Wide supply voltage range — 3.0V to 15V
- Low power — 50 nW typ
- Medium speed operation — 8.0 MHz typ with 10V supply
- High noise immunity — 0.45 V_{CC} typ

applications

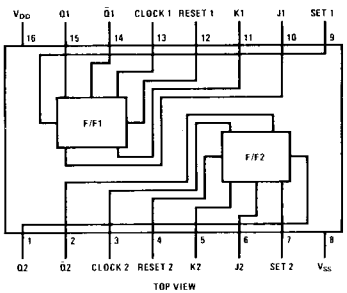
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Computers

schematic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Circle DATA UPDATE No. 265

MM4630A/MM5630A quad EXCLUSIVE-OR gate

general description

These EXCLUSIVE-OR gates are monolithic Complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

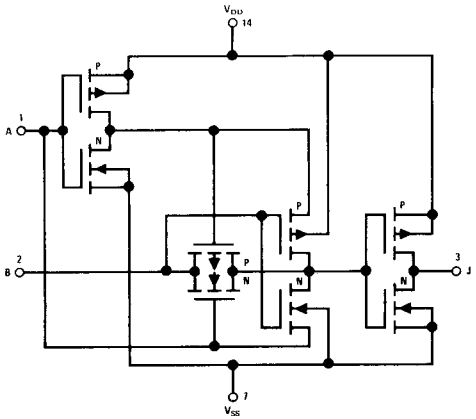
features

- Wide supply voltage range 3.0V to 15V
- Low power 100 nW (typ)
- Medium speed operation $t_{PHL} = t_{PLH} = 40$ ns (typ) at $C_L = 15$ pF, 10V supply
- High noise immunity 0.45 V_{CC} (typ)

applications

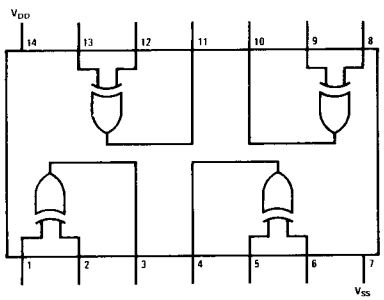
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

schematic diagram



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

Circle DATA UPDATE No. 266

MM4635A/MM5635A 4-bit parallel-in/parallel-out shift register

general description

The MM4635A/MM5635A 4-bit parallel-in/parallel-out shift register is a monolithic complementary MOS (CMOS) integrated circuit constructed with P and N-channel enhancement mode transistors. This shift register is a four-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via $J\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (Parallel/Serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the Parallel/Serial control is "high."

In the parallel or serial mode information is transferred on positive clock transitions.

When the True/Complement control is "high," the True contents of the register are available at the output terminals. When the True/Complement control is "low," the outputs are the complements of the data in the register. The True/Complement control functions asynchronously with respect to the clock signal.

$J\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With $J\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

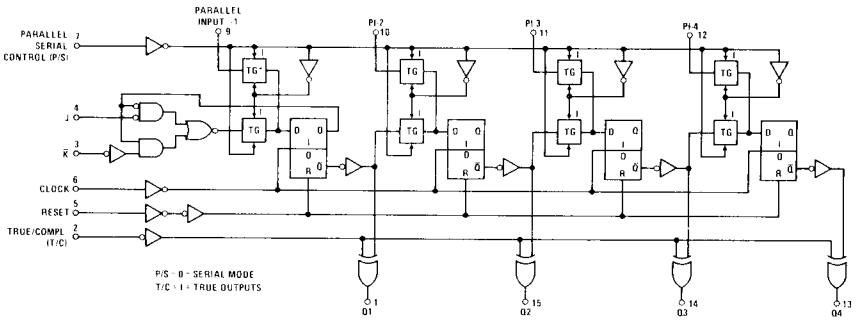
features

- Wide supply voltage range 3.0V to 15V
- 4-stage clocked shift operation
- Synchronous parallel entry on all 4 stages
- $J\overline{K}$ inputs on first stage
- Asynchronous True/Complement control on all outputs
- Reset control
- Static flip-flop operation; master/slave configuration
- Buffered outputs
- Low-power dissipation 5.0μW typ (ceramic)
- High speed to 5.0 MHz

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial controls
- Remote metering
- Computers

logic diagram



MM5215 12,288-bit read only memory

general description

The MM5215 12,288-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology and ion-implanted resistors. TRI-STATE® outputs provide wire-OR capability without loading common data lines or reducing system access times. The ROM is organized in a 1024 x 12 bit word configuration. The V_{GG} supply may be brought to 0V to reduce internal power dissipation in the non-enabled mode to 10μW/bit.

Customer programs may be submitted on Hollerith coded punched cards.

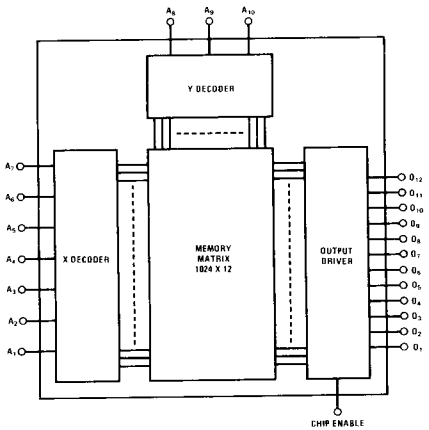
features

- Static operation
- TRI-STATE outputs
- No clocks required
- +12V and −12V supplies
- Pin compatible with E.A. 3800

applications

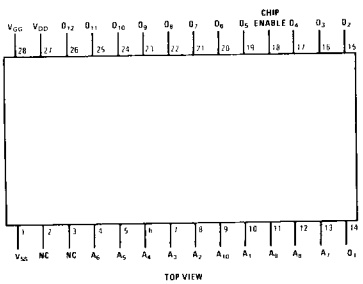
- Character generator
- Random logic synthesis
- Micro programming
- Table look-up

schematic diagram

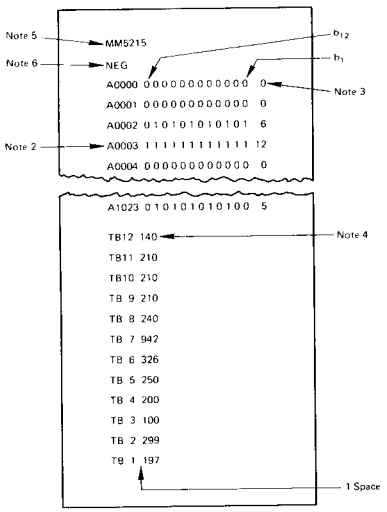


connection diagram

Dual-In-Line Package



ROM card format



Note 1: Punch three input addresses per card with the first in columns 1–25, the second in columns 26–50, and the third in columns 51–80.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

Note 5: Specify product type.

Note 6: Must type negative logic.

Note 7: NEGATIVE LOGIC ON ADDRESS AND OUTPUTS.

Note 8: "1" more negative output. "0" more positive output.

MM5311,MM5312,MM5313,MM5314, digital clocks

general description

These digital clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode devices. The devices provide all the logic required to build several types of clocks. Two display modes (four or six digits) facilitate end-product designs of varied sophistication. The circuits interface to LED and gas discharge displays with minimal additional components, and require only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking) or 24 hours. Outputs consist of multiplexed display drives ($\overline{BCD}$ and 7-segment) and digit enables. The devices operate over a power supply range of 11 to 19V and do not require a regulated supply. The MM5311 through MM5314 clocks are packaged in 24 and 28 lead dual-in-line packages.

features

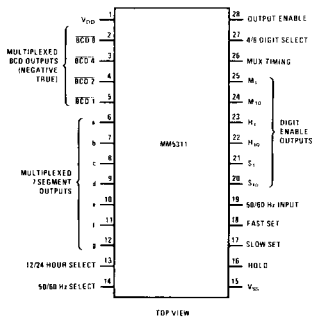
- 50 or 60 Hz operation
- 4 to 6 digit display mode
- 12 or 24 hour display format
- Leading-zero blanking (12-hour format)
- $\overline{BCD}$ and 7-segment outputs
- Single power supply
- Fast and slow set controls
- Output enable control
- Internal multiplex oscillator
- Hold count control

applications

- Desk clocks
- Automobile clocks
- Industrial clocks
- Military clocks

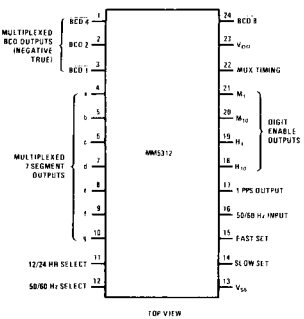
connection diagrams

Dual-In-Line Package



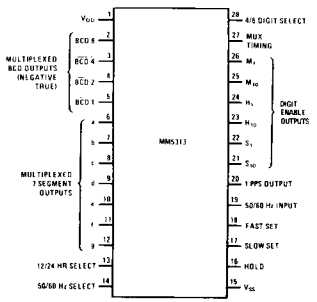
TOP VIEW

Dual-In-Line Package



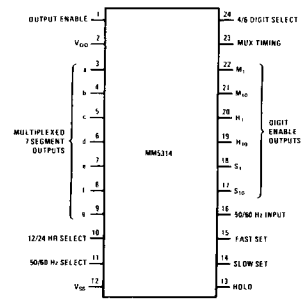
TOP VIEW

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Circle DATA UPDATE No. 269

MM5370 and MM5371 digital alarm clocks

general description

The MM5370 and MM5371 digital alarm clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. They provide all the logic required to build several types of clocks and timers. Three display modes (time, alarm and sleep) are provided to optimize circuit utility. The circuits interface simply with 7-segment gas discharge displays. The timekeeping function operates from either a 60 Hz (MM5370) or 50 Hz (MM5371) input, and the display format may be either 12 hours (with leading-zero blanking and AM/PM indication) or 24 hours. Outputs consist of display drives, alarm enable and sleep (e.g., timed radio turn-off). Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. The devices operate over a power supply range of 8.0 to 29V and do not require a regulated power supply. These clocks are packaged in 28-pin DIP.

features

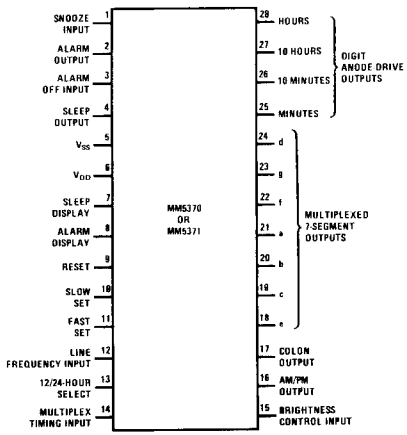
- 50 or 60 Hz operation
- Single power supply
- Low power dissipation
- 12 or 24-hour display format
- Colon drive output
- AM/PM drive output in 12-hour format
- Leading-zero blanking in 12-hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Brightness control capability
- Simple interface to gas discharge displays
- Elimination of illegal time display at turn-on
- Presettable 59-minute sleep timer
- 9-minute snooze timer

applications

- Alarm clocks
- Desk clocks
- Clock/radios
- Automobile clocks
- Industrial clocks
- Military clocks
- Appliance timers

connection diagram

Dual-In-Line Package



TOP VIEW

Circle DATA UPDATE No. 270

MM54C00/MM74C00 quad two-input NAND gate
MM54C02/MM74C02 quad two-input NOR gate
MM54C04/MM74C04 hex inverter
MM54C10/MM74C10 triple three-input NAND gate
MM54C20/MM74C20 dual four-input NAND gate

general description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

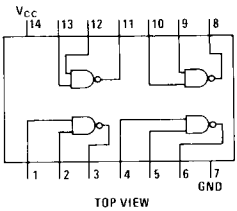
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ.
■ Low power consumption	10 nW/package typ.
■ Low power TTL compatibility	fan out of 2 driving 74L

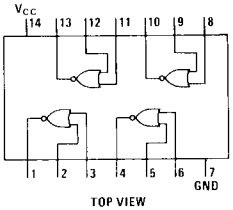
connection diagrams

MM54C00/MM74C00



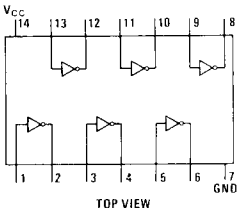
TOP VIEW

MM54C02/MM74C02



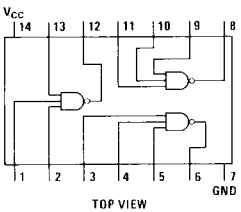
TOP VIEW

MM54C04/MM74C04



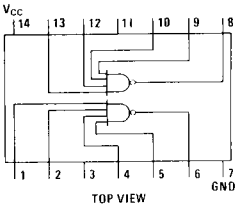
TOP VIEW

MM54C10/MM74C10



TOP VIEW

MM54C20/MM74C20



TOP VIEW

Circle DATA UPDATE No. 271

MM54C154/MM74C154 4-line to 16-line decoder/demultiplexer

general description

The MM54C154/MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

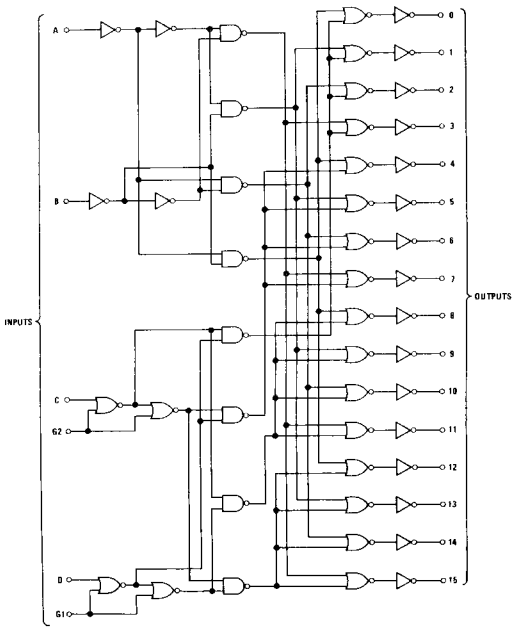
features

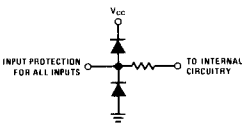
■ Supply voltage range	3.0V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise margin	1.0V guaranteed
■ High noise immunity	0.45 V_{CC} typ
■ Low power	100μW typ

applications

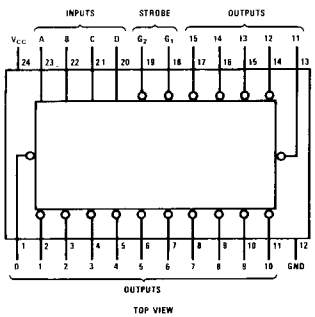
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams





Dual-In-Line Package



Circle DATA UPDATE No. 272

MM5740 90-key keyboard encoder

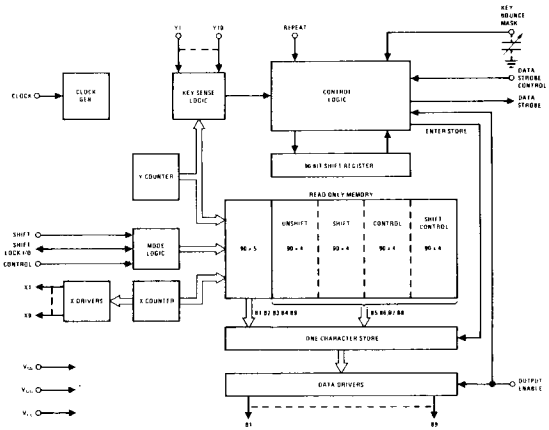
general description

The MM5740 MOS/LSI keyboard encoder is a complete keyboard interface system capable of encoding 90 single pole single throw switch closures into a usable 9-bit code. It is organized as a bit paired system and is capable of N key or two key rollover. The MM5740 is fabricated with silicon gate technology and provides for direct TTL/DTL compatibility on Data and Strobe outputs without the use of any special interface components.

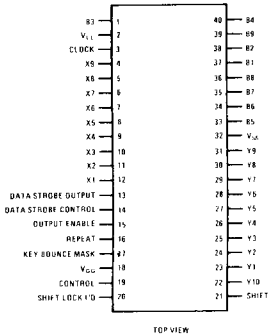
features

- TRI-STATE® data outputs directly compatible with TTL/DTL or MOS logic
- Function inputs directly compatible with TTL/DTL logic
- Only one TTL level clock required
- N key/two key rollover (mask programmable)
- 90 key-quad mode capability
- One character data storage
- Repeat function (selectable)
- Shift lock with indicator capability
- Key bounce masking by single external capacitor
- Level or pulse data strobe output
- Data strobe pulse width control

block and connection diagrams



Dual-In-Line Package



TRI-STATE is a registered trademark of National Semiconductor Corp.

Circle DATA UPDATE No. 273

MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® hex non-inverting buffers

general description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. Each of the devices are used to convert CMOS or TTL outputs to TRI-STATE® outputs with no logic inversion. The MM70C95/MM80C95 has common TRI-STATE controls for all six buffers. The MM70C97/MM80C97 has two TRI-STATE controls, one for two buffers and one for the other four.

Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

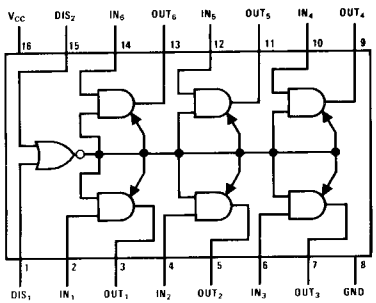
- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ)
- TTL compatible — Drive 1 TTL load

applications

- Bus drivers — typical propagation delay into a 150 pF load is 40 ns

connection diagrams

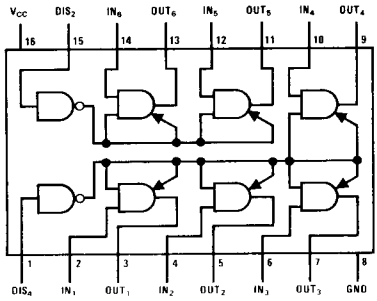
Dual-In-Line Package



TOP VIEW

MM70C95/MM80C95

Dual-In-Line Package



TOP VIEW

MM70C97/MM80C97

truth tables

MM70C95/MM80C95

DISABLE INPUT		INPUT	OUTPUT
DIS_1	DIS_2		
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

DISABLE INPUT		INPUT	OUTPUT
DIS_4	DIS_2		
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

*Output 5-6 only
**Output 1-4 only
X = Irrelevant

Circle DATA UPDATE No. 274

SEMICONDUCTOR PRODUCTS

HYBRID PRODUCTS

LX2602G/LX2603G/LX2610G/LX2620G, LX2702G/LX2703G/LX2710G/LX2720G gage LX2602D/LX2603D/LX2610D/LX2620D differential pressure transducers

general description

These rugged devices are highly accurate, completely field interchangeable, temperature compensated linear pressure transducers.

All of the basic transduction elements are incorporated in one hybrid package. A totally useful pressure transducer is shown in the block diagram below—the diaphragm and pressure references, piezoresistive sensors, signal discriminators, and signal amplifiers and processors. The first three functional elements for each input are contained in a single silicon die and the fourth is provided by standard National linear IC operational amplifiers.

The LX26XX series contains two complete absolute pressure transducers plus a comparator circuit and provides two absolute pressure outputs and a gage or differential pressure output.

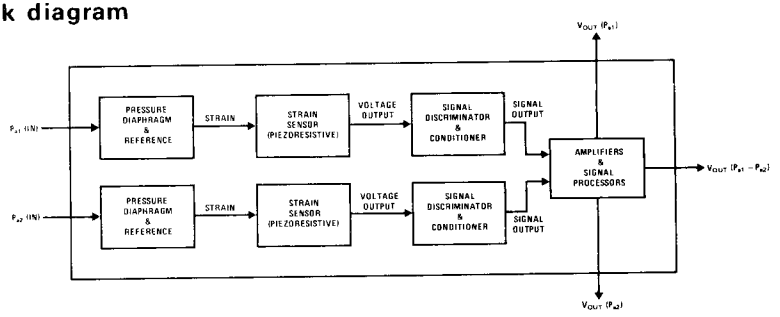
applications

- Fluid flow measurement and control
- Liquid level measurement and control
- Medical electronics
- Altimetry, air data, and meteorology
- Computer pneumatics
- Load cells and accelerometers
- Heating, ventilation, refrigeration and air conditioning controls
- Automotive emission control, safety, and diagnostic systems

features

- 10V span for very low gage and differential pressure
- Three transducers in one—two absolute pressure outputs and one gage or differential pressure output
- Field interchangeability—by using computerized laser trim all units meet one guaranteed characteristic curve.
- Accuracy—maximum calibration error band of differential ±1.5% of span
- Temperature compensated—transducer temperature effects offset by computerized laser trimming
- Flexibility—arithmetic functions, digital format and multiplexing are easily attainable because of the single ended op amp configuration
- Input overvoltage and output short circuit protection
- Low mass, no moving parts, good frequency response
- Failsafe—no fluid leakage, port to port, even in diaphragm rupture
- Available from local National distributor

block diagram



Circle DATA UPDATE No. 275

NSN66 1/8 inch 6-digit LED display

general description

The NSN66 is a six digit common cathode GaAsP LED numeric display with a nominal 1/8 inch character height. The NSN66 has one right-hand decimal point in digit number four only. Eight inputs are provided for selection of the appropriate segments and single decimal (anodes) and six inputs for digit selection (cathode). The anodes and cathodes are internally interconnected for multiplexing. Simple interface circuits may be used for TTL, DTL, or MOS operation.

The red faceplate of the display package provides excellent visual contrast and ease of visibility over a wide angle. The package is also designed to be readily incorporated into the system. Mounting holes accurately register the display location. PC board type terminals allow easy connection by wire or pin soldering or with a card-edge connector. The thin package allows significant size reduction for high density electronic equipment.

applications

- Hand held calculators
- Desk calculators
- Digital instruments
- Industrial controls
- Data terminals
- Instrumentation
- Electronic test and measurement equipment

absolute maximum ratings

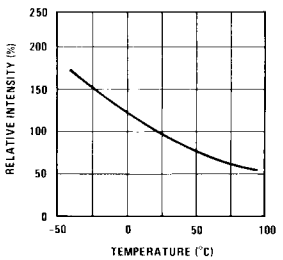
Average Current per Segment	5.0 mA
Peak Current per Segment	60 mA
Reverse Voltage	3.0V
Digit Current Pulse Width	10 ms
Operating and Storage Temperatures	−20°C to +60°C
Relative Humidity at +60°C	90%
Terminal Temperature (Soldering, 5 seconds)	230°C

electrical and optical characteristics

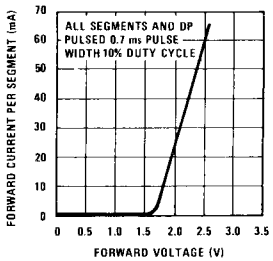
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Segment Light Intensity (Peak)	20 mA/Segm. Peak	0.1	0.4		mcd
Luminance (Brightness) of Emitting Areas (Peak)	20 mA/Segm. Peak		1600		fL
Segment Forward Voltage	5.0 mA DC		1.75	2.0	V
Intensity Matching			±33		%
Reverse Voltage	100μA/Segm.	3.0	8.0		V
Peak Wavelength			660		nm
Spectral Linewidth, Half-Intensity			25		nm
Viewing Angle, Off Axis			> ±60		degrees

typical performance characteristics (25°C)

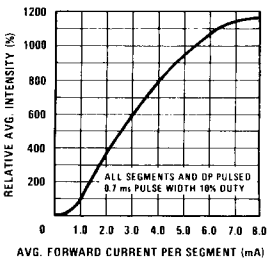
Light Intensity vs Ambient Temperature



Forward Current vs Forward Voltage



Average Light Intensity vs Average Forward Current



NSN98 1/8 inch 9 digit LED display

general description

The NSN98 is a nine digit common cathode GaAsP LED numeric display, with a nominal 1/8 inch character height. Each digit comprises seven segments with a right hand decimal point. Eight inputs are provided for selection of the appropriate segments and decimals (anodes) and nine inputs for digit (cathodes) selection. The anodes and cathodes are internally interconnected for multiplexing. Simple interface circuits may be used for TTL, DTL, or MOS operation.

The red faceplate of the display package provides excellent visual contrast and ease of visibility over a wide angle. The package is also designed to be readily incorporated into the system. Mounting holes accurately register the display location. PC board type terminals allow easy connection by wire or pin soldering or with a card-edge connector. The thin package allows significant size reduction for high density electronic equipment.

applications

- Hand held calculators
- Desk calculators
- Digital instruments
- Industrial controls
- Data terminals
- Instrumentation
- Electronic test and measurement equipment

absolute maximum ratings

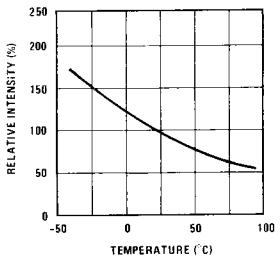
Average Current per Segment	5.0 mA
Peak Current per Segment	60 mA
Reverse Voltage	3.0V
Digit Current Pulse Width	10 ms
Operating and Storage Temperatures	−20°C to +60°C
Relative Humidity at +60°C	90%
Terminal Temperature (Soldering, 5 seconds)	230°C

electrical and optical characteristics

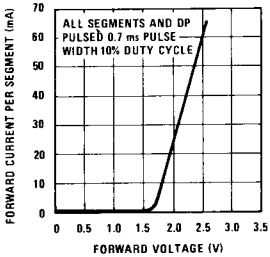
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Segment Light Intensity (Peak)	20 mA/Segm. Peak	0.1	0.4		mcd
Luminance (Brightness) of Emitting Areas (Peak)	20 mA/Segm. Peak		1600		fL
Segment Forward Voltage	5.0 mA/Segm. DC		1.75	2.0	V
Reverse Voltage	100μA/Segm.	3.0	8.0		V
Intensity Matching			±33		%
Peak Wavelength			660		nm
Spectral Linewidth, Half-Intensity			25		nm
Viewing Angle, Off Axis			>±60		degrees

typical performance characteristics (25°C)

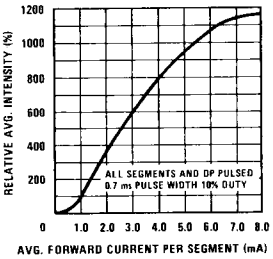
Light Intensity vs Ambient Temperature



Forward Current vs Forward Voltage



Average Light Intensity vs Average Forward Current



Circle DATA UPDATE No. 277

The following application literature and product selection guides are also available. Circle the appropriate DATA UPDATE number on your request card.

APPLICATION NOTES AND BRIEFS

AN-83 DATA BUS AND DIFFERENTIAL LINE DRIVERS AND RECEIVERS

Bring yourself up to date on National's data line drivers, transceivers and receivers. This note describes new unified and TRI-STATE® data bus devices and how they help solve common data-transmission problems. The note further discusses true differential transmission lines and their termination, and maximum line lengths and frequencies.

circle update No. 278

AN-86 A SIMPLE POWER SAVING TECHNIQUE FOR THE MM5262 2k RAM

Decoding the clocks of unselected MM5262 chips in a memory array significantly reduces the power consumption of the array. This note discusses a method to implement such a power-saving technique in an example 8-k word x 16-bits/word memory module.

circle update No. 279

AN-89 HOW TO DESIGN WITH PROGRAMMABLE LOGIC ARRAYS

Programmable logic arrays (PLAs) produce a known output function from a given input function. Since the number of inputs to the PLA can be many more than is possible with an ordinary rectangularly-structured ROM, PLAs simplify logic designs and save logic costs. This note discusses the structure of PLAs, tells you how to design with them and describes several PLA applications.

circle update No. 280

AN-90 54C/74C FAMILY CHARACTERISTICS

Here are the basic characteristics common to all members of the 54C/74C family: output voltage-current characteristics; noise immunity and noise margin performance; power consumption; propagation delay (speed); and temperature characteristics.

circle update No. 281

AN-91 THE LX1602A PRESSURE TRANSDUCER AND ALTIMETER APPLICATIONS

A small, low-cost LX1602A pressure transducer plus some extra circuitry lets you add complete altitude reporting capability to a transponder. The altimeter operates between altitudes of −1000 and +50,000 feet.

circle update No. 282

AN-92 INSTALLATION IDEAS FOR PRESSURE TRANSDUCERS

Here is a collection of helpful and practical ideas for mounting NSC's pressure transducers for various applications; it is oriented to the LX1600 and LX1700-series transducers.

circle update No. 283

AN-93 TRANSDUCERS IN FLUID FLOW APPLICATIONS

The three basic classes of transducer use are called pressure vessel, open flow and closed flow applications. This note thoroughly describes each of these use categories and derives the key equations for each, in terms suitable to electrical-engineer users of the transducers.

circle update No. 284

APPLICATIONS LITERATURE

AN-94 LX SERIES PRESSURE TRANSDUCERS: DESIGN AND APPLICATIONS INFORMATION

A description, in detail, of the construction and method of operation of National's LX-series of pressure transducers, plus several unique application examples of their use.

circle update No. 285

AN-95 PRESSURE TRANSDUCER LOAD CELL

Here's an interesting discussion of the fundamentals of using NSC's pressure transducers in load/weight measurement and control systems.

circle update No. 286

AN-96 PRESSURE TRANSDUCERS AS ACCELEROMETERS

This note examines and classifies accelerometer uses, and defines areas of such usage appropriate to pressure transducers. It also describes the fundamentals of using NSC's pressure transducers as accelerometers.

circle update No. 287

LINEAR BRIEF-21 INSTRUMENTATIONAL AMPLIFIERS

A single-op-amp instrumentation amplifier is described that compares favorably with multiple-op-amp designs. This wideband-circuit's high performance does not depend on resistor matching, and the design allows a single resistor to set the gain.

circle update No. 288

LINEAR BRIEF-22 LOW DRIFT AMPLIFIERS

This brief describes the many sources of drift error in (otherwise) very-low-drift amplifiers, and presents a simple circuit for drift measurement.

circle update No. 289

LINEAR BRIEF-23 PRECISE TRI-WAVE GENERATION

The triangle wave generator has become a popular circuit and is now widely used. This article describes such a generator, one that is useful to 200kHz, and features easy and accurate control of peak-to-peak amplitude, output frequency and symmetry.

circle update No. 290

LINEAR BRIEF-24 VERSATILE IC PREAMP MAKES THERMOCOUPLE AMPLIFIER WITH COLD JUNCTION COMPENSATION

Here is a thermocouple amplifier circuit that provides a direct-reading output of 10mV/°C, automatically compensates for reference-junction temperature changes and allows simple calibration.

circle update No. 291

LINEAR BRIEF-25 TRUE RMS DETECTOR

Basically a precision absolute-value circuit connected to a one-quadrant multiplier/divider, the design described here provides a dc output equal to the true-rms value of the input, regardless of the input's waveform. Typical accuracy is 2% for 20Vp-p inputs from 50Hz to 100kHz. (The circuit is usable, however, to 500kHz.)

circle update No. 292

TRANSDUCER BRIEF-1 THE MULTI-LEVEL SWITCH LX SERIES PRESSURE TRANSDUCER KIT PART NO. SK1007

All NSC LX-series pressure transducers provide a high-level analog output. The circuit described here uses any LX-series transducer plus additional circuitry to produce not only the standard analog output, but also three independent switch points (high, mid-range, and low).

circle update No. 293

TRANSDUCER BRIEF-2 TRANSDUCER ZERO-BASED OUTPUT OPTION

Using positive and negative power supplies, you can convert the standard 2.5V to 12.5V output range of any of NSC's LX-series pressure transducers to a range of 0–10V.

circle update No. 294

TRANSDUCER BRIEF-3 TRANSDUCER SENSOR DIAPHRAGM 15 MILLION CYCLE LIFE TEST

Derating the theoretical life curve for the thin silicon membrane sensing element to a safe design level predicts a life of at least 40 million cycles. Actual testing of 20 LX1600As from vacuum (1 psia) to 1 atm. at a rate of three cycles per minute produced no failures after a cum test of 15-million unit cycles.

circle update No. 295

TRANSDUCER BRIEF-4
THE PRESSURE TO CURRENT TRANSLATOR
LX SERIES PRESSURE TRANSDUCER KIT PART NO. SK1008

This circuit outputs a 4 to 20mA current that is proportional to the input pressure, and operates with any LX-series transducer. The load may be remotely located: for example, a 100Ω meter movement located 15 miles from the transducer/translator and connected with 19 AWG wire provides the same resolution as if it were mounted on the unit itself. Remote current sensing with low resistances also offers high-noise-immunity performance.

circle update No. 296

TRANSDUCER BRIEF-5
ADJUSTING THE OPERATING CHARACTERISTICS OF
LX16 SERIES AND LX17 SERIES PRESSURE TRANSDUCERS

NSC's standard LX16 and LX17-series pressure transducers have standardized curves. And on these curves, the 2.5V and 12.5V output points represent the minimum and maximum pressure inputs, respectively; this is true throughout the range of 0–300 psi. This brief tells you how to change the end points of the curve without affecting the slope of the curve.

circle update No. 297

TRANSDUCER BRIEF-6
THREE TRANSDUCERS IN ONE . . . THE LX26XX SERIES

Here's a brief description of some conventional, some complex and some highly innovative applications of National's newest and most unique pressure transducers, the LX26XX series. Each of these transducers consists of two independent absolute-pressure units, signal-processed to yield three outputs: the absolute pressure at each input port, and the port-to-port differential input pressure.

circle update No. 298

TRANSDUCER BRIEF-7
USE OF THE SK1007 PRESSURE TRANSDUCER KIT IN VAULT ALARM SYSTEMS

A ventilation system is required in all currently installed, larger safes and vaults. It is possible to develop a pressure differential between the interior of the vault and the surrounding ambient. This differential drops when the vault door is opened. Thus, a pressure transducer that monitors the differential pressure can become part of an accurate, reliable alarm system. The basic concept is extendable to other applications, as well.

circle update No. 299

TRANSDUCER BRIEF-8
TRANSDUCER FLUID FILLED OPTION

Protecting transducers from hostile media and/or insulating the media against electric shock from transducers is an old industrial problem. National has solved this problem for its pressure transducers by using a silicone protecting membrane and a silicone oil fill to provide device/media isolation.

circle update No. 300

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