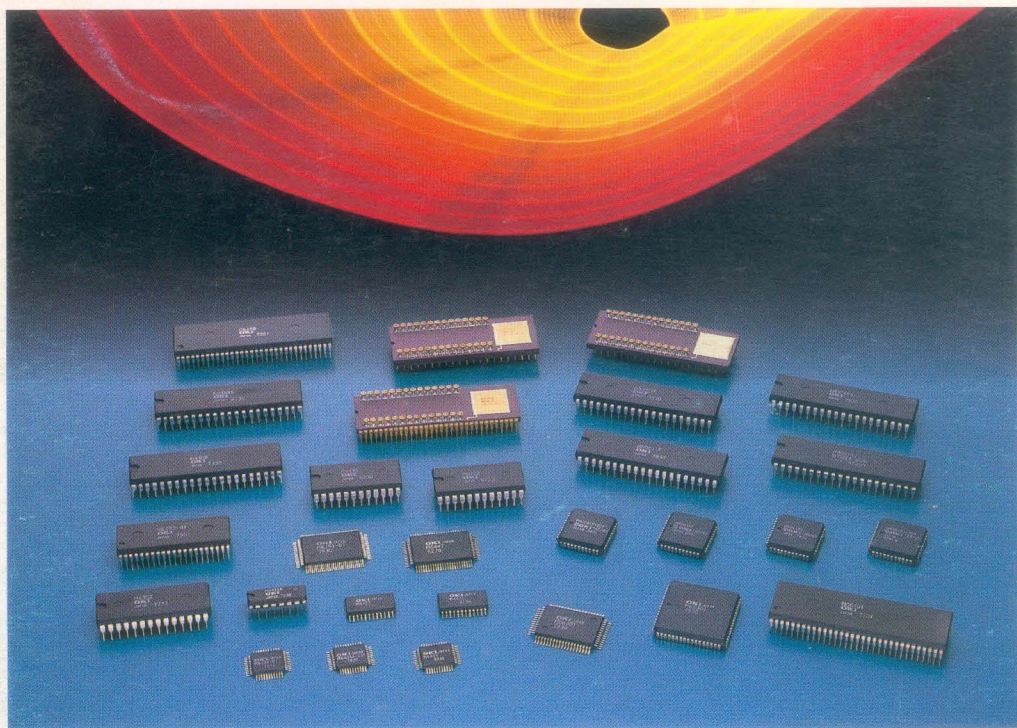


DATA BOOK

OKI

MICROCONTROLLER



THIRD EDITION
ISSUE DATE: MAR 1988

PREFACE

A high technology company with an aggressive approach to innovation, OKI has been supplying single-chip microcontrollers since 1975. OKI's single-chip microcontrollers find wide application in various types of electronic equipment in the consumer and the industrial fields. Our products have been enjoying a good reputation for their high quality and high performance. The most outstanding feature employed in all of OKI's microcontrollers is CMOS technology which ensures low power operation.

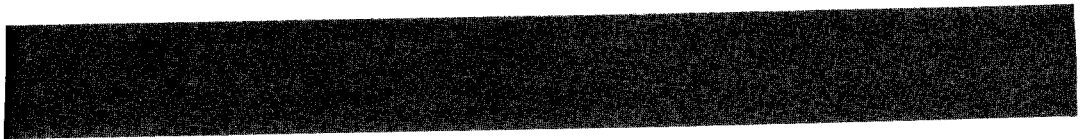
OKI will continue to enhance the its microcontroller series and program development systems to cater to cutomers' requirements.

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PROGRAM DEVELOPMENT SYSTEMS



PROGRAM DEVELOPMENT SYSTEMS FOR OKI MICROCONTROLLERS

OLMS-40 SERIES

target chip	development tool package name	standard software (included in package)	adaptor module (if necessary)	field debugging tool
MSM5840	EASE 40 (SERIAL INTERFACE) (BUS INTERFACE)	DB400 debugger ASM40 cross assembler	—	MPB202
MSM5842			MPB421	
MSM58421			MPB422	
MSM58422			—	—
MSM5847	dedicated hardware simulator			

[Note]

- The standard software DB400 and ASM40 are available on CP/M-80 for most personal computers, or ISIS-II for INTEL MDS.
- CP/M is a registered trade mark of Digital Research, and ISIS-II, MDS of Intel.

LOW POWER SERIES

target chip	development tool package name	standard software	
MSM5052	EASE5052/56	EASE host monitor	ASM50 cross assembler
MSM5056			
MSM5054	EASE5054/55		
MSM5055			
MSM6051	(EASE6051)		
MSM6351	(EASE6351/6353)		
MSM6353			
MSM6052	EASE6052, (EASE6352/6052)		
MSM6352	(EASE6352/6052)		

[Note]

- The standard software is available under following operating system.
CP/M-80 for most of personal computers
MSDOS for OKI if800, NEC PC9801 etc.
PCDOS for IBM PC-XT, AT, IBM 5550

OLMS-64 SERIES

target chip	development tool package name	I/O adaptor module	standard software (included in package)	field debugging tool	Piggy back
MSM6404	EASE6400	-	EASE host monitor	-	MSM6404VS
MSM6408		-		(ASM6408)*	
MSM6402		-		ASM6400	
MSM6422		PAM6422		PEM6422	
MSM6411		PAM6411		PEM6411	
MSM6442		PAM6442		PEM6442	
MSC6458	EASE6458	-	ASM6458	-	MSC6458VS

[Note] The standard software is available under following operating system.

EASE, ASM6400, ASM6458 CP/M-80 for most personal computers,
 MSDOS for OKI if800, NEC PC9801 etc.
 PCDOS for IBM PC-XT, AT, IBM 5550

* ASM6408 CP/M-80 version.
 ASM6400 Covers MSDOS and PCDOS for MSM6408.

OLMS-65 SERIES

target chip	development tool package name	standard software (included in package)	field debugging tool
MSM6502/6512	EASE6502	EASE65 ASM6502	MPB6502EVA

[Note] The standard software is available under CP/M-80, MSDOS, or PCDOS.

8 BIT SERIES (INTEL compatible)

target chip	development tool	standard software	optional software	piggy back
MSM80C48	EASE80C49	EASE49 ASM49	-	-
MSM80C49				
MSM80C50				
MSM80C51F	EASE80C51mKII	EASE	See Note 1.	MSM85C154VS
MSM83C154		ASM51		

[Note]

- Optional Software for MSM80C51/83C154
 PASM preprocessor, MAC51 relocatable assembler, RL51 object linker, LIB51 librarian SID51 symbolic debugger
- The softwares are available under following operating system.
 EASE49 CP/M-80, ISIS-II
 ASM49 CP/M-80, ISIS-II
 EASE & ASM51 CP/M-80 for OKI if 800, NEC PC8801 etc.
 MSDOS for OKI if800, NEC PC9801 etc.
 PCDOS for IBM PC-XT, AT, IBM 5550

 PASM, MAC51, RL51, LIB51 MSDOS for OKI if80, NEC PC9801 etc.
 SID51 PCDOS for IBM PC-XT, AT, IBM 5550

8 BIT SERIES (OKI original)

target chip	development tool package name	standard software (included in package)	optional software
MSM66301	EASE66301	ASM66301 EASE	See Note 1.
MSM62580	EASE62580	AS62580 EASE	

[Note]

- Optional Software for MSM66301
 c-compiler (VMS for uVAX-II)
 relocatable assembler (VMS)
 object linker and librarian (VMS)
 cc66 debugger (VMS)
 symbolic debugger (VMS)

* under development
 "
 "
 "
 "

LINE-UP AND TYPICAL CHARACTERISTICS



● OLMS-40 SERIES

TYPE NO.	PROCESS	POWER SUPPLY VOLTAGE	CLOCK FREQUENCY	ROM (BIT)	RAM (BIT)	INPUT PORT	OUTPUT PORT	I/O PORT	TIMER COUNTER	INTER-RUPT	STACK	INSTRUC-TION	MACHINE CYCLE	POWER CONSUMPTION		PACKAGE	REMARKS
														ACTIVE	STAND-BY		
MSM5840	CMOS	5V	4.2MHz	2048 x 8	128 x 4	6	16	8	8 Bit R/W	2	4	98	7.6μS	1.6mA	—	42DIP/44FLAT	
MSM5842	CMOS	5V	4.2MHz	768 x 8	32 x 4	5	8	8	8 Bit	—	1	52	7.6μS	1.5mA	—	28DIP/32FLAT	
MSM5841	CMOS	5V	4.2MHz	1536 x 8	40 x 4	5	3LCD Seg, 5LCD Seg, or LOGIC	8	12 Bit	—	1	52	7.6μS	2.0mA	—	60FLAT	
MSM5842	CMOS	5V	4.2MHz	1536 x 8	40 x 4	5	7 x 5 FLT Seg, 5 Discrete	8	12 Bit	—	1	52	7.6μS	2.0mA	—	60FLAT	
MSM5847	CMOS	3V	32kHz	1536 x 8	96 x 4	—	24 x 3LCD Seg.	7	13 Bit	—	2	43	610μS	50μA	—	44FLAT/CHIP	

● OLMS-50/60 SERIES

TYPE NO.	PROCESS	POWER SUPPLY VOLTAGE	CLOCK FREQUENCY	ROM (BIT)	RAM (BIT)	INPUT PORT	OUTPUT PORT	I/O PORT	TIMER COUNTER	INTER-RUPT	STACK	INSTRUC-TION	MACHINE CYCLE	POWER CONSUMPTION		PACKAGE	REMARKS
														ACTIVE	STAND-BY		
MSM5052	CMOS	1.5V	32kHz	1280 x 14	62 x 4	8	26 x 2LCD Seg, 5 LOGIC	—	—	—	—	42	122μS	3μA	—	CHIP	Built-in temperature detector
MSM5054	CMOS	1.5V/3V	32kHz	1024 x 14	62 x 4	6	44 x 2LCD Seg.	—	—	—	—	40	122μS	3μA	—	CHIP	
MSM5055	CMOS	1.5V/3V	32kHz	1792 x 14	96 x 4	8	60 x 2LCD Seg, 4 LOGIC	—	—	—	—	42	122μS	3μA	—	CHIP	VOICE CONTROLLER
MSM5056	CMOS	1.5V	32kHz	1792 x 14	90 x 4	4	38 x 2LCD Seg, 4 LOGIC	—	—	—	—	42	122μS	3μA	—	CHIP	Connection with solar cell available
MSM6051	CMOS	1.5V/3V	32kHz	2560 x 14	120 x 4	9	63 x 3LCD Seg, 4 LOGIC	—	—	1	2	59	91.5μS	3μA	—	CHIP	
MSM6351	CMOS	1.5V/3V	32kHz	4096 x 15	1024 x 4	—	59 x 3LCD Seg, or 58 x 4LCD Seg.	20	—	3	7	65	61.0μS	3μA	—	CHIP/100FLAT	
MSM6353	CMOS	1.5V/3V	32kHz	4096 x 15	1024 x 4	—	—	20	—	3	7	60.0μA	3μA	—	CHIP/42PINS DIP		
MSM6052	CMOS	3V	3.58MHz	2048 x 14	640 x 4	12	12	4	4 Bit	1	5	52	17.9μS	1.2mA	0.2μA	28DIP/40DIP/44FLAT	Built-in DTMF
MSM6352	CMOS	3V	3.58MHz	2048 x 14	640 x 4	12	12	4	4 Bit	2	5	52	17.9μS	1.8mA	0.2μA	28DIP/40DIP/44FLAT	Built-in DTMF on-hook dialing

2

● OLMS-64 SERIES

TYPE NO.	PROCESS	POWER SUPPLY VOLTAGE	CLOCK FREQUENCY	ROM (BIT)	RAM (BIT)	INPUT PORT	OUTPUT PORT	I/O PORT	TIMER COUNTER	INTER-RUPT	STACK	INSTRUC-TION	MACHINE CYCLE	POWER CONSUMPTION ACTIVE	POWER CONSUMPTION STAND-BY	PACKAGE	REMARKS
MSM6404	CMOS	5V	4.2MHz	4000 × 8	256 × 4	4	—	32	12 Bit R/W 12 Bit R/W 8 bit R/W	5	32	121	952nS	6mA	1 μ A	42DIP/44FLAT	
MSM6408	CMOS	5V	4.0MHz	8096 × 8	256 × 4	4	—	32	12 Bit R/W 12 Bit R/W 8 Bit R/W	5	32	121	1 μ S	6mA	1 μ A	42DIP/44FLAT	
MSM6411	CMOS	5V	4.2MHz	1024 × 8	32 × 4	4	—	8	—	2	8	63	952nS	6mA	1 μ A	16DIP/24FLAT	
MSM6422	CMOS	5V	4.2MHz	2048 × 8	64 × 4	1	—	18	12 Bit	2	16	63	952nS	6mA	1 μ A	16DIP/24FLAT	
MSM6442	CMOS	5V	4.2MHz	2048 × 8	128 × 4	1	46 × 2LCD Seg	16	8 Bit R/W	4	16	76	952nS	6mA	1 μ A	80FLAT	Built-in LCD Con-troller/Driver
MSC6458	Bi CMOS	5V	4.3MHz	6192 × 8	512 × 4	9	12 × 12FLT Seg	24	12 Bit R/W 16 Bit R/W 8 Bit R/W	8	32	147	930nS	9mA	1 μ A	64 Shrink DIP/ 64 FLAT	Built-in FLT Con-troller/Driver

● OLMS-65 SERIES

TYPE NO.	PROCESS	POWER SUPPLY VOLTAGE	CLOCK FREQUENCY	ROM (BIT)	RAM (BIT)	INPUT PORT	OUTPUT PORT	I/O PORT	TIMER COUNTER	INTER-RUPT	STACK	INSTRUC-TION	MACHINE CYCLE	POWER CONSUMPTION ACTIVE	POWER CONSUMPTION STAND-BY	PACKAGE	REMARKS
MSM6502	CMOS	3V	32kHz	2000 × 8	128 × 4	4	108LCD Seg	8	12 Bit	3	32	68	91.5 μ S	45 μ A	30 μ A	44FLAT-CHIP	
MSM6512	CMOS	3V	32kHz	2000 × 8	128 × 4	4	108LCD Seg	8	12 Bit	3	32	68	91.5 μ S	30 μ A	12 μ A	44FLAT-CHIP	

● 8 Bit SERIES (INTEL compatible)

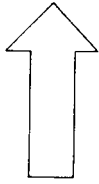
TYPE NO	PROCESS	POWER SUPPLY VOLTAGE	CLOCK FREQUENCY	ROM (KBIT)	RAM (KBIT)	INPUT PORT	OUTPUT PORT	IO PORT	TIMER COUNTER	INTER- RUPT	STACK	INSTRUC- TION	MACHINE CYCLE	POWER CONSUMPTION		PACKAGE	REMARKS
														ACTIVE	STAND-BY		
MSM80C35	CMOS	5V	1MHz	—	64 × 8	—	—	24	8 Bit R/W	2	8	111	1.36μS	10mA	1μA	40DIP/44FLAT	
MSM80C39	CMOS	5V	1MHz	—	128 × 8	—	—	24	8 Bit R/W	2	8	111	1.36μS	10mA	1μA	40DIP/44FLAT	
MSM80C40	CMOS	5V	6MHz	—	256 × 8	—	—	24	8 Bit R/W	2	8	111	2.5μS	10mA	1μA	40DIP/44FLAT	
MSM80C31F	CMOS	5V	16MHz	—	128 × 8	—	—	32	16 Bit R/W × 2	5	64	111	0.75μS	20mA	1μA	40DIP/44FLAT/44PLCC	
MSM80C154	CMOS	5V	16MHz	—	256 × 8	—	—	32	16 Bit R/W × 3	6	128	111	0.75μS	20mA	1μA	40DIP/44FLAT/44PLCC	
MSM80C48	CMOS	5V	1MHz	1024 × 8	64 × 8	—	—	24	8 Bit R/W	2	8	111	1.36μS	10mA	1μA	40DIP/44FLAT	
MSM80C49	CMOS	5V	1MHz	2048 × 8	128 × 8	—	—	34	8 Bit R/W	2	8	111	1.36μS	10mA	1μA	40DIP/44FLAT	
MSM80C50	CMOS	5V	6MHz	4096 × 8	256 × 8	—	—	24	8 Bit R/W	2	8	111	2.5μS	10mA	1μA	40DIP/44FLAT	
MSM80C51F	CMOS	5V	16MHz	4096 × 8	128 × 8	—	—	32	16 Bit R/W × 2	5	64	111	0.75μS	20mA	1μA	40DIP/44FLAT/44PLCC	
MSM83C154	CMOS	5V	16MHz	16384 × 8	256 × 8	—	—	32	15 Bit R/W × 3	6	128	111	0.75μS	20mA	1μA	40DIP/44FLAT/44PLCC	

● 8 BIT SERIES (OKI original)

TYPE NO	PROCESS	POWER SUPPLY VOLTAGE	CLOCK FREQUENCY	ROM (KBIT)	RAM (KBIT)	INPUT PORT	OUTPUT PORT	IO PORT	TIMER COUNTER	INTER- RUPT	STACK	INSTRUC- TION	MACHINE CYCLE	POWER CONSUMPTION		PACKAGE	REMARKS
														ACTIVE	STAND-BY		
MSM86580	CMOS	5V	5MHz	3072 × 8	128 × 8	—	—	1	—	—	32	95	800ns	4mA	10μA	C.O.B	For IC cards under development
MSM86581	CMOS	5V	16MHz	16384 × 8	256 × 8	8	—	40	16 Bit × 4	17	256	99	400ns	—	—	C.O.B	Under development (PGB type) • V.DC 8ch, 10bit • UART • PWM • Character register

● LINE-UP AND TYPICAL CHARACTERISTICS ●

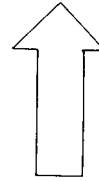
LOW POWER



OLM-50/60 SERIES

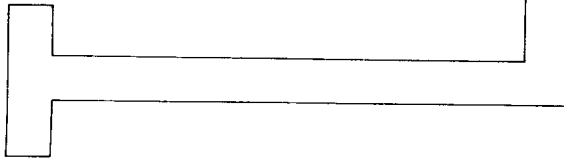
TYPE NO	ROM	RAM	POWER CONSUMPTION	FEATURES
MSM5052	1280 x 14	62 x 4	3 μ A	52 Seg. LCD Driver
MSM5054	1024 x 14	62 x 4	3 μ A	88 Seg. LCD Driver
MSM5055	1792 x 14	96 x 4	3 μ A	120 Seg. LCD Driver
MSM5056	1792 x 14	90 x 4	3 μ A	76 Seg. LCD Driver
MSM6051	2560 x 14	120 x 4	3 μ A	189 Seg. LCD Driver
MSM6052 6352	2048 x 14	640 x 4	1.2mA 1.8mA	DTMF Generator
MSM6351	4096 x 15	1024 x 4	3 μ A	232 Seg. LCD Driver
MSM6353	4096 x 15	1024 x 4	3 μ A	Serial board (Synchronised/ Non synchronised)

HIGH SPEED



OLM-64 SERIES

TYPE NO	ROM	RAM	MACHINE CYCLE	FEATURES
MSM6404	4000 x 8	256 x 4	952nS	I/O: 36
MSM6408	8096 x 8	256 x 4	952nS	I/O: 36
MSM6411	1024 x 8	32 x 4	952nS	I/O: 11
MSM6422	2048 x 8	64 x 4	952nS	I/O: 19
MSM6442	2048 x 8	128 x 4	952nS	92 Seg. LCD Driver
MSM6458	8192 x 8	512 x 4	930nS	144 Seg. FLT Driver



OLM-40/65 SERIES

TYPE NO	ROM	RAM	MACHINE CYCLE	FEATURES
MSM5840	2048 x 8	128 x 4	7.6 μ S	I/O: 30
MSM5842	768 x 8	32 x 4	7.6 μ S	I/O: 21
MSM58421	1536 x 8	40 x 4	7.6 μ S	35 Seg. LCD Driver
MSM58422	1536 x 8	40 x 4	7.6 μ S	35 Seg. FLT Driver
MSM5847	1536 x 8	96 x 4	600 μ S	72 Seg. LCD Driver
MSM6502	2000 x 8	128 x 4	91.5 μ S	108 Seg. LCD Driver
MSM6512	2000 x 8	128 x 4	91.5 μ S	104 Seg. LCD Driver

IC CARD



ONE CHIP MICROCOMPUTER FOR IC CARD

TYPE NO	ROM	RAM	MACHINE CYCLE	FEATURES
MSM62580	3072 x 8	128 x 8	800nS	Built-in EEPROM 2048 x 8

4BIT

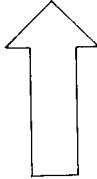
8BIT



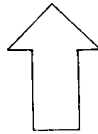
OKI ONE CHIP

2

HIGH PERFORMANCE



**HIGH PERFORMANCE
nX SERIES**



MSM80C154 SERIES

TYPE NO	ROM	RAM	MACHINE CYCLE
MSM83C154	16384 x 8	256 x 8	750nS
MSM80C154	—	256 x 8	750nS

OLMS-66K SERIES

TYPE NO	ROM	RAM	MACHINE CYCLE
MSM66301*	16384 x 8	512 x 8	400nS

16BIT

MSM80C51 SERIES

TYPE NO	ROM	RAM	MACHINE CYCLE
MSM80C51/51F	4096 x 8	128 x 8	0.75μS
MSM80C31/31F	—	128 x 8	0.75μS

MSM80C48 SERIES

TYPE NO.	ROM	RAM	MACHINE CYCLE
MSM80C48	1024 x 8	64 x 8	1.36μS
MSM80C49	2048 x 8	128 x 8	1.36μS
MSM80C50	4096 x 8	256 x 8	2.5μS
MSM80C35	—	64 x 8	1.36μS
MSM80C39	—	128 x 8	1.36μS
MSM80C40	—	256 x 8	2.5μS

8BIT

CODE ENTRY



CODE ENTRY

The program code ENTERING method is outlined below.

1. USABLE MEDIA

- (1) 2 pieces of same type EPROMs containing identical DATA

EPROM specification

- 2716
- 2732
- 27C32
- 27C32A
- 2764
- 27C64
- 27128
- 27256

- (2) 1 copy of object machine code list

2. SINGLE CHIP MICROCONTROLLER DEVELOPMENT STAGES

3

USER 1

- Program with OKI development tool.



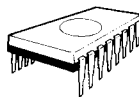
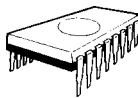
if 800



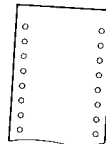
TOOL

USER 2

- Prepare 2 pcs of EPROM and programming list



EPROM



Printout

OKI 3

- Print out identical EPROM data.



OKI 4

- Engineering Sample
Actual production sample of your microcontroller chip prepared for final approval.



OKI 5

- Volume production of single chip microcontrollers.

USER 6

START
PRODUCT/SYSTEM
MANUFACTURE

PACKAGING



PACKAGING

	PACKAGE/PIN COUNT		
	DIP	FLAT	PLCC
MSM5840	42 PIN	44 PIN	-
MSM5842	28 PIN	32 PIN	-
MSM58421	-	60 PIN	-
MSM58422	-	60 PIN	-
MSM5847 *	-	44 PIN	-
MSM5052 *	-	56 PIN	-
MSM5054 *	-	56 PIN	-
MSM5055 *	-	80 PIN	-
MSM5056 *	-	-	-
MSM6051 *	-	-	-
MSM6351 *	-	100 PIN	-
MSM6052	28/40 PIN	44 PIN	-
MSM6352	28/40 PIN	44 PIN	-
MSM6404	42 PIN	44 PIN	44 PIN
MSM6404VS	42 PIN PIGGY BACK	-	-
MSM6408	42 PIN	44 PIN	44 PIN
MSM6411	16 PIN	24 PIN	-
MSM6422	24 PIN	24 PIN	-
MSM6442	-	80 PIN	-
MSC6458	64 PIN SHRINK	64 PIN	68 PIN
MSC6458VS	64 PIN SHRINK PIGGY BACK	-	-

NOTE: * CHIP TYPE is available.

4

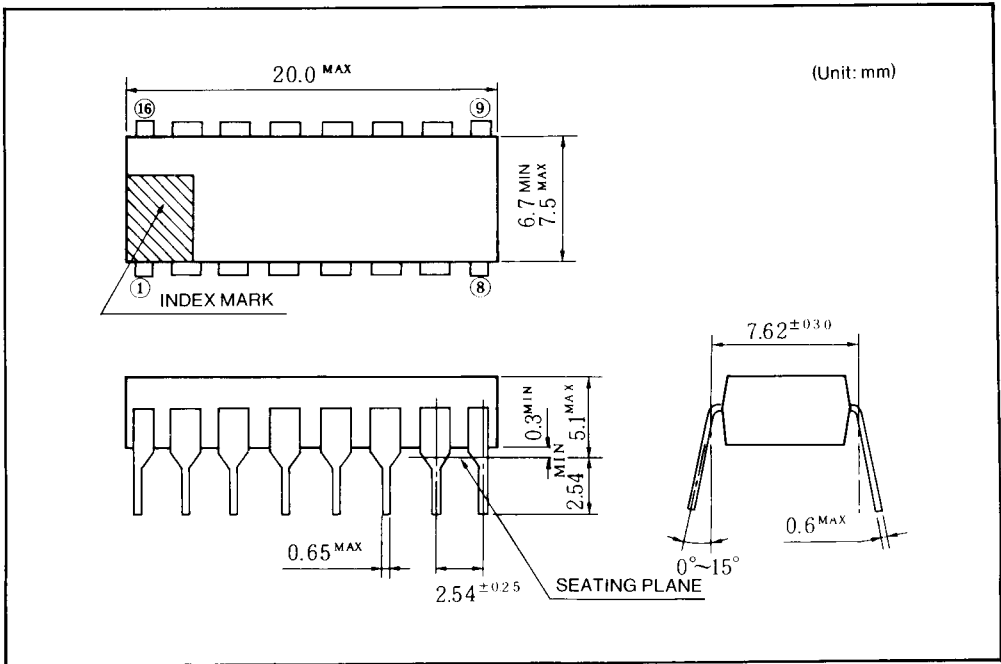
● PACKAGING ●

	PACKAGE/PIN COUNT		
	DIP	FLAT	PLCC
MSM6502*	-	56 PIN(S)	-
MSM6512*	-	56 PIN(S)	-
MSM62580	-	COB (5PIN)	-
MSM66301	64 PIN SHRINK	64 PIN	68 PIN
MSM80C35	40 PIN	44 PIN	44 PIN
MSM80C39	40 PIN	44 PIN	44 PIN
MSM80C40	40 PIN	44 PIN	44 PIN
MSM80C31	40 PIN	44 PIN	44 PIN
MSM80C48	40 PIN	44 PIN	44 PIN
MSM80C49	40 PIN	44 PIN	44 PIN
MSM80C50	40 PIN	44 PIN	44 PIN
MSM80C31F	40 PIN	44 PIN	44 PIN
MSM80C51FVS	40 PIN PIGGY BACK	-	-
MSM80C51F	40 PIN	44 PIN	44 PIN
MSM80C154	40 PIN	44 PIN	44 PIN
MSM83C154	40 PIN	44 PIN	44 PIN
MSM85C154VS	40 PIN PIGGY BACK	-	-

NOTE: (S) means Small package

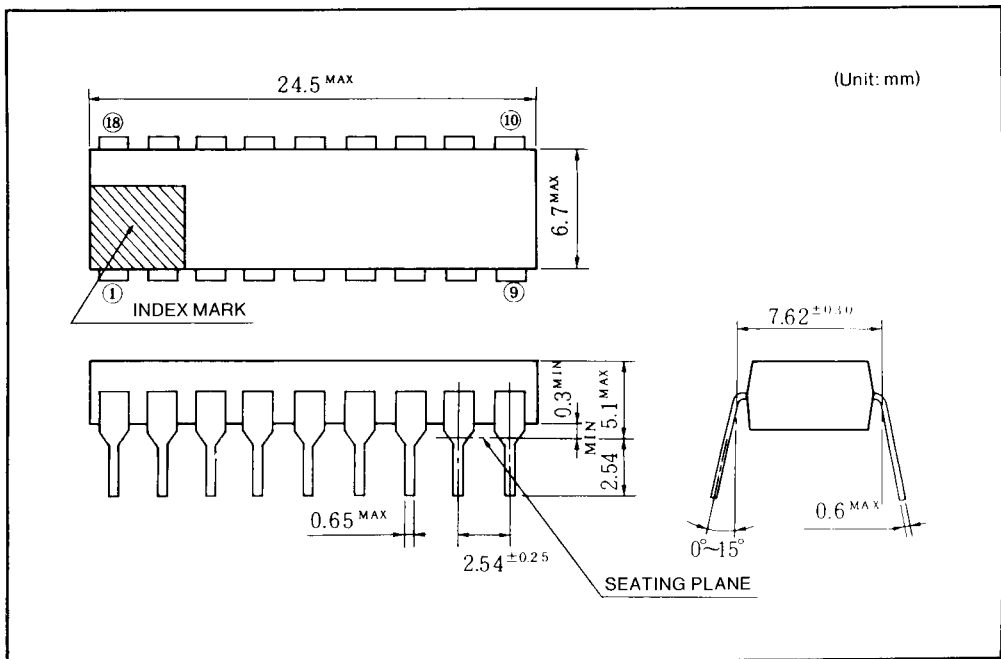
4

• 16 PIN PLASTIC DIP



4

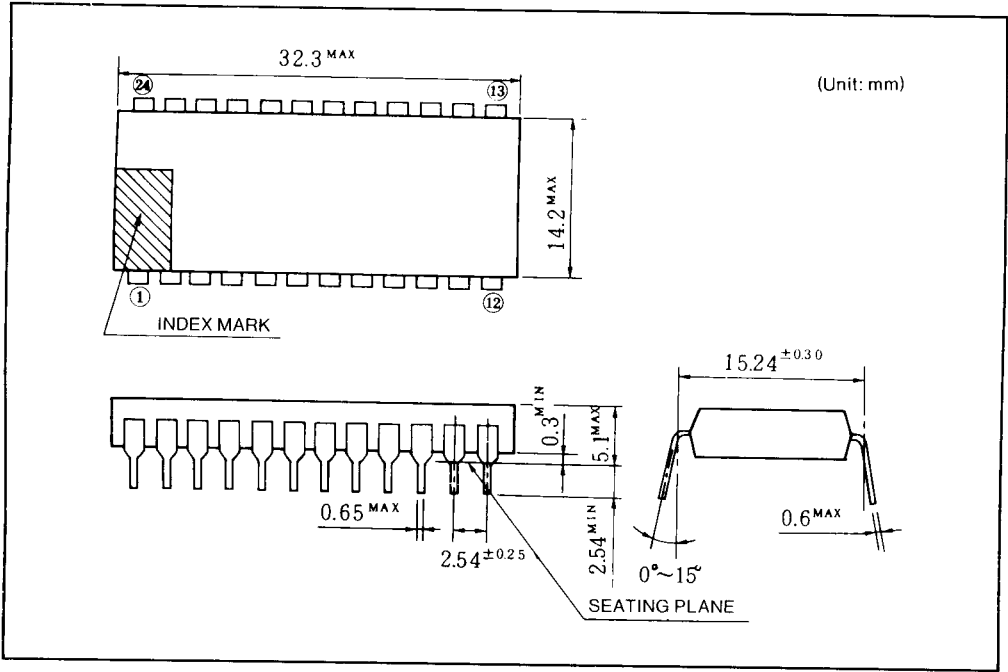
• 18 PIN PLASTIC DIP



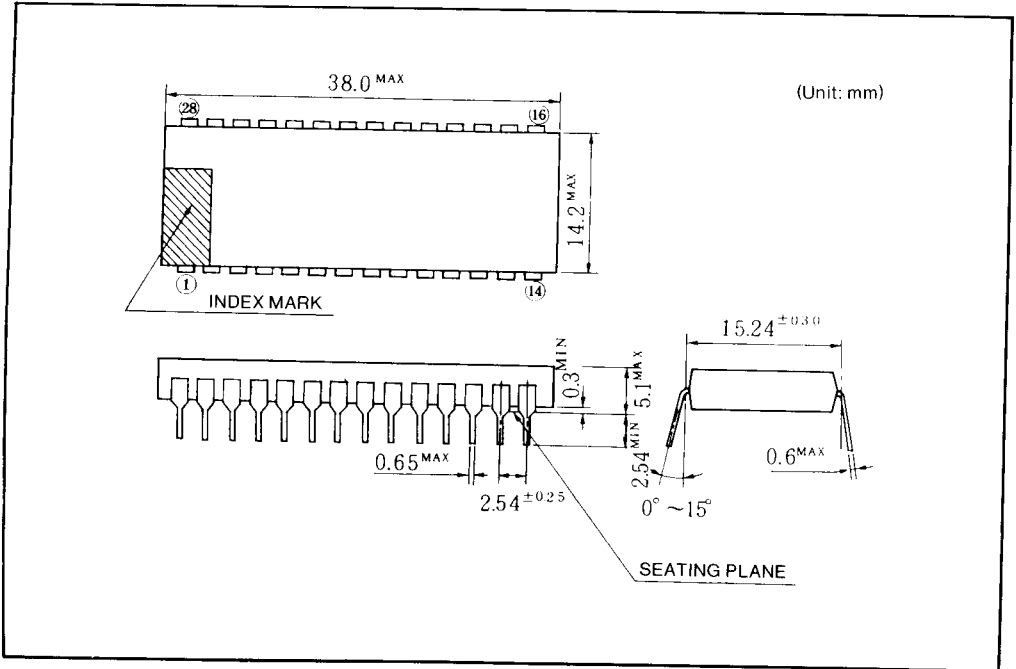
● PACKAGING ●

● 24 PIN PLASTIC DIP

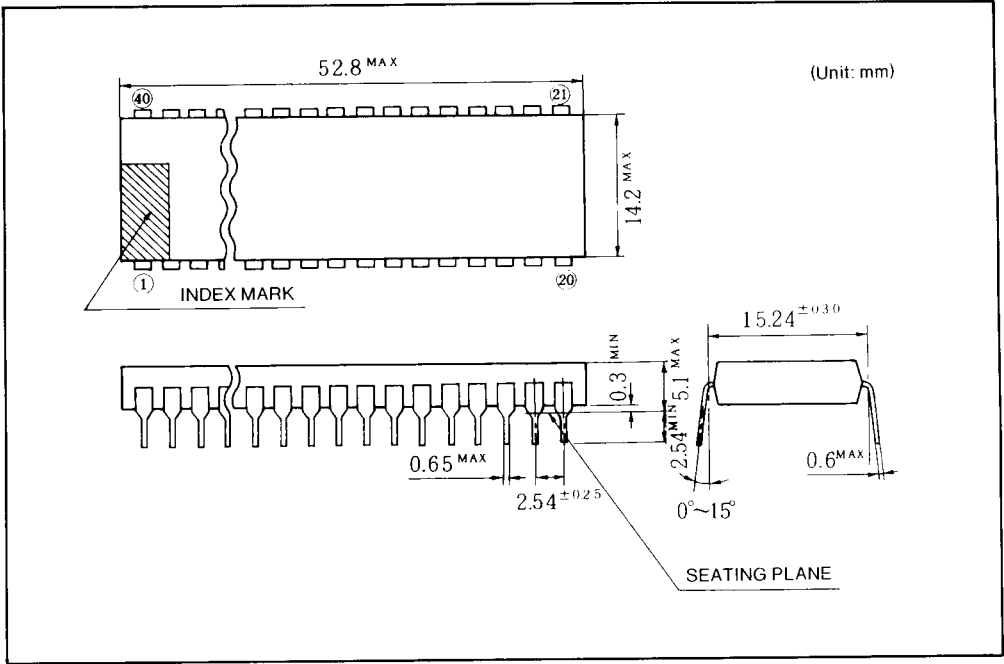
4



● 28 PIN PLASTIC DIP

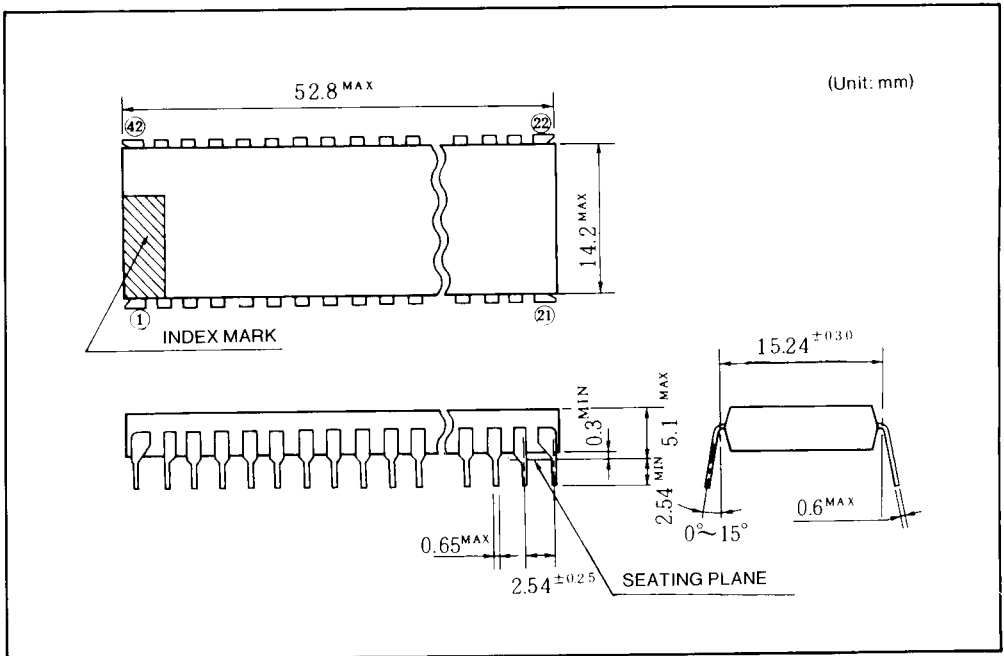


• 40 PIN PLASTIC DIP



4

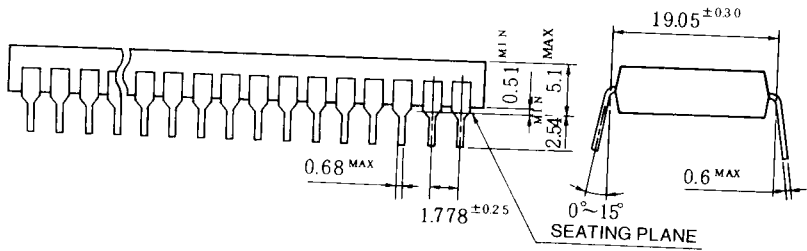
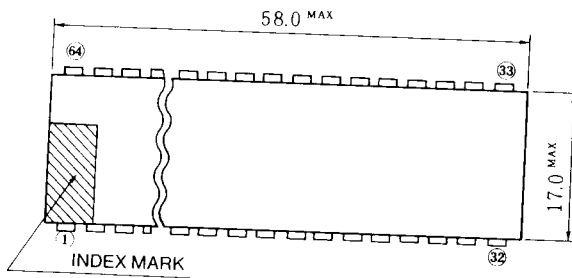
• 42 PIN PLASTIC DIP



• PACKAGING •

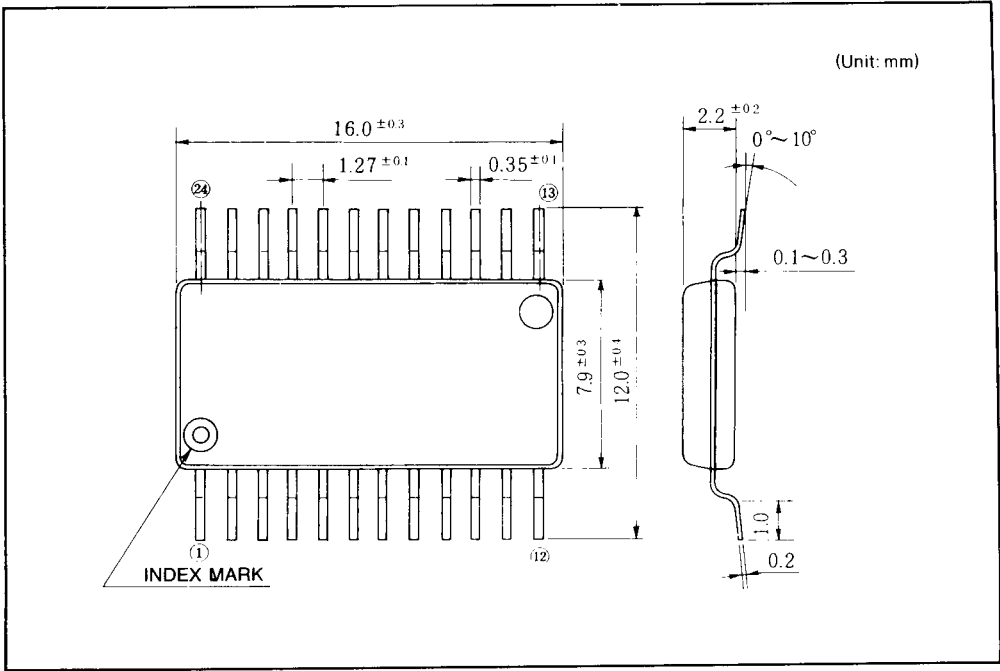
• 64 PIN SHRINK DIP

(Unit: mm)



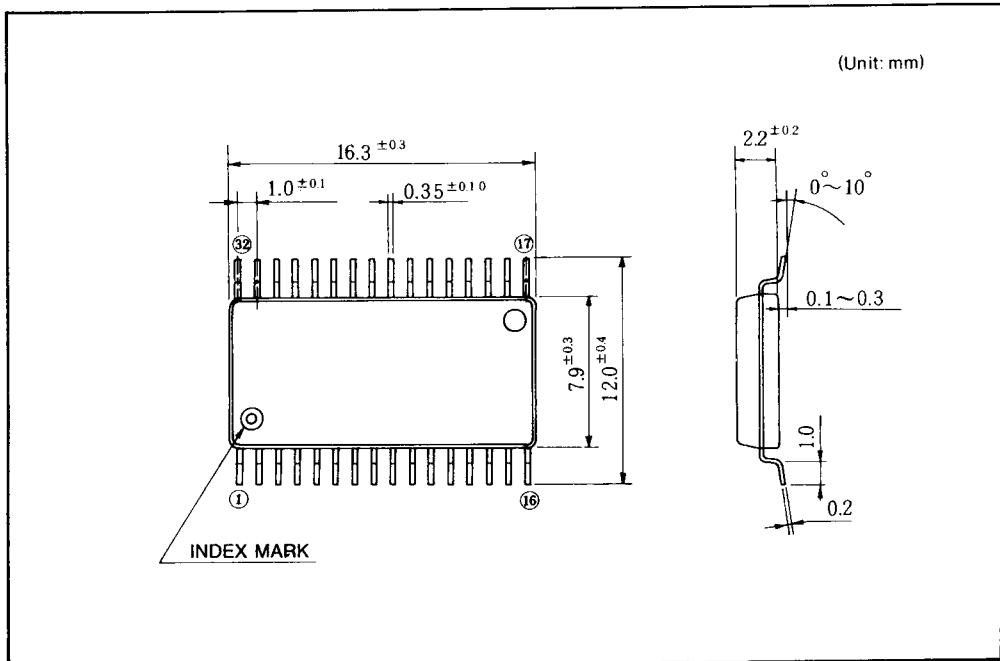
4

● 24 PIN PLASTIC FLAT



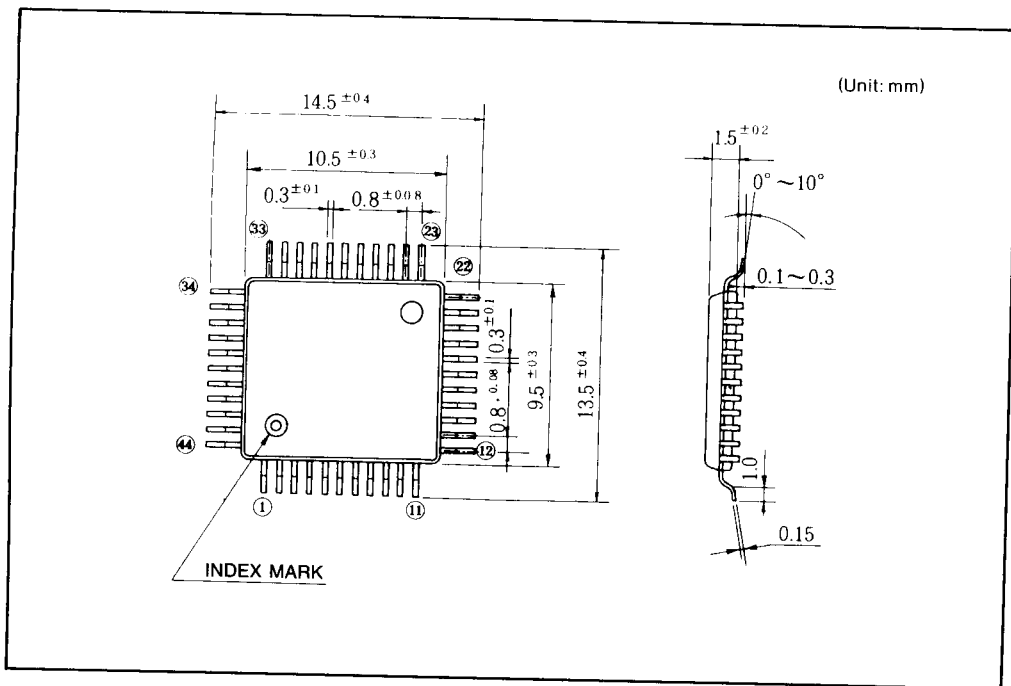
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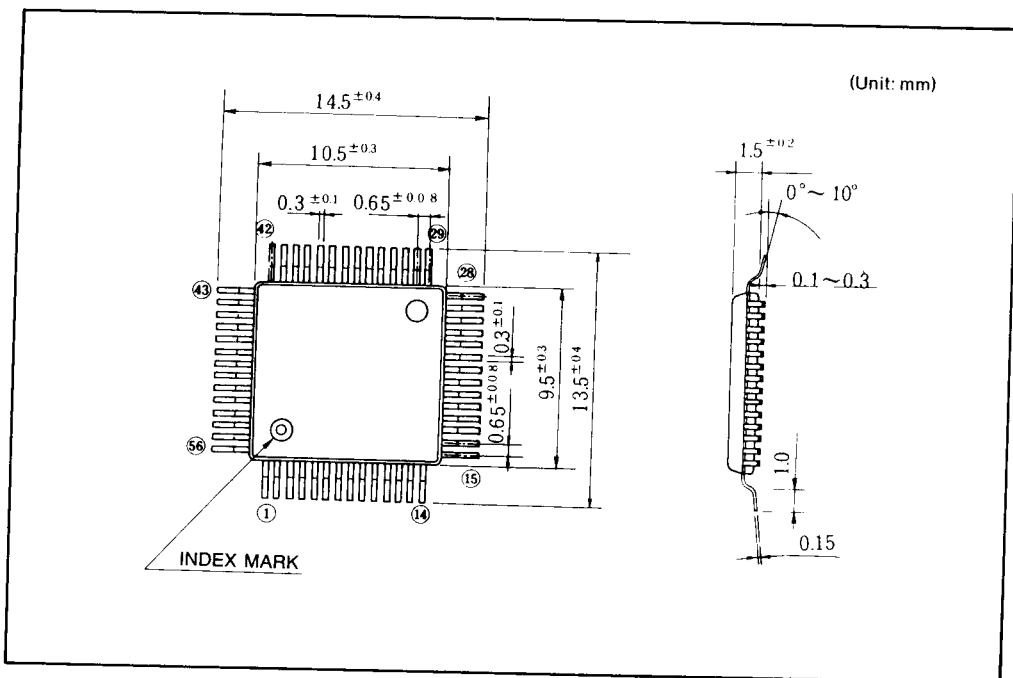


● PACKAGING ●

● 44 PIN PLASTIC FLAT

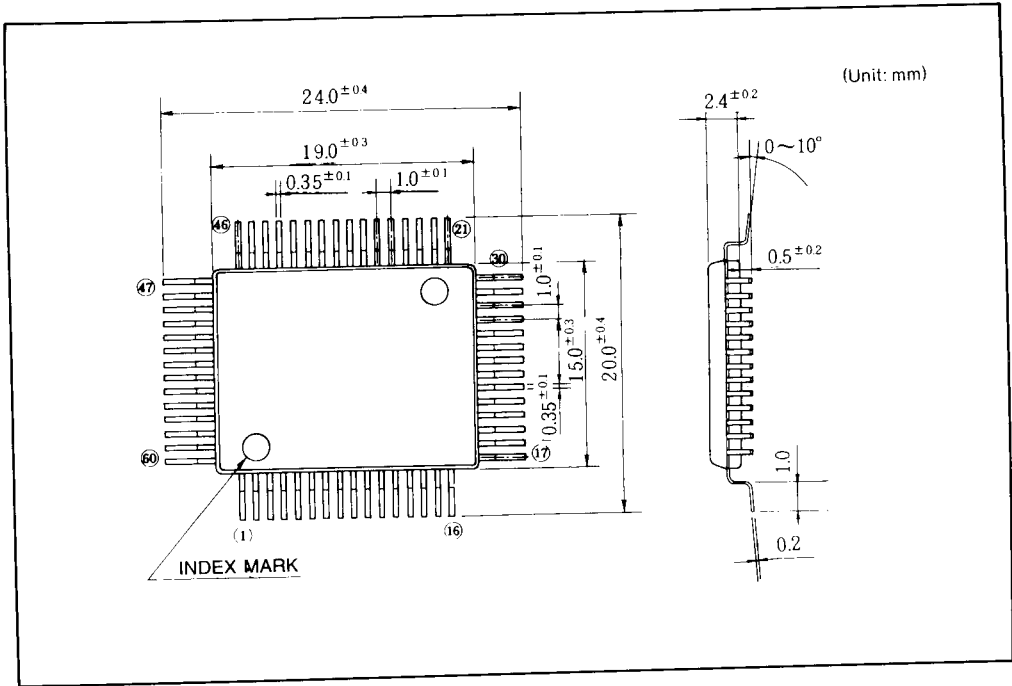


● 56 PIN PLASTIC FLAT



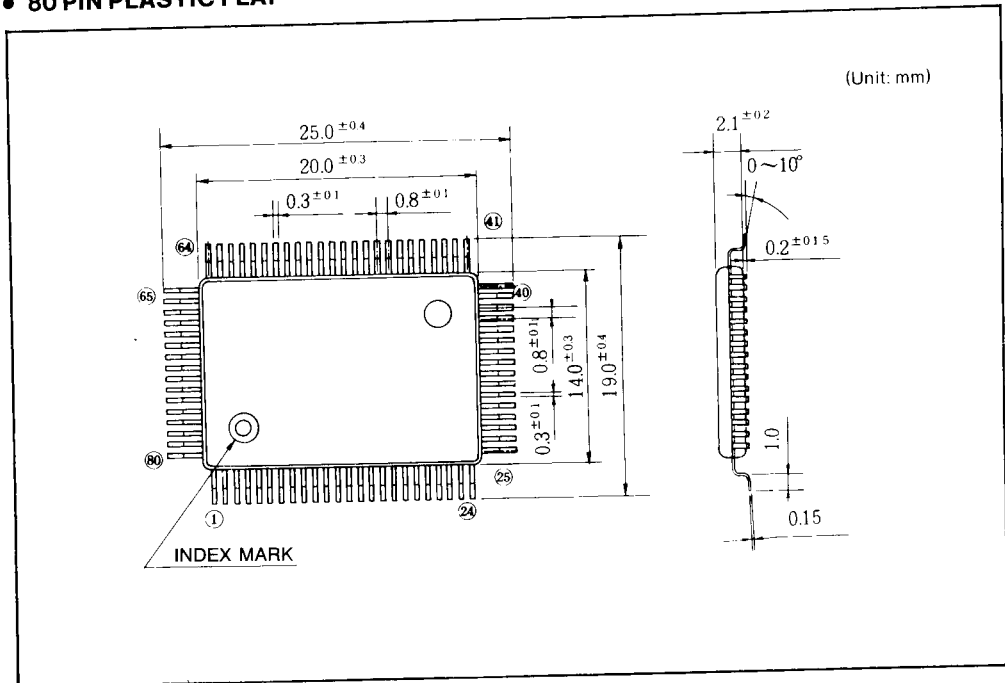
4

● 60 PIN PLASTIC FLAT



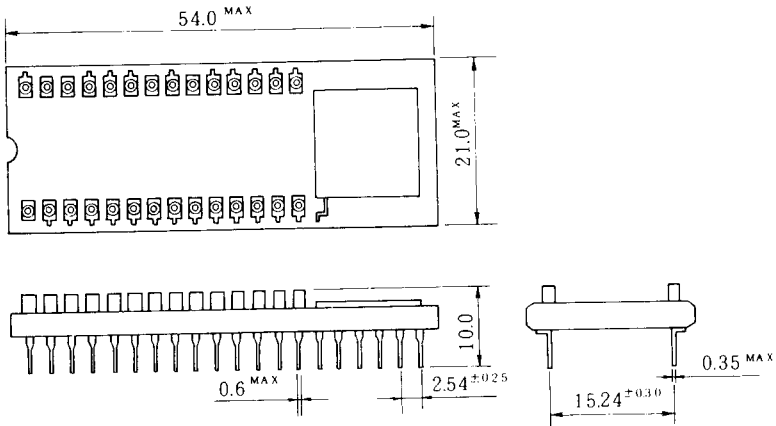
4

● 80 PIN PLASTIC FLAT



• 40 PIN PIGGY BACK

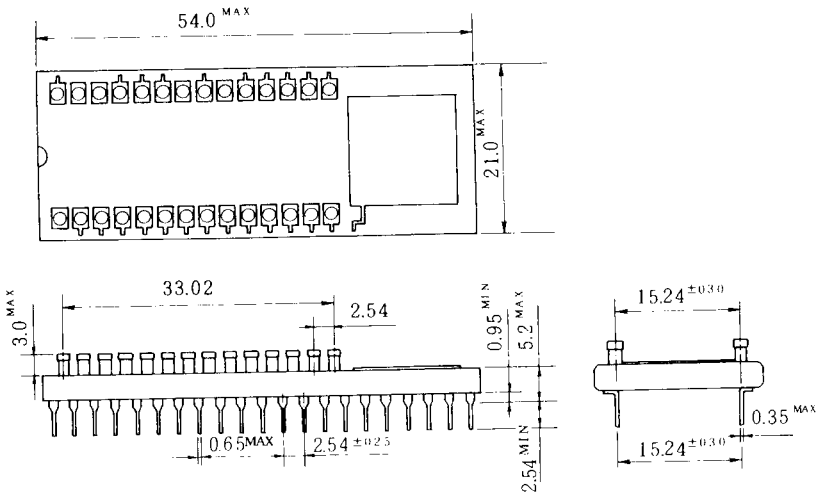
(Unit: mm)



4

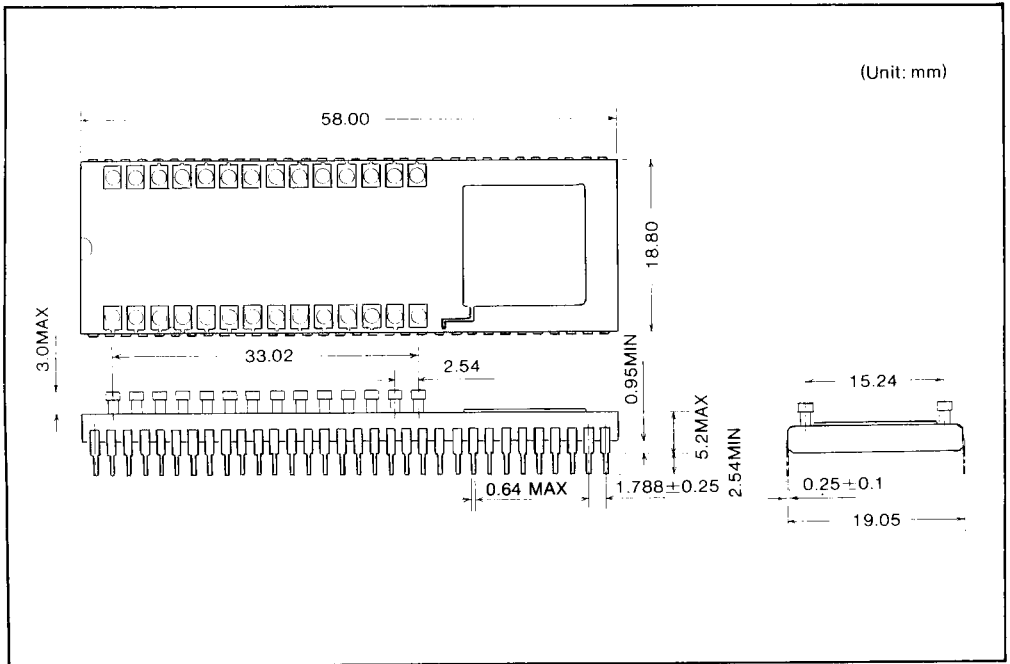
• 42 PIN PIGGY BACK

(Unit: mm)



• PACKAGING •

• 64 PIN SHRINK PIGGY BACK



4

RELIABILITY INFORMATION



RELIABILITY INFORMATION

1. INTRODUCTION

Semiconductor devices play a leading role in the explosive progress of technology. They use some of the most advanced design and manufacturing technology developed to date. With greater integration, diversity and reliability, their applications have expanded enormously. Their use in large scale computers, control equipment, calculators, electronic games and in many other fields has increased at a fast rate.

A failure in electronic banking or telephone switching equipment, for example, could have far reaching effects and can cause incalculable losses. So, the demand, for stable, high quality memory devices is strong.

We, at Oki are fully aware of this demand. So we have adopted a comprehensive quality assurance system based on the concept of consistency in development, manufacturing and sales.

With the increasing demand for improvement in function, capability and reliability, we will expand our efforts in the future. Our quality assurance system and the underlying concepts are outlined briefly below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

The quality assurance system employed by Oki can be divided into four major stages: device planning, developmental prototype, production prototype, and mass production. This system is outlined in the following block diagram (Fig. 1).

1) Device planning stage

To manufacture devices that meet market demands and satisfy customer needs, we carefully consider functional and failure rate requirements, utilization form, environment and other conditions. Once we determine the proper type, material and structure, we check the design and manufacturing techniques, and the line processing capacity. Then we prepare the development planning and time schedule.

2) Developmental prototype stage

We determine circuits, pattern design, process settings, assembly techniques and structural requirements during this stage. At the same time, we carry out actual prototype reliability testing. Since device quality is largely determined during the designing stage, Oki pays careful attention to quality confirmation during this stage.

This is how we do it:

- (1) After completion of circuit design (or pattern design), personnel from the design, process technology, production technology, installation technology and reliability departments get together for a thorough review to ensure

design quality and to anticipate problems that may occur during mass production. Past experience and know-how guide these discussions.

- (2) Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.

Note: TEG (Test Element Group) refers to the device group designed for stability evaluation of MOS transistors, diodes, resistors, capacitors and other circuit component element used in LSI memories.

- (3) Prototypes are subjected to repeated reliability and other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Production prototype stage

During this stage, various tests check the reliability and other special features of the production prototype at the mass production factory level. After confirming the quality of a device, we prepare the various standards required for mass production, and then start production. Although reliability and other special tests performed on the production prototype are much the same as those performed on the developmental prototype, the personnel, facilities and production site differ for the two prototypes, necessitating repeated confirmation tests.

4) Mass production

During the mass production stage, careful management of purchased materials, parts and facilities used during the manufacturing process, measuring equipment, manufacturing conditions and environment is necessary to ensure device quality first stipulated during the designing stages. The manufacturing process (including inspection of the completed device) is followed by a lot guarantee inspection to check that the specified quality is maintained under conditions identical to those under which a customer would actually use the device. This lot guarantee inspection is performed in three different forms as shown below.

- (1) Group A tests: appearance, labels, dimensions and electrical characteristics inspection
- (2) Group B tests: check of durability under thermal and mechanical environmental stresses, and operating life characteristics
- (3) Group C tests: performed periodically to check operational life, etc., on a long term basis.

Note: Like the reliability tests, the group B tests conform to the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

5

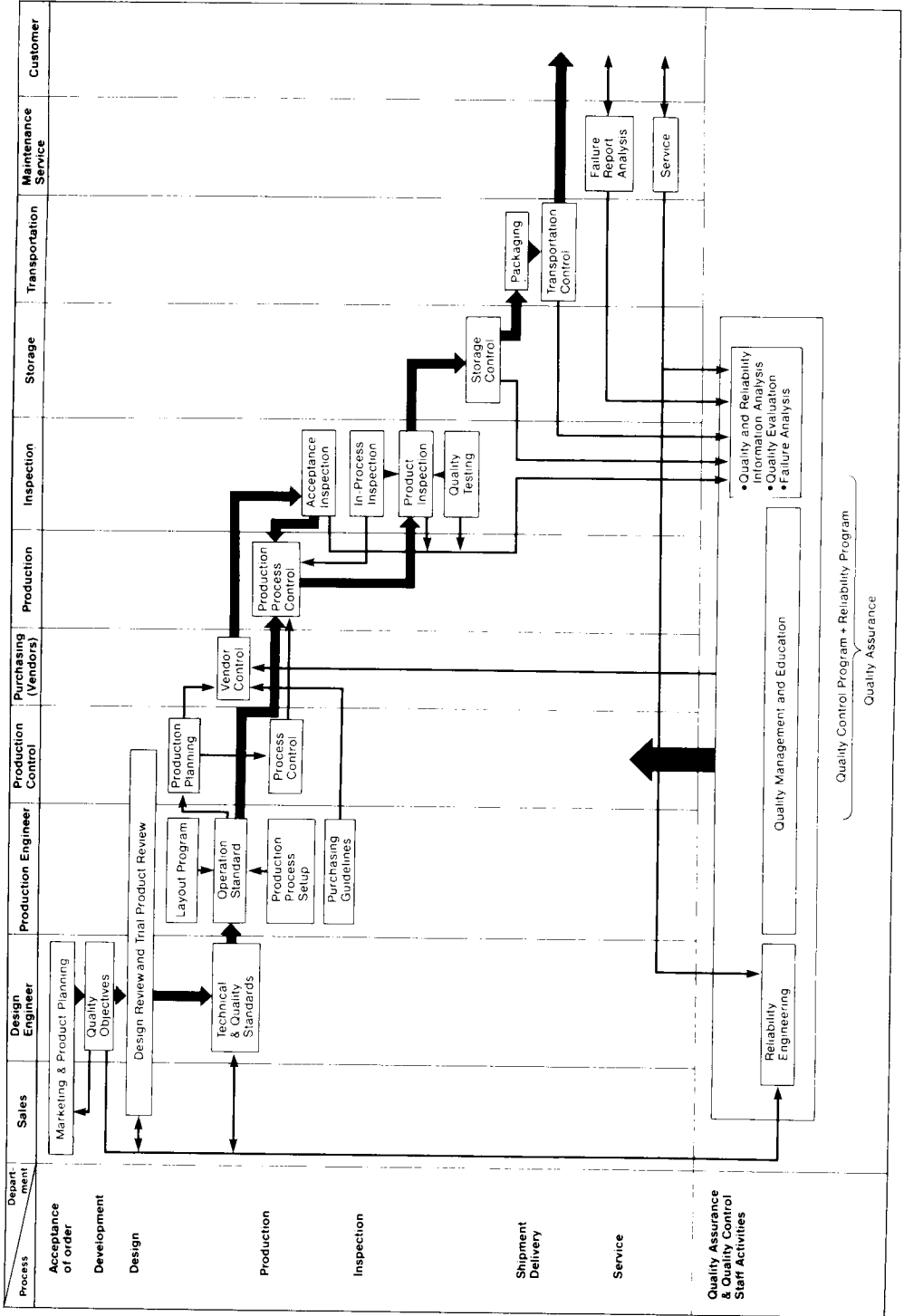


Figure 1 Quality Assurance System

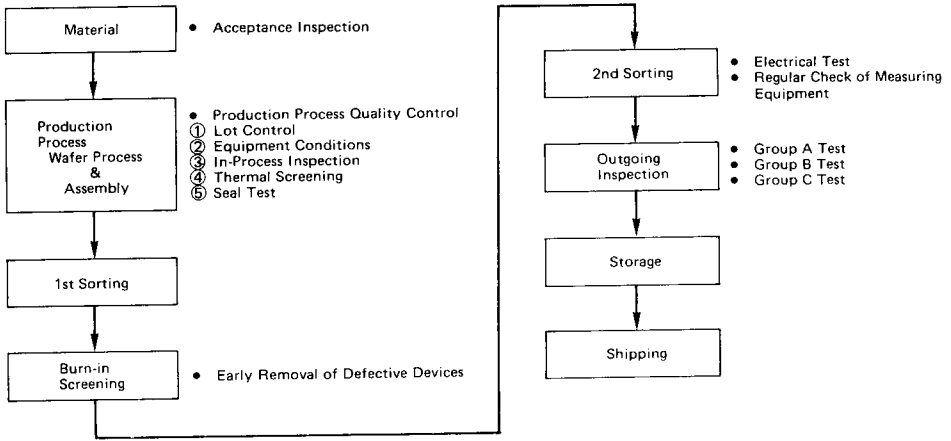


Figure 2 Manufacturing Process

Devices which pass these lot guarantee inspections are stored in a warehouse awaiting shipment to customers. Standards are also set up for handling, storage and transportation during this period, thereby ensuring quality prior to delivery. Figure 2 shows the manufacturing flow of the completed device.

5) At Oki, all devices are subjected to thorough quality checks. If, by chance, a failure does occur after delivery to the customer, defective devices are processed and the problem rectified immediately to minimize the inconvenience to the customer in accordance with the following flowchart.

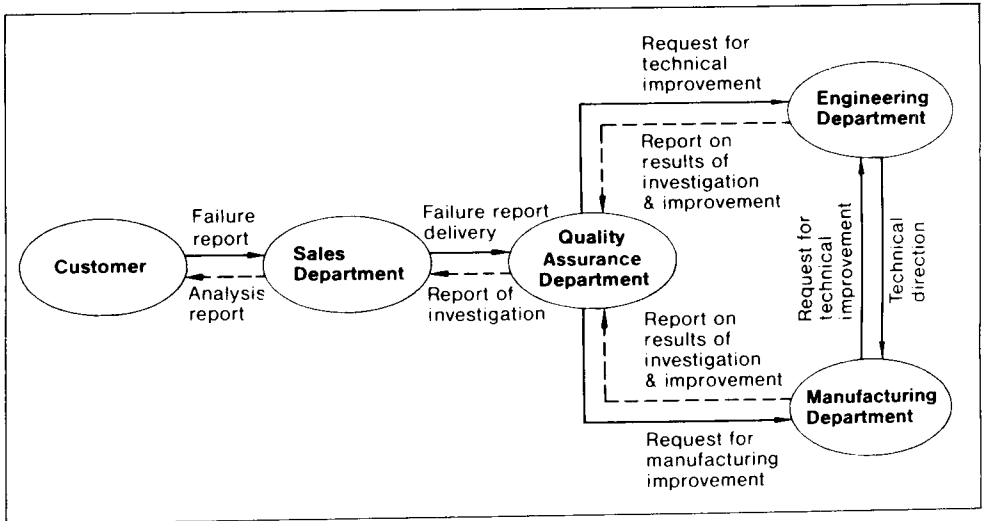
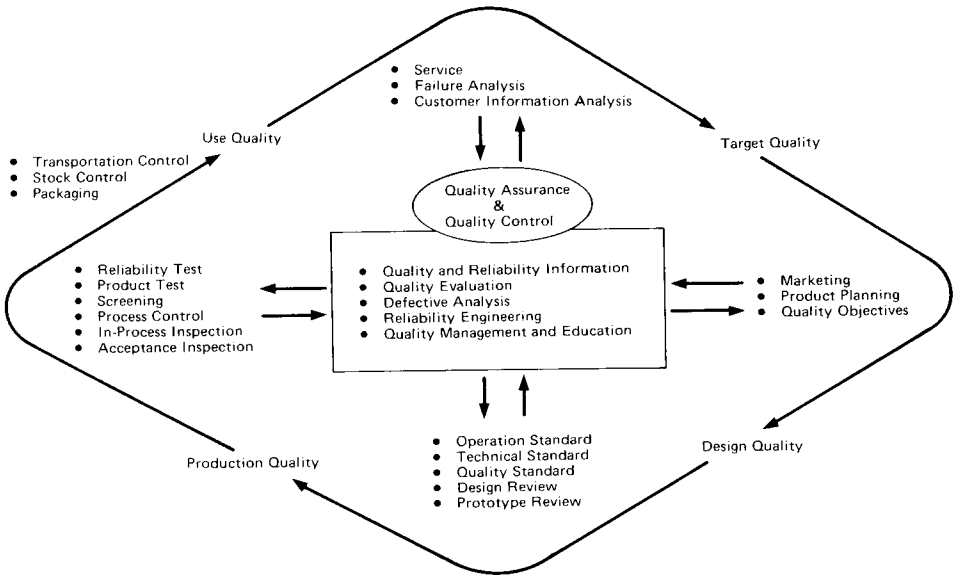


Figure 3 Failure report process

5



3. EXAMPLE OF RELIABILITY TEST RESULTS

We have outlined the quality assurance system and the underlying concepts employed by Oki. Now, we will give a few examples of the reliability tests performed during the developmental and production prototype stages. All reliability tests performed by Oki conform to the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

Since these reliability tests must determine performance under actual working conditions in a short period of time, they are performed under severe test conditions. For example, the 125°C high temperature continuous operation test performed for 1000 hours is equivalent to testing device life from 2 to 300 years of use at $T_a = 40^\circ\text{C}$.

By repeating these accelerated reliability tests, device quality is checked and defects analyzed. The resulting information is extremely useful in improving the manufacturing processes. Some of the more common defects in LSI elements and their analysis are described on next page.

MICROCONTROLLER LIFE TEST RESULTS

Part name		MSM80C31/51-XXRS			MSM80C35/39/48/49-XXRS			MSM83C154-XXRS			Referred standard
Function		8 BIT ONE CHIP MICROCONTROLLER			8 BIT ONE CHIP MICROCONTROLLER			8 BIT ONE CHIP MICROCONTROLLER			
Test item	Test condition	Sample size (pcs)	Test hours	Failures	Sample size (pcs)	Test hours	Failures	Sample size (pcs)	Test hours	Failures	
Operating life test	Ta = 125°C Vcc = 6V	88	2000 (H)	0	88	2000 (H)	0	88	2000 (H)	0	MIL-STD-883C METHOD 1005
Temperature humidity test	Ta = 85°C RH = 85% Vcc = 6V	100	2000 (H)	0	100	2000 (H)	0	100	2000 (H)	0	
Temperature cycling test	-55°C ⇄ RT ⇄ 150°C (30 min) ↑ (30 min) (5 min)	100	500 (cy)	0	100	300 (cy)	0	100	500 (cy)	0	MIL-STD-883C METHOD 1010
Pressure cooker test	Ta = 121°C RH = 100% 2 atm	50	200 (H)	0	50	200 (H)	0	50	200 (H)	0	

5

Part name		MSM6404-XXJS			MSM80C31JS			Referred standard
Function		4 BIT ONE CHIP MICROCONTROLLER			8 BIT ONE CHIP MICROCONTROLLER			
Test item	Test condition	Sample size (pcs)	Test hours	Failures	Sample size (pcs)	Test hours	Failures	
Operating life test	Ta = 125°C Vcc = 6V	88	2000 (H)	0	88	2000 (H)	0	MIL-STD-883C METHOD 1005
Temperature humidity test	Ta = 85°C RH = 85% Vcc = 6V	100	2000 (H)	0	100	2000 (H)	0	
Temperature cycling test	-55°C ⇄ RT ⇄ 150°C (30 min) ↑ (30 min) (5 min)	100	500 (cy)	0	100	500 (cy)	0	MIL-STD-883C METHOD 1010
Pressure cooker test	Ta = 121°C RH = 100% 2 atm	50	200 (H)	0	50	200 (H)	0	

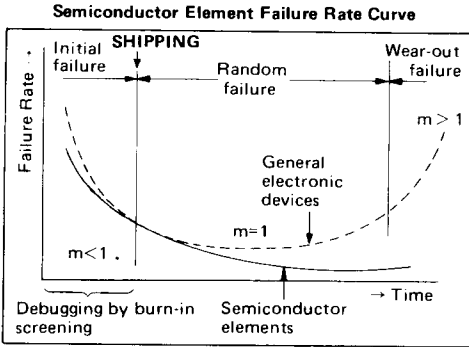
MICROCONTROLLER ENVIRONMENTAL TEST RESULTS

Part name		MSM80C31/51-XXRS	MSM80C35/39/48/49-XXRS		MSM83C154-XXRS		Referred standard		
Function		8 BIT ONE CHIP MICROCONTROLLER	8 BIT ONE CHIP MICROCONTROLLER		8 BIT ONE CHIP MICROCONTROLLER				
Test item	Test condition	Sample size (pcs)	Failures	Sample size (pcs)	Failures	Sample size (pcs)	Failures		
Soldering Heat Test	260°C 10 SEC	22	0	22	0	22	0	MIL-STD-883C METHOD 2003	
Temperature Cycling Test	-55°C±RT±150°C (30min) (5min) (30min) 20 cycles	22	0	22	0	22	0	MIL-STD-883C METHOD 1010	
Thermal Shock Test	100°C±0°C (5min) (5min) 10 cycles	22	0	22	0	22	0	MIL-STD-883C METHOD 1011	
Lead Integrity	Tensile	500 g 10 SEC	11	0	11	0	11	0	MIL-STD-883C METHOD 2004
	Bending	250 g 90° BEND 3 TIMES							
Solderability	230°C 5 SEC	22	0	22	0	22	0	MIL-STD-883C METHOD 2003	

Part name		MSM6404 XXJS	MSM80C31JS		Referred standard		
Function		4 BIT ONE CHIP MICROCONTROLLER	8 BIT ONE CHIP MICROCONTROLLER				
Test item	Test condition	Sample size (pcs)	Failures	Sample size (pcs)	Failures		
Thermal Environmental Test	PRE-Bake	Bake (125°C, 6 hrs)	22	0	22	0	
	Soldering Heat Test	Vapor Phase Reflow (215±2°C, 90+10, -0sec) 2 times					
	Temperature Cycling Test	-55°C±RT±150°C (30min) (5min) (30min) 20 cycles					
	Thermal Shock Test	100°C±0°C (5min) (5min) 10 cycles					
Other Test	Solderability	○ Bake (125°C, 24hrs) ○ Immerse into Flux ○ Immerse into Solder (215±2°C 10±1sec)	22	0	22	0	MIL-STD-883C METHOD 1010 MIL-STD-883C METHOD 1011

4. SEMICONDUCTOR MEMORY FAILURES

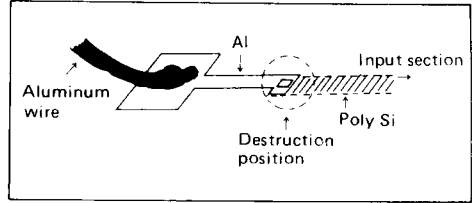
The life-span characteristics of semiconductor elements in general (not only semiconductor IC devices) are described by the curve shown in the diagram below. Although semiconductor memory failures are similar to those of ordinary integrated circuits, the degree of integration (miniaturization), manufacturing complexity and other circuit element factors influence their incidence.



1) Surge Destruction

This is destruction of the input/output stage circuits by external surge currents or static electricity. The accompanying photograph shows a point of contact between aluminum and polysilicon that has been dissolved by a surge current. A hole has formed in the substrate silicon, leading to a short circuit. This kind of failure is traceable in about 30% of defective devices returned to the manufacturer. Despite miniaturization of semiconductor memory component elements (which means the elements themselves are less resistant), these failures usually occur during assembly and other handling operations. At Oki, all devices are subjected to static electricity intensity tests (under simulated operation-

al conditions) in the development stage to reduce this type of failure. In addition to checking endurance against surge currents, special protective circuits are incorporated in the input and output sections.



2) Oxide Film Insulation Destruction (Pin Holes)

Unlike surge destruction, this kind of failure is caused by manufacturing defects. Locally weakened sections are ruptured when subjected to external electrical stress. Although this problem is accentuated by the miniaturization of circuit elements, it can be resolved by maintaining an ultra-clean manufacturing environment and through 100% burn-in screening.

3) Surface Deterioration due to Ionic Impurities

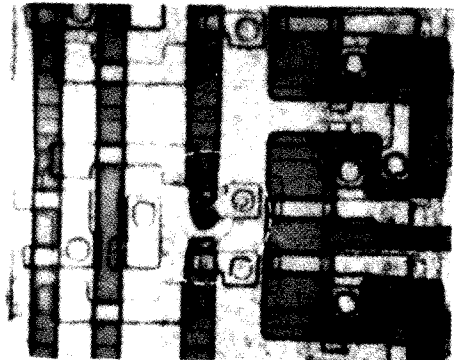
Under some temperature and electric field conditions, charged ionic impurities moving within the oxide film previously resulted in occasional deterioration of silicon surfaces. This problem has been eliminated by new surface stabilization techniques.

4) Photolithographic Defects

Integrated circuits are formed by repeated photographic etching processes. Dust and scratches on the mask (which corresponds to a photographic negative) can cause catastrophic defects. At present, component elements have been reduced in size to the order of 10 μ m through miniaturization. However, the size of dust and scratches stays the same. At Oki, a high degree of automation, minimizing human intervention in the process, and unparalleled cleanliness, solves this problem.



Example of surge destruction



Photolithographic Defect

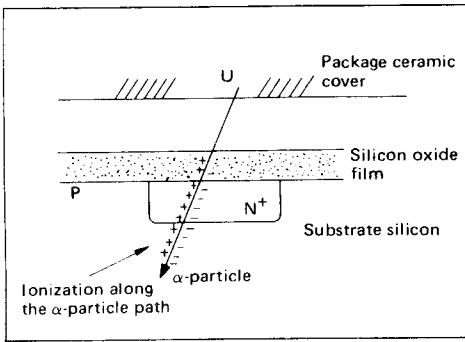
5

5) Aluminum Corrosion

Aluminum corrosion is due to electrolytic reactions caused by the presence of water and minute impurities. When aluminum dissolves, lines break. This problem is unique to the plastic capsules now used widely to reduce costs. Oki has carefully studied the possible cause and effect relationship between structure and manufacturing conditions on the one hand, and the generation of aluminum corrosion on the other. Refinements incorporated in Oki LSIs permit superior endurance to even the most severe high humidity conditions.

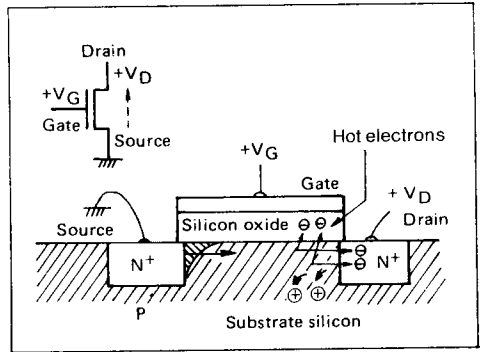
6) Alpha-Particle Soft Failure

This problem occurs when devices are highly miniaturized, such as in 1 megabit RAMs. The inversion of memory cell data by alpha-particle generated by radio-active elements like uranium and thorium (present in minute quantities, measured in ppb) in the ceramic package material causes defects. Since failure is only temporary and normal operation restored quickly, this is referred to as a "soft" failure. At Oki we have eliminated the problem by coating the chip surface of 1 megabit RAMs with a resin which effectively screens out these alpha-particles.



7) Degradation in Performance Characteristics Due to Hot Electrons

With increased miniaturization of circuit elements, internal electric field strength in the channels increases since the applied voltage remains the same at 5V. As a result, electrons flowing in the channels, as shown in the accompanying diagram, tend to enter into the oxide film near the drain, leading to degradation of performance. Although previous low-temperature operation tests have indicated an increase of this failure, we have confirmed by our low-temperature acceleration tests, including checks on test element groups, that no such problem exists in Oki LSIs.



Characteristic deterioration caused by hot electrons

With further progress in the miniaturization of circuit components, failures related to pin hole oxide film destruction and photolithography have increased. To eliminate these defects during manufacturing, Oki has been continually improving its production processes based on reliability tests and information gained from the field. And we subject all devices to high-temperature burn-in screening for 48 to 96 hours to ensure even greater reliability.

5

DATA SHEETS



OLMS-40 SERIES

OKI semiconductor

MSM5840

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER

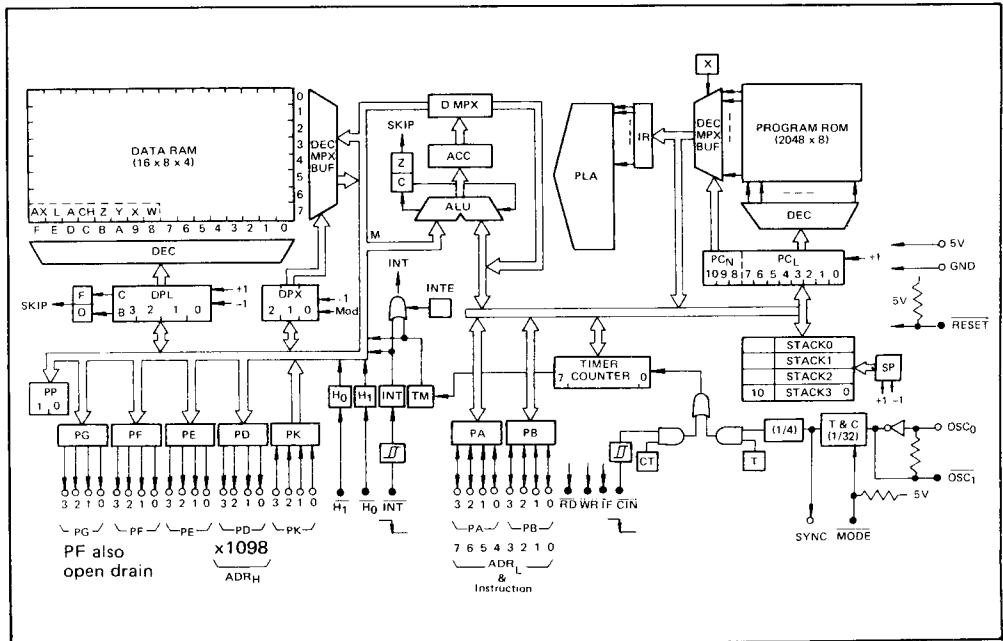
GENERAL DESCRIPTION

The OKI MSM5840 microcontroller is a low-power, high-performance single chip device implemented in complementary metal oxide semiconductor technology. Integrated within this one chip are 16K bits of mask program ROM, 512 bits of data RAM, 30 Input/Output lines, a programmable timer/counter, and oscillator. Program memory is byte wide and data-paths are organized in 4 bit nibbles. RAM and I/O lines are bit addressable. Up to 4K of external ROM interfaces to the 8 bit bidirectional bus. 98 instructions include binary, BCD, logical operations; bit set, reset, test, 8 bit I/O; relative jumps; multifunctional instructions (increment, modify, skip); 8 bit wide table output; subroutine call and return. 94% of instructions are single byte, single cycle operations.

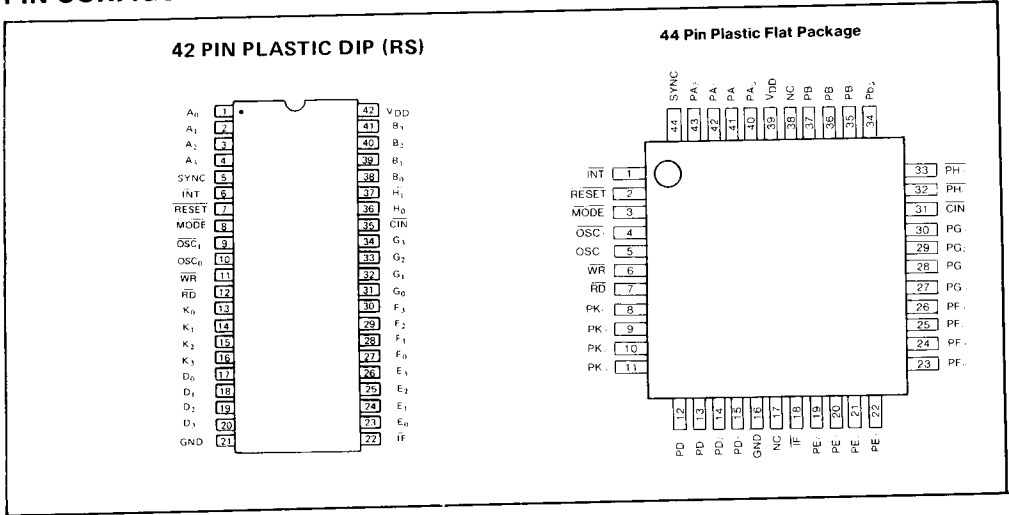
FEATURES

- Low Power Consumption – 8mW Typical
- 100% Static Logic – 50 μ W Standby, Typical
- 2K \times 8 Internal ROM
- Up to 4K \times 8 External ROM
- 128 \times 4 Internal RAM
- 30 I/O Lines Incl. 8 Bit Data Bus
- Programmable 8 Bit Timer/Counter
- Self-contained Oscillator
- 98 Instructions
- Expandable Memory and I/O
- 2 Interrupt Levels
- 4 Stack Levels
- Operating Temperature –40 $^{\circ}$ to +85 $^{\circ}$ C
- 3V to 6V Operating V_{DD}
- Battery Powered or Battery Backup
- TTL Compatible (with pullups)
- 7.6 μ s Cycle Time @ 4.2MHz (V_{DD} 5V \pm 10%)

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



6

PIN DESCRIPTION

Designation	Pin No.	Function
GND	21	Circuit GND potential
VDD	42	Main power source (+5V)
OSC ₀	10	Crystal OSC input, external clock input
OSC ₁	9	Crystal OSC input, external clock output (not TTL compatible)
PA, PB	1 to 4 38 to 41	Pseudo-bidirectional ports for 4-bit parallel I/O. Used as a pair for 8-bit I/O. Used to output 8 LSBs of address in external ROM mode. Used to read external instruction during IF.
PD, PE, PE, PG	17 to 20 23 to 34	Output ports for 4-bit parallel output and bit set/reset. Specified by internal port pointer, Bit position specified by set/reset instruction. PD also used for instruction address MSBs in external ROM mode during IF.
PK	13 to 16	4-bit parallel or bit test input port (unlatched)
PH	36 and 37	2-bit input port with latched memory (negative level sensitive)
RESET	7	RESET has priority over every other signal. (see MSM5840 user's manual for initialization sequence)
MODE	8	Used to enable external ROM mode during RESET and also to enable STOP mode during execution (for stepping program)
INT	6	Negative edge sensitive external interrupt signal associated with EI and DI instructions. Vectors to location 200H.
CIN	35	Negative edge sensitive external input for counter associated with ECT and DCT instructions. Vectors to location 100H. (same as timer)
SYNC	5	General purpose synchronizing signal output at the beginning of each machine cycle. Used for address strobe during external ROM mode.
RD	12	Read strobe pulse occurring when port A or B is read (1A, 1B, 1AB)
WR	11	Write strobe pulse occurring when port A or B is written (OA, OB, OAB, OBS, OTD)
IF	22	Read strobe pulse occurring during an instruction fetch from external ROM.

FUNCTIONAL DESCRIPTION

Program ROM

The MSM5840 will address up to 4K bytes of program ROM and can have 2K bytes of internal masked ROM, or all ROM may be located externally. External EPROM may be used for program development with conversion to internal ROM occurring after program debug and system check-out and verification. All instructions are byte wide. Only three of the 98 instructions require two bytes of program code. The instructions are routed to a programmed logic array which generates the necessary internal control signals.

Data RAM

Data is organized in 4 bit nibbles. Internal data RAM consists of 128 nibbles, 8 nibbles of which are dedicated registers accessible directly under program control. These are the general purpose registers, W, X, Y and Z, and the 4 save (exchange) registers, CH, A, L, and AX. All other DATA RAM must be addressed indirectly through the DP (data pointer) registers, a seven bit pointer (directly accessible by numerous instructions) consisting of 4 bit DPL register and a 3 bit DP_H register. Any nibble of internal data RAM can be accessed through the DP registers. Some instructions automatically change the contents of the DP registers allowing efficient array processing.

Input/Output Ports

PA, PB – These two ports are pseudo-bidirectional ports which can be used as simple I/O lines or used as either a 4-bit or 8-bit parallel bus. An instruction fetches the external ROM data through these ports by outputting the 8 low order bits of address during SYNC followed by an IF (instruction fetch) cycle. In addition, synchronized data transfers are possible through these ports with the I/O pin signals \overline{RD} and \overline{WR} associated with certain input/output instructions dedicated to these ports. In short, PA and PB can be used as a multiplexed address/instruction/data bus.

PD, PE, PF, PG – These four output ports are addressed indirectly through the TWO BIT port pointer whose contents are changed through certain instructions. These ports are bit (set/reset) addressable. PD is also used for the high order bits of address during an external instruction fetch. PF and PG are open drain outputs and PG is set high by a hardware RESET.

PK is an input port without memory, addressable either as a nibble or bit level input.

PH is a two-bit input port with memory, which can be tested and reset under program control.

External Interrupt

The \overline{INT} pin can be tested under program control or enabled to cause a vectored interrupt to location 200H. It is negative edge sensitive.

Timer/Counter

The timer/counter is an 8-bit counter whose input is selected under program control to be either an external signal (CIN) or an internal square wave of 1/128 the frequency of the OSC₀ input ($2\text{ MHz}/128 = 15.625\text{ kHz}$). The timer/counter can be enabled or disabled under program control as can be associated internal interrupt which vectors to location 100H and has higher priority than the external interrupt.

Stack

The stack is an LIFO queue for storing return-from-interrupt and return-from-subroutine address information. It is eleven bits wide and 4 levels deep.

Program Counter (PC)

The program counter is 11 bits wide and loaded under program control.

Accumulator

The accumulator register is the data path focal point of the CPU. Approximately one-half of the instructions involve the accumulator. Its contents are the source and destination for many ALU operations and port operations. CASE statements (computed GOTOs) are possible by using the Jump with Accumulator (JA) instruction.

Flags

The MSM5840 is endowed with the following set of flags.

Z – zero flag	:	Indicates that the result of the previous operation was zero
F – all ones	:	Indicates a carry from the DP _L register
O – all zeros	:	Indicates a borrow from the DP _L register
C – carry	:	Indicates a carry from the previous operation
T – timer	:	Indicates that the timer/counter is specified as a timer
CT – counter	:	Indicates that the timer/counter is specified as a counter
TM – timer flag	:	Indicates an overflow of the timer/counter register
INT – interrupt	:	Latching memory flag for the external interrupt
INTE – interrupt enable	:	Indicates that interrupts have been enabled
H ₀ – H ₀ memory	:	Indicates that an input has been detected on the H ₀ input
H ₁	:	same as H ₀ except H ₁ input
X	:	0 indicates internal ROM, 1 indicates external ROM. If all external ROM, 0 indicates first bank of 2K.

INSTRUCTION SET

Mnemonic	Description	Instruction Code								Byte	Cycle	
		7	6	5	4	3	2	1	0			
Load, Store, Read, Clear	CLA	Clear Accumulator	0	0	0	1	0	0	0	0	1	1
	CLL	Clear DP _L	0	0	1	0	0	0	0	0	1	1
	CLH	Clear DP _H	0	1	1	0	0	0	0	0	1	1
	LAI	Load Accumulator with Immediate	0	0	0	1	i ₃	i ₂	i ₁	i ₀	1	1
	LLI	Load DP _L with Immediate	0	0	1	0	i ₃	i ₂	i ₁	i ₀	1	1
	LHI	Load DP _H with Immediate	0	1	1	0	0	i ₂	i ₁	i ₀	1	1
	L	Load Accumulator with Memory	1	0	0	1	0	1	0	0	1	1
	LM	Load Accumulator with Memory then Modify DP _H	1	0	0	1	0	1	i ₁	i ₀	1	1
	LAL	Load Accumulator with DP _L	0	1	0	1	0	1	0	1	1	1
	LLA	Load DP _L with Accumulator	0	1	0	1	0	1	0	0	1	1
	LAW	Load Accumulator with W Register	1	0	0	0	0	1	0	0	1	1
	LAX	Load Accumulator with X Register	1	0	0	0	0	1	0	1	1	1
	LAY	Load Accumulator with Y Register	1	0	0	0	0	1	1	0	1	1
	LAZ	Load Accumulator with Z Register	1	0	0	0	0	1	1	1	1	1
	SI	Store Accumulator to Memory then Increment DP _L	1	0	0	1	0	0	0	0	1	1
	SMI	Store Accumulator to Memory then Modify DP _H and Increment DP _L	1	0	0	1	0	0	i ₁	i ₀	1	1
	LWA	Load W Register with Accumulator	1	0	0	0	0	0	0	0	1	1
	LXA	Load X Register with Accumulator	1	0	0	0	0	0	0	1	1	1
	LYA	Load Y Register with Accumulator	1	0	0	0	0	0	1	0	1	1
	LZA	Load Z Register with Accumulator	1	0	0	0	0	0	1	1	1	1
LPA	Load Port Pointer with Accumulator	0	1	0	1	1	0	0	0	1	1	
LTI	Load Timer with Immediate	0	1	1	0	1	0	0	0	2	2	
RTH	Read Timer H	1	7	6	5	4	3	2	1	0	1	1
RTL	Read timer L	0	1	1	0	1	0	1	1	1	1	
Exchange	XA	Exchange Accumulator with Save Register A	0	1	0	0	1	0	0	1	1	1
	XL	Exchange DP _L with Save Register L	0	1	0	0	1	0	1	0	1	1
	XCH	Exchange DP _H and Carry with Save Register CH	0	1	0	0	1	0	0	0	1	1
	X	Exchange Accumulator with Memory	1	0	0	1	1	0	0	0	1	1
	XM	Exchange Accumulator with Memory then Modify DP _H	1	0	0	1	1	0	i ₁	i ₀	1	1
	XAX	Exchange Accumulator with Save Register AX	0	1	0	0	1	0	1	1	1	1
Increment/Decrement	INA	Increment Accumulator	0	0	0	0	0	0	0	1	1	1
	INL	Increment DP _L	0	1	0	1	0	1	1	1	1	1
	INM	Increment Memory	0	1	0	1	1	1	0	1	1	1
	INW	Increment W Register	1	0	0	0	1	0	0	0	1	1
	INX	Increment X Register	1	0	0	0	1	0	0	1	1	1
	INY	Increment Y Register	1	0	0	0	1	0	1	0	1	1
	INZ	Increment Z Register	1	0	0	0	1	0	1	1	1	1

6

INSTRUCTION SET (CONT.)

	Mnemonic	Description	Instruction Code								Byte	Cycle
			7	6	5	4	3	2	1	0		
Increment/Decrement	DCA	Decrement Accumulator – Skip if Not All Ones	0	0	0	0	1	1	1	1	1	1
	DCL	Decrement DP _L	0	1	0	1	0	1	1	0	1	1
	DCM	Decrement Memory	0	1	0	1	1	1	0	0	1	1
	DCW	Decrement W Register	1	0	0	0	1	1	0	0	1	1
	DCX	Decrement X Register	1	0	0	0	1	1	0	1	1	1
	DCY	Decrement Y Register	1	0	0	0	1	1	1	0	1	1
	DCZ	Decrement Z Register	1	0	0	0	1	1	1	1	1	1
	DCH	Decrement DP _H – Skip if All Ones and C = Zero	0	1	0	1	1	1	1	1	1	1
Logical	CAO	Complement Accumulator of One	0	1	0	1	0	0	0	0	1	1
	AND	And Accumulator with Memory	0	1	0	0	0	1	0	0	1	1
	OR	Or Accumulator with Memory	0	1	0	0	0	1	0	1	1	1
	EOR	Exclusive or Accumulator with Memory	0	1	0	0	0	1	1	0	1	1
	RAL	Rotate Accumulator Left through Carry	0	1	0	0	0	1	1	1	1	1
Arithmetic	AC	Add Memory to Accumulator with Carry	0	1	0	0	1	1	0	0	1	1
	ACS	Add Memory to Accumulator with Carry, Skip if Carry	0	1	0	0	1	1	0	1	1	1
	AS	Add Memory to Accumulator, Skip if Carry	0	1	0	0	1	1	1	0	1	1
	AIS	Add Immediate to Accumulator, Skip if Carry	0	0	0	0	l ₃	l ₂	l ₁	l ₀	1	1
	DAS	Decimal adjust Accumulator in Subtraction	0	1	0	1	1	0	1	0	1	1
	CM	Compare Accumulator with Memory, Skip if Equal	0	1	0	1	1	1	1	0	1	1
	AWS	Add W Register to Accumulator, Skip if Carry	1	0	0	1	1	1	0	0	1	1
	AXS	Add X Register to Accumulator, Skip if Carry	1	0	0	1	1	1	0	1	1	1
	AYS	And Y Register to Accumulator, Skip if Carry	1	0	0	1	1	1	1	0	1	1
AZS	Add Z Register to Accumulator, Skip if Carry	1	0	0	1	1	1	1	1	1	1	
Bit Set/Reset/Test	SPB	Set Port Bit	1	0	1	1	0	0	l ₁	l ₀	1	1
	RPB	Reset Port Bit	1	0	1	1	0	1	l ₁	l ₀	1	1
	SMB	Set Memory Bit	1	0	1	1	1	0	l ₁	l ₀	1	1
	RMB	Reset Memory Bit	1	0	1	1	1	1	l ₁	l ₀	1	1
	TAB	Test Accumulator Bit	1	0	1	0	0	0	l ₁	l ₀	1	1
	TMB	Test Memory Bit	1	0	1	0	0	1	l ₁	l ₀	1	1
	TKB	Test K Port Bit	1	0	1	0	1	0	l ₁	l ₀	1	1
	THB	Test H Port Bit	1	0	1	0	1	1	0	l ₀	1	1
	TI	Test Interrupt flag	1	0	1	0	1	1	1	1	1	1
	TTM	Test Time flag	1	0	1	0	1	1	1	0	1	1
	TC	Test Carry flag	0	1	0	0	0	0	1	0	1	1
	SC	Set Carry flag	0	1	0	0	0	0	0	0	1	1
	RC	Reset Carry flag	0	1	0	0	0	0	0	1	1	1

INSTRUCTION SET (CONT.)

	Mnemonic	Description	Instruction Code								Byte	Cycle
			7	6	5	4	3	2	1	0		
Branch/Subroutine	J	Jump	0	0	1	1	0	I ₁₀	I ₉	8	2	2
	JC	Jump in Current Page	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	1	1
	JA	Jump with Accumulator	1	1	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	1	1
	CAL	Call Subroutine	0	1	0	0	0	0	1	1	1	1
	RT	Return from Subroutine	0	0	1	1	1	I ₁₀	I ₉	8	2	2
Input/Output	OBS	Output Byte String	I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	1	2~17
	OTD	Output Table Data	0	1	1	1	0	0	0	0	1	2
	OA	Output Accumulator to Port A	0	1	1	1	0	0	0	1	1	1
	OB	Output Accumulator to Port B	0	1	1	1	0	0	1	0	1	1
	OP	Output Accumulator to Port P designated Port Pointer	0	1	1	1	0	0	1	1	1	1
	OAB	Output Memory and Accumulator to Ports A and B	0	1	1	1	0	1	0	1	1	1
	OPM	Output Memory to Port P designated Port Pointer	0	1	1	1	0	1	1	0	1	1
	IA	Input Port A in Accumulator	0	1	1	1	1	0	1	0	1	1
	IB	Input Port B in Accumulator	0	1	1	1	1	0	1	1	1	1
	IK	Input Port K in Accumulator	0	1	1	1	1	1	0	0	1	1
	IAB	Input Ports A and B in Memory and Accumulator	0	1	1	1	1	1	0	1	1	1
Control	EI	Enable Interrupt	0	1	0	1	0	0	1	1	1	1
	DI	Disable Interrupt	0	1	0	1	0	0	1	0	1	1
	ET	Enable Timer	0	1	1	0	1	1	1	1	1	1
	DT	Disable Timer	0	1	1	0	1	1	1	0	1	1
	ECT	Enable Counter	0	1	1	1	1	1	1	1	1	1
	DCT	Disable Counter	0	1	1	1	1	1	1	0	1	1
	HLT	Halt	0	1	1	0	1	1	0	1	1	1
	EXP	Exchange Program	0	1	1	0	1	0	0	1	1	1
	NOP	No Operation	0	0	0	0	0	0	0	0	1	1

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to 7	V
Input Voltage	V_I	$T_a = 25^\circ\text{C}$	-0.3 to V_{DD}	V
Operating Voltage PF PG	V_O	$T_a = 25^\circ\text{C}$	-0.3 to 25	V
Storage Temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	@1 MHz	3 to 6	V
		@4.2 MHz	4.5 to 5.5	V
Operating Temperature	T_{op}		-40 to +85	$^\circ\text{C}$
Fan Out	N	MOS Load	15	
		TTL Load	1	

D.C. CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$, $T_a = -20^\circ$ to $+70^\circ\text{C}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Input Voltage	V_{IH}	-	3.6			V
Low Input Voltage	V_{IL}	-			0.8	V
High Output Voltage ⁽¹⁾	V_{OH}	$I_O = -40\mu\text{A}$	4.2			V
Low Output Voltage	V_{OL}	$I_O = 1.6\text{mA}$			0.4	V
OSC ₀ Input Leak Current	I_{IH}	$V_I = V_{DD}/0V$			25	μA
	I_{IL}				-25	
RESET, MODE Leak Current	I_{IH}	$V_I = V_{DD}/0V$			1	μA
	I_{IL}				-50	
Input Leak Current ⁽²⁾	I_{IH}	$V_I = V_{DD}/0V$			1	μA
	I_{IL}				-1	
PA, PB High Output Current	I_{OH}	$V_{OH} = 0.4V$			-1	mA
High Output Current ⁽¹⁾	I_{OH}	$V_{OH} = 2.5V$	-0.25			mA
Low Output Current	I_{OL}	$V_{OL} = 0.4V$	1.6			mA
PF, PG Output Breakdown Voltage	BV_{OH}	$I_O = 10\mu\text{A}$	20			V
Input Capacitance	C_I	$f = 1\text{MHz}$ $T_a = 25^\circ\text{C}$		5		pF
Output Capacitance	C_O	$f = 1\text{MHz}$ $T_a = 25^\circ\text{C}$		7		pF
Current Consumption ⁽³⁾	I_{DD}	$V_I = V_{DD}/0V$		10	200	μA
	I_{DD}	$V_I = V_{DD}/0V$ $f = 4.2\text{MHz}$		1.6	4	mA

Notes: (1) Except PA, PB (see graphs)
 (2) Except OSC₀, RESET, MODE
 (3) Typical Value of V_{DD} is 5V

A.C. CHARACTERISTICS (INTERNAL ROM MODE)

($V_{DD} = 5V \pm 10\%$, $T_a = -40^\circ$ to $+85^\circ C$)

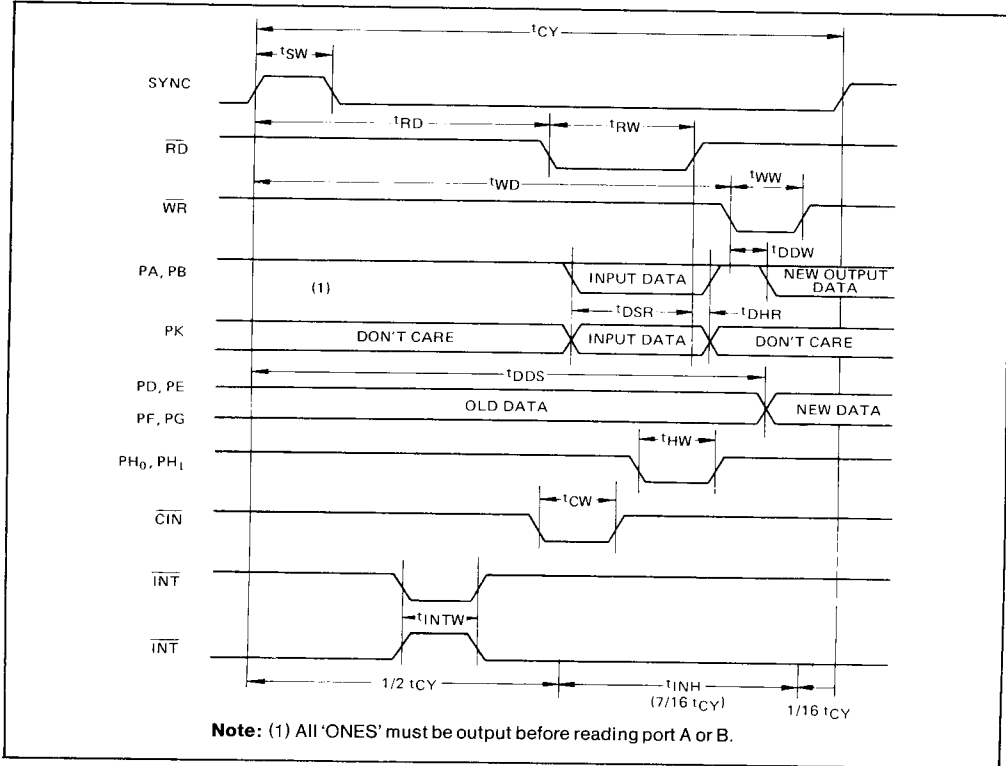
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cycle Time	t_{CY}		7.6			μS
Sync Pulse Width	t_{SW}		0.95			μS
\overline{RD} Pulse Width	t_{RW}		1.9			μS
Sync to \overline{RD}	t_{RD}	$C_L = 50pF$	$1/2 t_{CY} + 0.5$			μS
\overline{WR} Pulse Width	t_{WW}		0.95			μS
Sync to \overline{WR}	t_{WD}	$C_L = 50pF$	$13/16 t_{CY} + 0.5$			μS
Port Input Setup Time	t_{DSR}		$4/16 t_{CY}$			μS
Port Input Hold Time	t_{DHR}		0		0.8	μS
\overline{WR} to New Data Valid	t_{DDW}	PA, PB $C_L = 50pF$			0.8	μS
Sync to New Data Valid	t_{DDS}	PD, PE, PF, PG $C_L = 50pF$			$13/16 t_{CY} + 0.5$	μS
PH_0, PH_1 Input Pulse Width	t_{HW}	(1)	500			nS
\overline{CIN} Input Pulse Width	t_{CW}		250			nS
INT Input Pulse Width	t_{INTW}	(1)	500			nS

Note: (1) The processor logic will ignore the following events:

1. An INT falling edge occurring during T_{INH} of a T_{IH} instruction.
2. A PH_0 or PH_1 low level occurring only during T_{INH} of a T_{HB} instruction.



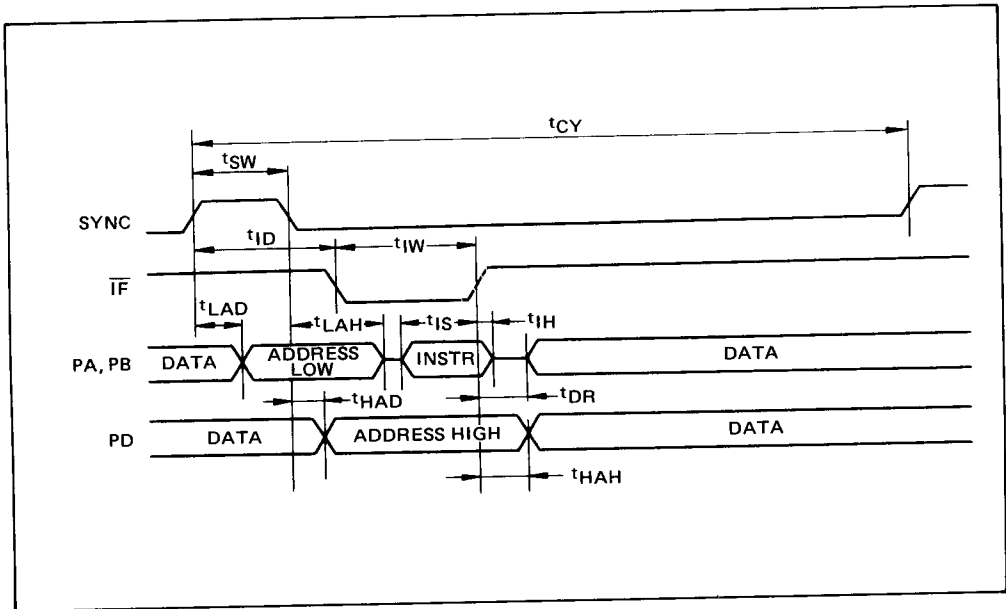
TIMING CHARTS



A.C. CHARACTERISTICS (EXTERNAL ROM MODE)

($V_{DD} = 5V \pm 10\%$, $T_a = -40^\circ$ to $+85^\circ C$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cycle Time	t_{CY}		7.6			μS
Sync Pulse Width	t_{SW}		0.95			μS
\overline{IF} Pulse Width	t_{IW}		1.425			μS
Sync to \overline{IF}	t_{ID}	$C_L = 50pF$	$3/16 t_{CY} + 1$			μS
Address Low Delay	t_{LAD}	$C_L = 50pF$			0.8	μS
Address Low Hold	t_{LAH}		$1/16 t_{CY}$		$1/16 t_{CY} + 1$	μS
Instruction Setup	t_{IS}		$1/16 t_{CY}$			μS
Instruction Hold	t_{IH}				20	nS
Data Recovery	t_{DR}	$C_L = 50pF$	0		0.8	μS
Address High Delay	t_{HAD}	$C_L = 50pF$			0.5	μS
Address High Hold	t_{HAH}		0		0.5	μS



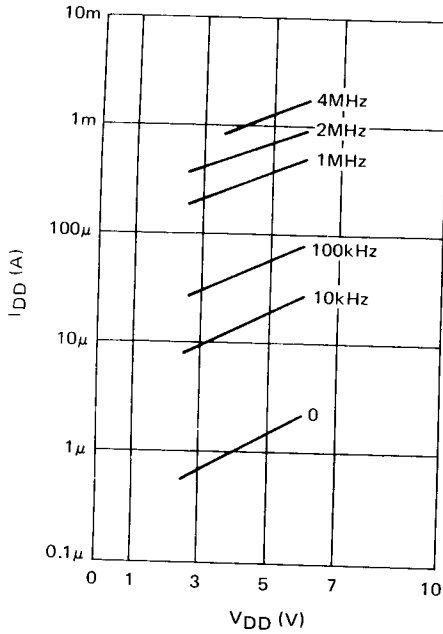
6

Cycle Dependent Timings	4MHz	2MHz	1MHz	500kHz
$1/16 t_{CY}$	$0.5 \mu S$	$1 \mu S$	$2 \mu S$	$4 \mu S$
$1/16 t_{CY} + 1$	$1.5 \mu S$	$2 \mu S$	$3 \mu S$	$5 \mu S$
$3/16 t_{CY} + 1$	$2.5 \mu S$	$4 \mu S$	$7 \mu S$	$13 \mu S$
$4/16 t_{CY} - 1$	$1 \mu S$	$3 \mu S$	$7 \mu S$	$15 \mu S$
$1/2 t_{CY} + 1$	$5 \mu S$	$9 \mu S$	$17 \mu S$	$33 \mu S$
$7/16 t_{CY}$	$3.5 \mu S$	$7 \mu S$	$14 \mu S$	$28 \mu S$
$13/16 t_{CY} + 1$	$7.5 \mu S$	$14 \mu S$	$27 \mu S$	$53 \mu S$

TYPICAL PERFORMANCE CURVES

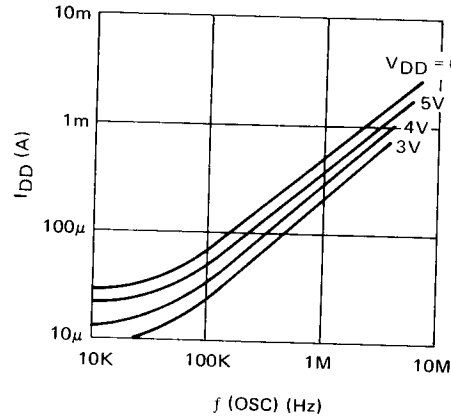
Supply Current vs Supply Voltage

($T_a = 25^\circ\text{C}$, No Load)



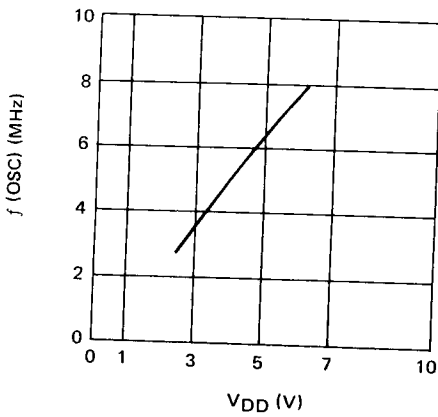
Supply Current vs Oscillator Frequency

($T_a = 25^\circ\text{C}$, No Load)



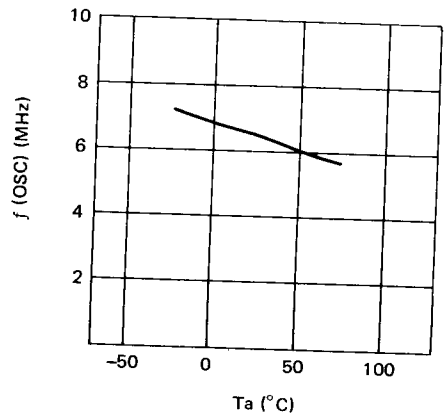
Oscillator Frequency vs Supply Voltage

($T_a = 25^\circ\text{C}$, $C_L = 50\text{pF}$)

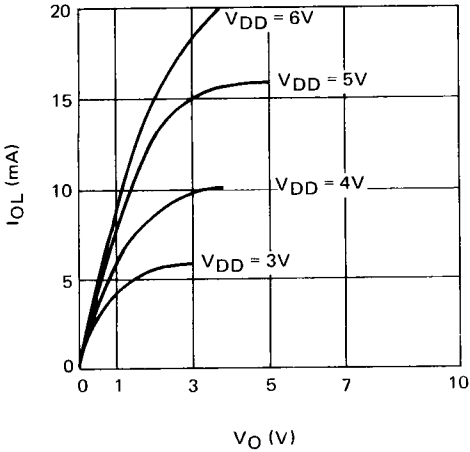


Oscillator Frequency vs Temperature

($C_L = 50\text{pF}$)

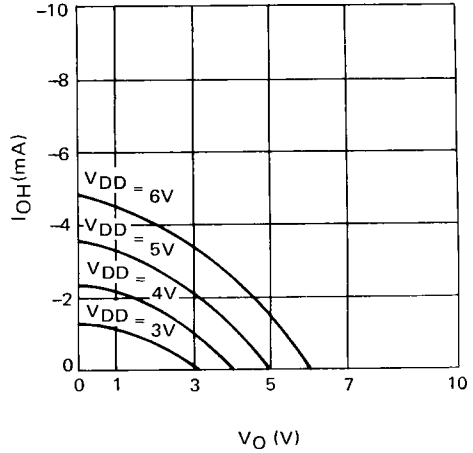


Low Current Out vs Voltage



High Current Out vs Voltage

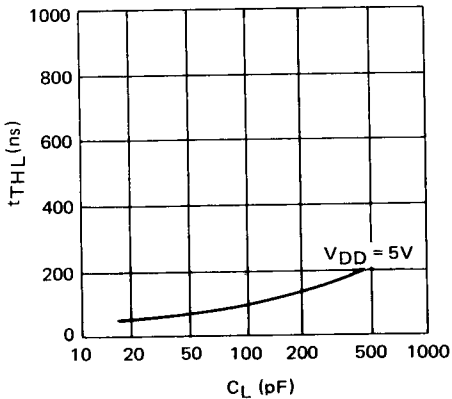
($T_a = 25^\circ C$, Except PA, PB)



6

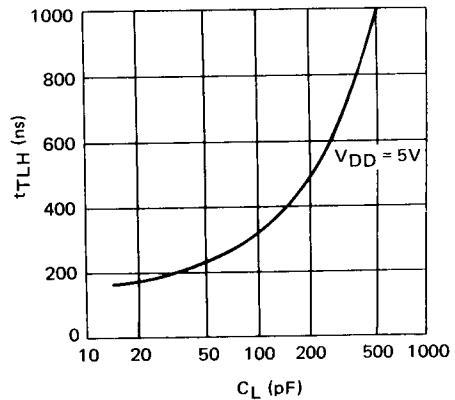
Fall Time vs Load

($T_a = 25^\circ C$, PA, PB, PD, PE, \overline{RD} , \overline{WR} , \overline{IF} , SYNC)

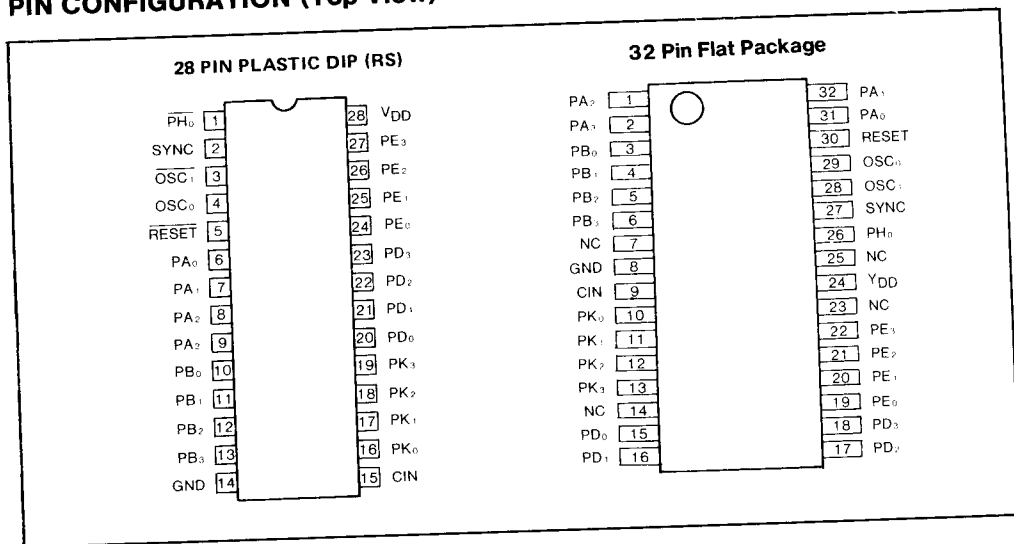


Rise Time vs Load

($T_a = 25^\circ C$, PD, PE, \overline{RD} , \overline{WR} , \overline{IF} , SYNC)



PIN CONFIGURATION (Top View)



PIN DESCRIPTION

Designation	Pin No.	Function
GND	14	Circuit GND potential
VDD	28	Main power source (+5V)
OSC ₀	4	Crystal OSC input, external clock input
OSC ₁	3	Crystal OSC input, external clock output (not TTL compatible)
PA, PB	6 to 13	Quasi-bidirectional ports for 4 bit parallel I/O. Used as a pair for 8 bit I/O.
PD, PE	20 to 27	Output ports for 4 bit parallel output and bit set/reset. Specified by internal port pointer. Bit position specified by set/reset instruction.
PK	16 to 19	4 bit parallel or bit test input port (unlatched)
PH	1	1 bit input port with latched memory (negative level sensitive)
RESET	5	RESET must be low for more than one machine cycle and has priority over every other signal. (see MSM5842 user's manual for initialization sequence)
CIN	15	Negative edge sensitive external input for timer/counter.
SYNC	2	General purpose synchronizing signal output at the beginning of each machine cycle.

6

FUNCTIONAL DESCRIPTION

Program ROM

The MSM5842 will address up to 768 bytes of program ROM. All instructions are byte wide. Only three of the 52 instructions require two bytes of program code. The instructions are routed to a programmed logic array which generates the necessary internal control signals.

Data RAM

Data is organized in 4 bit nibbles. Internal data RAM consists of 32 nibbles and one nibble which is a dedicated general purpose register, W, accessible directly under program control. DATA RAM must be addressed indirectly through the DP (data pointer) register, a five bit pointer (directly accessible by numerous instructions) consisting of a 4 bit DP_L register and a 1 bit DP_H register. Any nibble of internal data RAM can be accessed through the DP registers. Some instructions, automatically change the contents of the DP register allowing efficient array processing.

Input/Output Ports

PA, PB – These two ports are pseudo-bidirectional ports which can be used as simple I/O lines or used as either a 4 bit or 8 bit parallel bus.

PD, PE – These two output ports are addressed indirectly through the ONE BIT port pointer whose contents are changed through certain instructions. These ports are bit (set/reset) addressable.

PK is an input port without a Latch circuit, addressable as a nibble input.

PH is a one bit input port with a Latch circuit, which can be tested and reset under program control.

Timer/Counter

The timer/counter is an 8-bit counter with input is an external signal (CIN). The TM flag is set when the timer/counter generates a carry.

Stack

The stack is a single register for store return-from-subroutine address information, ten bits wide.

Program Counter (PC)

The program counter is ten bits wide.

Accumulator

The accumulator register is the data focal point of the CPU. Approximately one-half the instructions involve the accumulator. Its contents are the source and destination of many ALU operations and port operations. Carry statements (computed GOTOs) are possible using the Jump with Accumulator (JA) instruction.

Flags

The MSM5842 is endowed with the following set of flags.

- Z – zero flag : Indicates that the result of the previous operation was zero
- C – carry : Indicates a carry from the previous operation
- TM – timer flag : Indicates an overflow of the timer/counter register
- H₀ – H₀ memory : Indicates that an input has been detected on H₀ input

INSTRUCTION SET

Mnemonic	Description	Instruction Code								Byte	Cyc	
		7	6	5	4	3	2	1	0			
Load, Store, Read, Clear	CLA	Clear Accumulator	0	0	0	1	0	0	0	0	1	1
	CCL	Clear DP _L	0	0	1	0	0	0	0	0	1	1
	CLH	Clear DP _H	0	1	1	0	0	0	0	0	1	1
	LAI	Load Accumulator with Immediate	0	0	0	1	l ₃	l ₂	l ₁	l ₀	1	1
	LLI	Load DP _L with Immediate	0	0	1	0	l ₃	l ₂	l ₁	l ₀	1	1
	LHI	Load DP _H with Immediate	0	1	1	0	0	0	0	l ₀	1	1
	L	Load Accumulator with Memory	1	0	0	1	0	1	0	0	1	1
	LAL	Load Accumulator with DP _L	0	1	0	1	0	1	0	1	1	1
	LLA	Load DP _L with Accumulator	0	1	0	1	0	1	0	0	1	1
	LAW	Load Accumulator with W Register	1	0	0	0	0	1	0	0	1	1
	SI	Store Accumulator to Memory then Increment DP _L	1	0	0	1	0	0	0	0	1	1
	LWA	Load W Register with Accumulator	1	0	0	0	0	0	0	0	1	1
	LPA	Load Port Pointer with Accumulator	0	1	0	1	1	0	0	0	1	1
	LTI	Load Timer with All Zeros	0	1	1	0	1	0	0	0	1	1

INSTRUCTION SET (CONT.)

Mnemonic	Description	Instruction Code								Byte	Cycle			
		7	6	5	4	3	2	1	0					
Exchange	X	Exchange Accumulator with Memory								1	1			
Increment/Decrement	INA	Increment Accumulator	} Skip if Zero	0	0	0	0	0	0	0	1	1	1	
	INL	Increment DP _L		0	1	0	1	0	1	1	1	1	1	
	INM	Increment Memory		0	1	0	1	1	1	0	1	1	1	
	INW	Increment W Register		1	0	0	0	1	0	0	0	1	1	
	DCA	Decrement Accumulator	} Skip if Not All Ones	0	0	0	0	1	1	1	1	1	1	
	DCL	Decrement DP _L		} Skip if All Ones	0	1	0	1	0	1	1	0	1	1
	DCM	Decrement Memory			0	1	0	1	1	1	0	0	1	1
Logical	CAO	Complement Accumulator of One		0	1	0	1	0	0	0	0	1	1	
	RAL	Rotate Accumulator Left through Carry		0	1	0	0	0	1	1	1	1	1	
Arithmetic	AC	Add Memory to Accumulator with Carry		0	1	0	0	1	1	0	0	1	1	
	AS	Add Memory to Accumulator, Skip if Carry		0	1	0	0	1	1	1	0	1	1	
	AIS	Add Immediate to Accumulator, Skip if Carry		0	0	0	0	<i>l₃</i>	<i>l₂</i>	<i>l₁</i>	<i>l₀</i>	1	1	
	DAS	Decimal adjust Accumulator in Subtraction		0	1	0	1	0	1	0	1	1	1	
	CM	Compare Accumulator with Memory, Skip if Equal		0	1	0	1	1	1	1	0	1	1	
Bit Set/Reset/Test	SMB	Set Memory Bit		1	0	1	1	1	0	<i>l₁</i>	<i>l₀</i>	1	1	
	RMB	Reset Memory Bit		1	0	1	1	1	1	<i>l₁</i>	<i>l₀</i>	1	1	
	TAB	Test Accumulator Bit		1	0	1	0	0	0	<i>l₁</i>	<i>l₀</i>	1	1	
	TMB	Test Memory Bit		1	0	1	0	0	1	<i>l₁</i>	<i>l₀</i>	1	1	
	THB	Test H Port Bit		1	0	1	0	1	1	0	<i>l₀</i>	1	1	
	TTM	Test Timer flag		1	0	1	0	1	1	1	0	1	1	
	TC	Test Carry flag		0	1	0	0	0	0	1	0	1	1	
	SC	Set Carry flag		0	1	0	0	0	0	0	0	1	1	
	RC	Reset Carry flag		0	1	0	0	0	0	0	1	1	1	
Branch/Subroutine	J	Jump		0	0	1	1	0	0	<i>l₉</i>	<i>l₈</i>	2	2	
	JC	Jump in Current Page		1	1	<i>l₅</i>	<i>l₄</i>	<i>l₃</i>	<i>l₂</i>	<i>l₁</i>	<i>l₀</i>	1	1	
	JA	Jump with Accumulator		0	1	0	0	0	0	1	1	1	1	
	CAL	Call Subroutine		0	0	1	1	1	0	<i>l₉</i>	<i>e</i>	2	2	
	RT	Return from Subroutine		0	1	0	1	1	0	0	1	1	2	
Input/Output	OTD	Output Table Data		0	1	1	1	0	0	0	1	1	2	
	OA	Output Accumulator to Port A		0	1	1	1	0	0	1	0	1	1	
	OB	Output Accumulator to Port B		0	1	1	1	0	0	1	1	1	1	
	OP	Output Accumulator to Port P designated Port Pointer		0	1	1	1	0	1	0	0	1	1	
	OPM	Output Memory to Port P designated Port Pointer		0	1	1	1	0	1	1	0	1	1	
	IA	Input Port A in Accumulator		0	1	1	1	1	0	1	0	1	1	
	IB	Input Port B in Accumulator		0	1	1	1	1	0	1	1	1	1	
	IK	Input Port K in Accumulator		0	1	1	1	1	1	0	0	1	1	
Control	NOP	No Operation		0	0	0	0	0	0	0	0	1	1	

6

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.3 to 7	V
Input Voltage	V_I	$T_a = 25^\circ\text{C}$	-0.3 to V_{DD}	V
Storage Temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	1MHz	3 to 6	V
		4.2MHz	4.5 to 5.5	V
Operating Temperature	T_{op}		-40 to 85	$^\circ\text{C}$
Fan Out		MOS Load	40	
		TTL Load	1	

D.C. CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$, $T_a = -40^\circ$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Input Voltage	V_{IH}	-	3.6			V
Low Input Voltage	V_{IL}	-			0.8	V
High Output Voltage (1)	V_{OH}	$I_O = -40\mu\text{A}$	4.2			V
Low Output Voltage	V_{OL}	$I_O = 1.6\text{mA}$			0.45	V
OSC ₀ Input Leak Current	I_{IH}	$V_I = V_{DD}/0V$			25	μA
	I_{IL}				-25	
RESET Leak Current	I_{IH}	$V_I = V_{DD}/0V$			1	μA
	I_{IL}				-20	
Input Leak Current(2)	I_{IH}	$V_I = V_{DD}/0V$			1	μA
	I_{IL}				-1	
PA, PB High Output Current	I_{OH}	$V_{OH} = 0.4V$			-1	mA
High Output Current(1)	I_{OH}	$V_{OH} = 2.5V$	-0.25			mA
Low Output Current	I_{OL}	$V_{OL} = 0.45V$	1.6			mA
Input Capacitance	C_I	$f = 1\text{MHz}$ $T_a = 25^\circ\text{C}$		5		pF
Output Capacitance	C_O	$f = 1\text{MHz}$ $T_a = 25^\circ\text{C}$		7		pF
Current Consumption(3)	I_{DD}	$V_I = V_{DD}/0V$		20	200	μA
	I_{DD}	$V_I = V_{DD}/0V$ $f = 4.2\text{MHz}$		1.5	4	mA

Notes: (1) Except PA, PB (see graphs)

(2) Except OSC₀, RESET

(3) Typical Value of V_{DD} is 5V

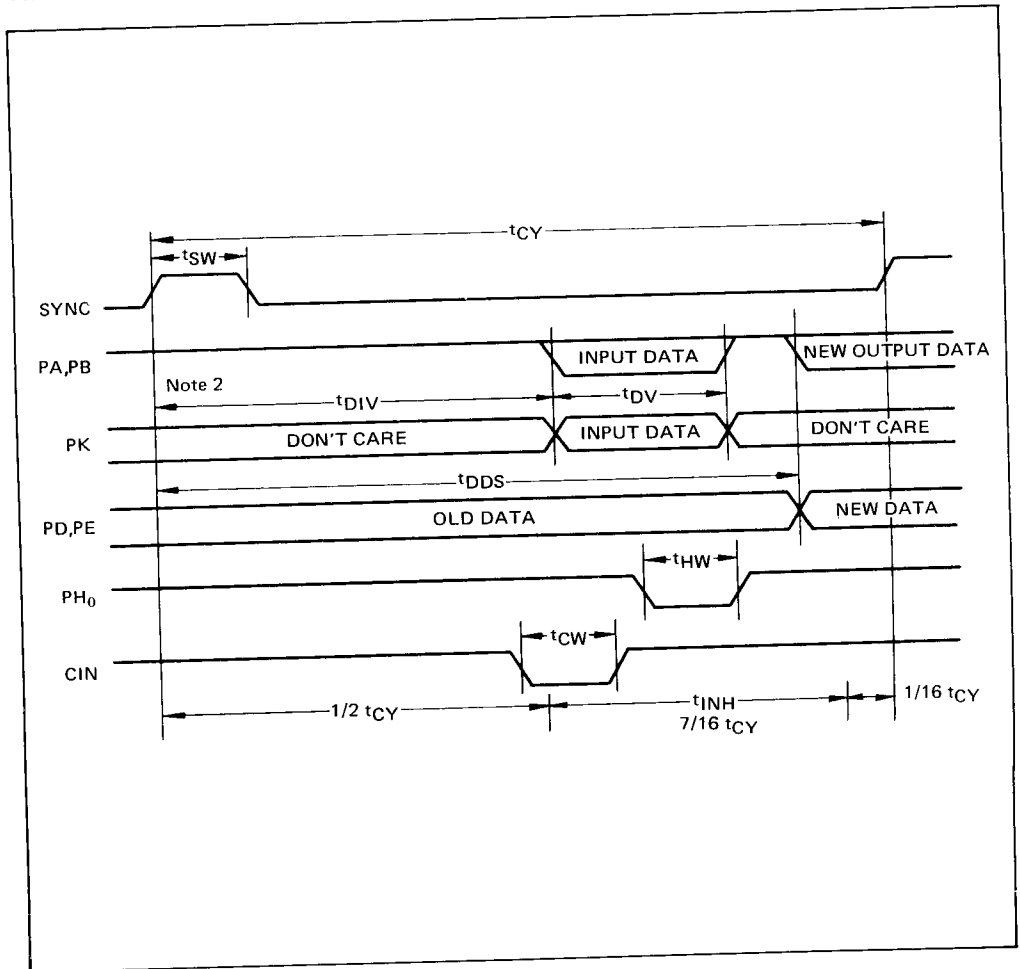
A.C. CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$, $T_a = -40^\circ$ to $+85^\circ C$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cycle Time	t_{CY}	$OSC = 4MHz$	7.6			μS
Sync Pulse Width	t_{SW}		0.95			μS
Port Input Invalid Time	t_{DIV}				$1/2 t_{CY} + 0.5$	μS
Port Input Valid Time	t_{DV}		2			μS
Sync \uparrow to New Data Valid	t_{DDS}	$PD, PE C_L = 50pF$			$13/16 t_{CY} + 0.5$	μS
PH_0 Input Pulse Width	t_{HW}	(1)	250			nS
\overline{CIN} Input Pulse Width	t_{CW}		250			nS

- Notes:** (1) The processor logic may ignore the following event:
 A PH_0 low level occurring only during T_{INH} of a THB instruction.
 (2) All 'ONES' must be output before reading port A or B.

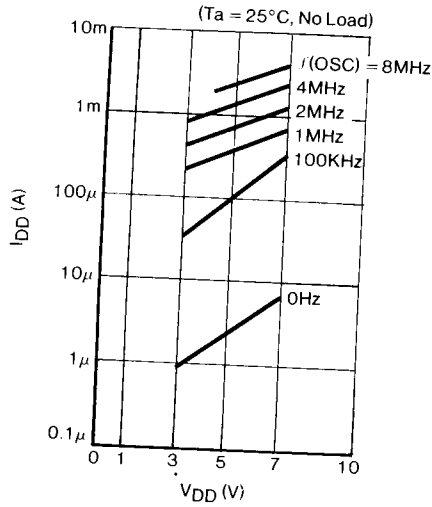
TIMING CHARTS



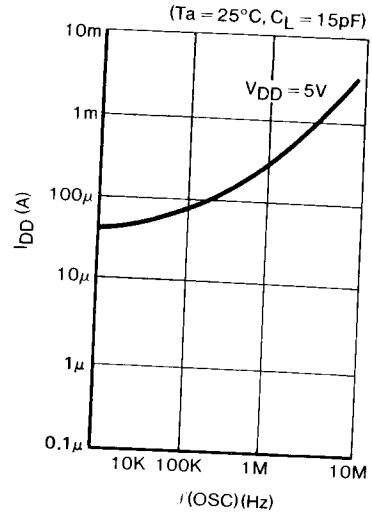
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TYPICAL PERFORMANCE CURVES

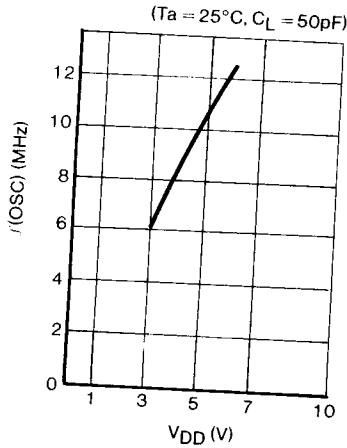
Supply Current vs Supply Voltage



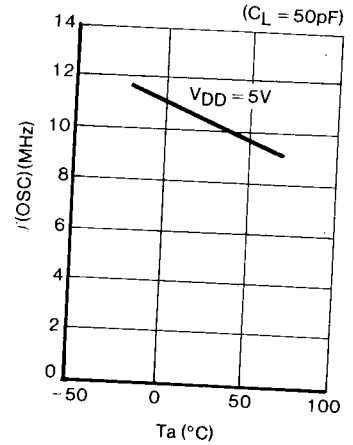
Supply Current vs Oscillator Frequency



Oscillator Frequency vs Supply Voltage

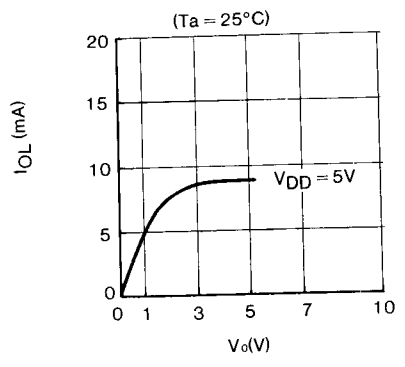


Oscillator Frequency vs Temperature

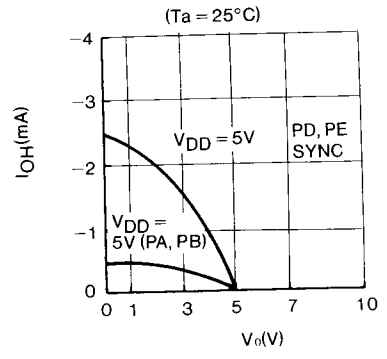


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Low Current Out vs Voltage

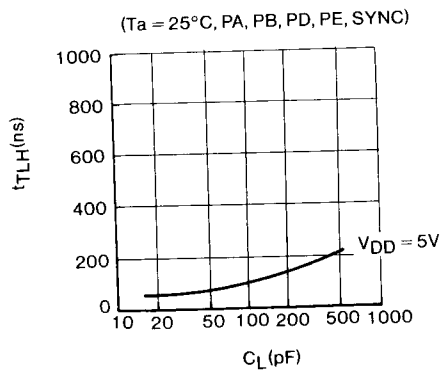


High Current Out vs Voltage

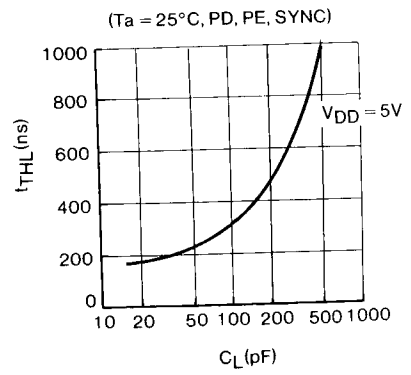


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Fall Time vs Load



Rise Time vs Load



OKI semiconductor

MSM58421

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

The OKI MSM58421 is a low-power, high-performance 4-bit single-chip microcontroller implemented in complementary metal oxide semiconductor technology.

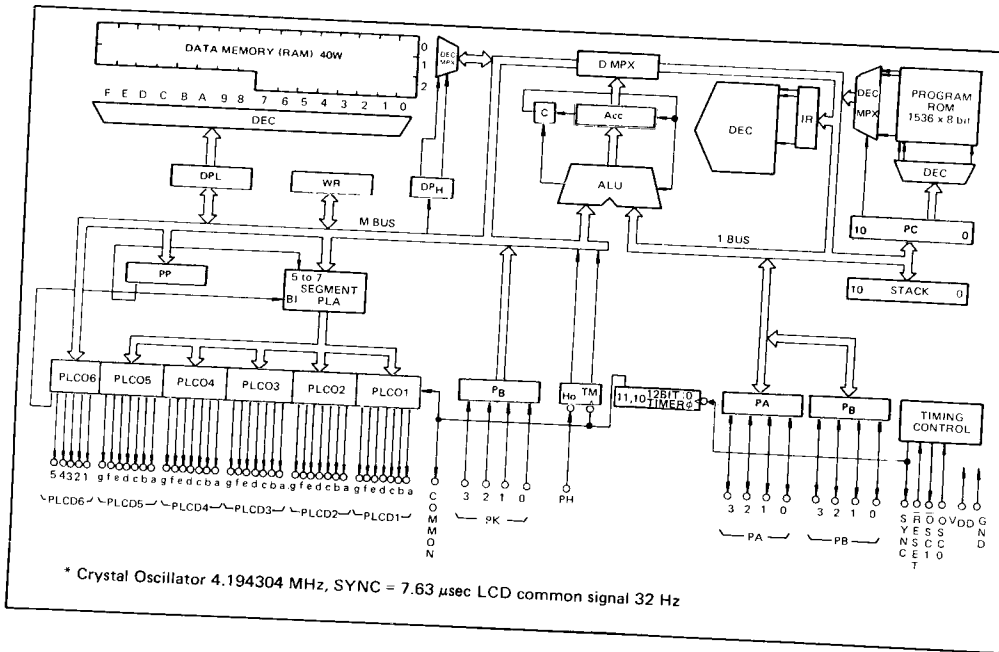
Integrated within this one chip is a 5 digit 7-segment LCD driver and PLA which can change character font for the 7 segments freely under the control of the mask programmable data.

Also integrated in this chip are mask ROM of 1536×8 bits for programming, data RAM of 4096 bits, 13 general-purpose input/output ports, 12-bit timer, and clock oscillator to facilitate easy application to equipment with an LCD display.

FEATURES

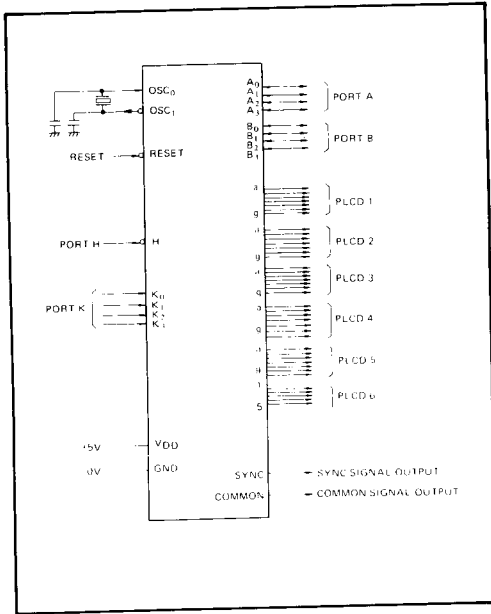
- Low Power Consumption CMOS 4-bit One-Chip Microcomputer
- 100% Static Logic
- 1536×8 bits Mask ROM
- 40×4 bits Data RAM
- 1 Static Register
- Built-in 12-bit Timer (with 32 Hz Common Output)
- All Input Ports Contain Schmitt Trigger Circuits
- 8-bit Interface Bus
- 52 Instructions
- 94% of the 52 Instructions are 1 Byte and 1 Machine Cycle
- Integrated with 13 Input/Output Ports and 4096 Static LCD Driver Circuit
- +5V Single Power Supply, 60-Pin Mold Flat Package
- 7-Segment Character User Programmable Font (32 Words \times 7 Segments)
- Various Functions Changeable under Mask Program Control

FUNCTIONAL BLOCK DIAGRAM

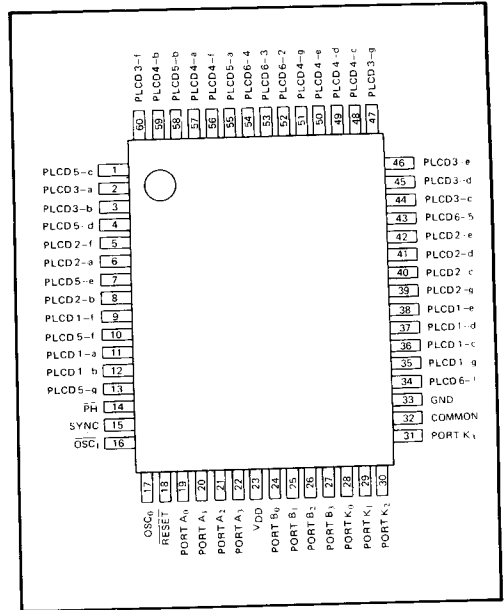


* Crystal Oscillator 4.194304 MHz, SYNC = 7.63 μsec LCD common signal 32 Hz

LOGIC SYMBOL



PIN CONFIGURATION



PIN DESCRIPTION

Designation	Pin No.	Function
GND	33	Circuit GND potential
V _{DD}	23	Main power source (+5V)
OSC ₀	17	Crystal OSC input, external clock input
OSC ₁	16	Crystal OSC input, external clock output (not TTL compatible)
PA, PB	19 to 22 24 to 27	Pseudo-bidirectional ports for 4-bits parallel I/O. To input data from these ports, it is necessary to write "1" to them beforehand. When nothing is applied to their terminals, the content of output ports is written in them, so they can also be used as registers. In addition, it is possible to use them for make 8-bit parallel output depending on instructions.
PK	28 to 31	Input ports for 4-bit parallel input with no latching function.
PH	14	Input port with latching function to be set by negative logical signal. That is, this terminal is set at the time when the negative logical signal is applied to it from the outside. It is reset automatically after execution of the test instruction of this port.
RESET	18	The RESET signal which input has priority over all of other signals and performs the following functions: (1) Resets all bits of the program counter; (2) Resets the timer counter and timer flag; (3) Resets the port pointer; (4) Resets the accumulator; (5) Resets I/O ports PA and PB; (6) Resets the input port PH flag; (7) Initializes the output port PLCD for LCD; (8) Resets the machine cycle to M ₁ . Since the RESET terminal is pulled up to V _{DD} by an internal resistor (approx. 800 kΩ), it is possible to make power ON/reset by connecting it with an external capacitor.

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PIN DESCRIPTION (CONT.)

Designation	Pin No.	Function																																																	
SYNC	15	<p>General-purpose synchronizing signal output. The signal is output at the beginning of each machine cycle. Output constantly, this signal is used also as clock pulse to external units.</p> <p>The cycle of SYNC becomes 32 times that of the original oscillation (8 μs when the clock pulse is 4 MHz).</p>																																																	
PLCD 1 ~ 6	1 to 13 34 to 60	<p>PLCD 1 ~ 6 (Pins 1 ~ 13 and 34 ~ 60) 7-bit and 5-bit parallel output ports, respectively. They are used to direct drive an LCD (static type). Specification of each port is done by the port pointer (PP) as shown in the table below:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="4">Content of PP</th> <th rowspan="2">Port Specified</th> </tr> <tr> <th>b₃</th> <th>b₂</th> <th>b₁</th> <th>b₀</th> </tr> </thead> <tbody> <tr> <td>x</td> <td>0</td> <td>0</td> <td>0</td> <td>PLCD1</td> </tr> <tr> <td>x</td> <td>0</td> <td>0</td> <td>1</td> <td>PLCD2</td> </tr> <tr> <td>x</td> <td>0</td> <td>1</td> <td>0</td> <td>PLCD3</td> </tr> <tr> <td>x</td> <td>0</td> <td>1</td> <td>1</td> <td>PLCD4</td> </tr> <tr> <td>x</td> <td>1</td> <td>0</td> <td>0</td> <td>PLCD5</td> </tr> <tr> <td>x</td> <td>1</td> <td>0</td> <td>1</td> <td>PLCD6 1 ~ 4</td> </tr> <tr> <td>x</td> <td>1</td> <td>1</td> <td>0</td> <td>PLCD6 5 and BI</td> </tr> <tr> <td>x</td> <td>1</td> <td>1</td> <td>1</td> <td>—</td> </tr> </tbody> </table> <p>X: Don't care BI: 7 Segment Decoder PLA Blank Input The data of b₀ of the internal 4-bit bus is written to 5 of PLCD6, and that of b₃ to BI.</p>	Content of PP				Port Specified	b ₃	b ₂	b ₁	b ₀	x	0	0	0	PLCD1	x	0	0	1	PLCD2	x	0	1	0	PLCD3	x	0	1	1	PLCD4	x	1	0	0	PLCD5	x	1	0	1	PLCD6 1 ~ 4	x	1	1	0	PLCD6 5 and BI	x	1	1	1	—
Content of PP				Port Specified																																															
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x	1	1	0	PLCD6 5 and BI																																															
x	1	1	1	—																																															
COMMON	32	<p>COMMON (Pin 32) COMMON output terminal. This output signal is connected to the common electrode of static type LCD. The frequency of the COMMON signal output is given with the following equation:</p> $f(\text{COM}) = f(\text{OSC})/2^{17}$ <p>Where the basic clock f(OSC) is 4.19304 MHz, f(COM) becomes 32 Hz (duty ratio: 50%).</p>																																																	

MASK OPTION TABLE

No.	Port K0	Port K2	Port K3	Common	Timer
	28 pin	30 pin	31 pin	32 pin	
0	K ₀	K ₂	K ₃	32Hz	12 bit
1	K ₀	BUZZER	COMMON	32Hz	12 bit
2	K ₀	BUZZER	K ₁	32Hz	12 bit
3	K ₀	BUZZER	K ₃	64Hz	11 bit
4	K ₀	K ₂	K ₃	64Hz	11 bit
5	K ₀	K ₂	K ₃	128Hz	10 bit
6	K ₁	BUZZER	K ₃	128Hz	10 bit
7	K ₀	K ₂	K ₃	256Hz	9 bit
8	K ₀	K ₂	K ₃	512Hz	8 bit
9	K ₀	BUZZER	K ₁	512Hz	8 bit

f(osc)=4.194304MHz

f (BUZZER)=2048Hz

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Power Supply Voltage	V _{DD}	T _a = 25°C	-0.3 to 7	V
Input Voltage	V _I	T _a = 25°C	-0.3 to V _{DD}	V
Power Dissipation	P _D	T _a = 25°C per 1 package	200	mW
Storage Temperature	T _{stg}		-55 to +150	°C

OPERATING RANGE

Parameter	Symbol	Conditions	Limits	Unit
Power Supply Voltage	V _{DD}	f(OSC) = 0 to 4.2 MHz	4 to 6	V
Operating Temperature	T _{OP}	-	-40 to +85	°C
Fan Out (excluding COM, SEC)	N	MOS Load	15	-
		TTL Load	1	

D.C. CHARACTERISTICS

(V_{DD} = 5V ± 10%, T_a = -40 to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V _{IH}		3.6			V
"L" Input Voltage	V _{IL}				0.8	V
"H" Output Voltage ⁽¹⁾	V _{OH}	I _O = -80μA	V _{DD} -0.1			V
"H" Output Voltage ⁽²⁾	V _{OH}	I _O = -20μA	V _{DD} -0.1			V
"H" Output Voltage ⁽³⁾	V _{OH}	I _O = -40μA	4.2			V
"H" Output Voltage ⁽⁴⁾	V _{OH}	I _O = -15μA	4.2			V
"L" Output Voltage ⁽¹⁾	V _{OL}	I _O = 80μA			0.1	V
"L" Output Voltage ⁽²⁾	V _{OL}	I _O = 20μA			0.1	V
"L" Output Voltage ⁽⁵⁾	V _{OL}	I _O = 1.6mA			0.4	V
OSC ₀ Input Leak Current	I _{IH} /I _{IL}	V _I = V _{DD} /V _I = 0V			10/-10	μA
Input Current ⁽⁶⁾	I _{IH} /I _{IL}	V _I = V _{DD} /V _I = 0V			1/-20	μA
PA PB "H" Output Current	I _{OH}	V _O = 0.4V			-1	mA
"H" Output Current ⁽³⁾	I _{OH}	V _O = 2.5V	-0.25			mA
"L" Output Current ⁽⁴⁾	I _{OL}	V _O = 0.4V	1.6			mA
Input Capacity	C _I	f = 1MHz, T _a = 25°C		5		pF
Output Capacity	C _O	f = 1MHz, T _a = 25°C		7		pF
Current Consumption	I _{DD}	f = 4.194304 MHz, at no load		2	5	mA

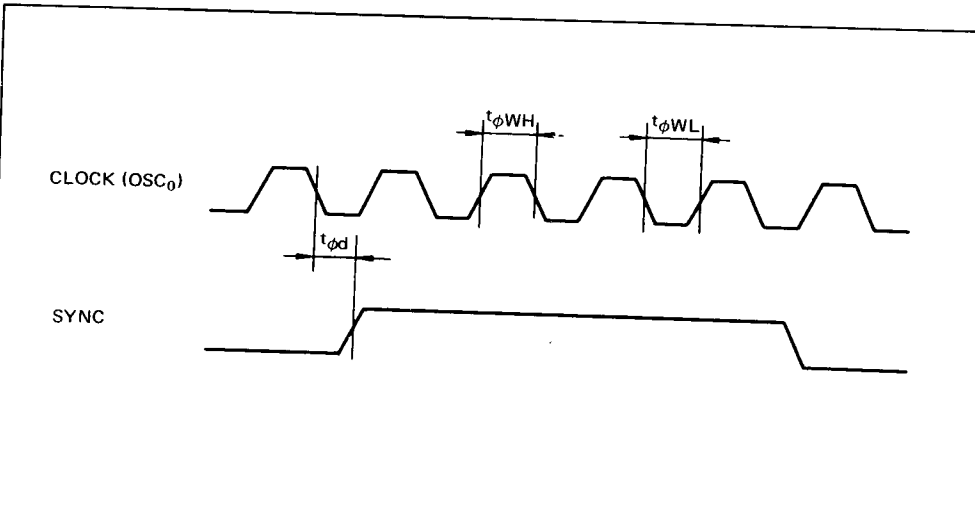
- Notes:** (1) Applied to COMMON
 (2) Applied to SEGMENT
 (3) Applied to SYNC
 (4) Applied to PA, PB
 (5) Applied to SYNC, PA, and PB
 (6) Applied to RESET, PK, and PH

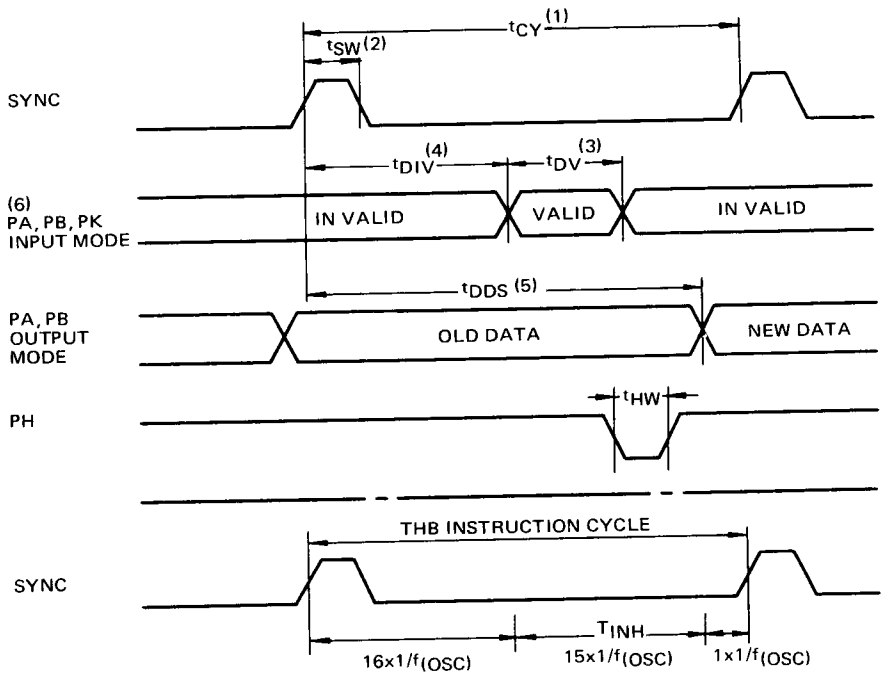
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SWITCHING CHARACTERISTIC

($V_{DD} = 5V \pm 10\%$, $T_a = -40^\circ$ to $+85^\circ C$)

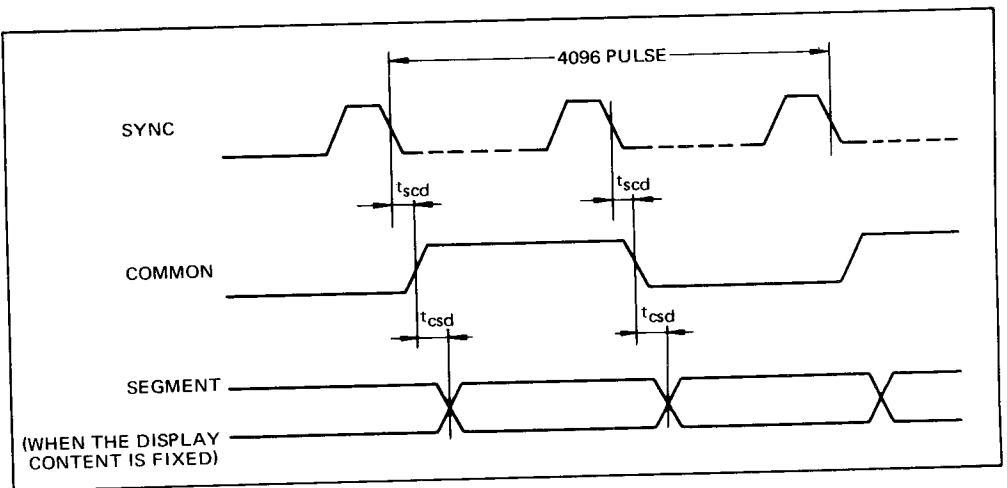
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SYNC Delay Time from Clock (OSC_0)	$t_{\phi d}$	$C_L = 50pF$			800	ns
Clock (OSC_0) Pulse Width	$t_{\phi WH}$ $t_{\phi WL}$		115			ns
Cycle Time	t_{CY}		(1)			μs
SYNC Pulse Width	t_{SW}		(2)			μs
PA PB Data Valid Time PK	t_{DV}	$C_L = 50pF$	(3)			μs
PA PB Data Invalid Time PK	t_{DIV}	$C_L = 50pF$			(4)	μs
Data Delay Time	t_{DDS}	$C_L = 50pF$	500			ns
Port H Set Pulse Width ⁽⁷⁾	t_{HW}		500			ns
COMMON Delay Time from SYNC	t_{SCd}	$C_L = 50pF$			2	μs
SEGMENT Delay Time from COMMON	t_{CSd}	$C_L = 50pF$			1	μs





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- Notes:**
- (1) $t_{CY} = 32 \times 1/f(OSC)$
 - (2) $t_{SW} = 4 \times 1/f(OSC)$
 - (3) $t_{DV} = 8 \times 1/f(OSC)$
 - (4) $t_{DIV} = 16 \times 1/f(OSC) + 0.5 \mu s$
 - (5) $t_{DDS} = 26 \times 1/f(OSC) + 1 \mu s$
 - (6) When data is input from PA or PB, set the contents of PA or PB to "1" prior to reading instruction.
 - (7) At execution of the THB instruction, any input made during a period of T_{INH} ($15 \times 1/f(OSC)$) shown in the above figure may be neglected.



DESCRIPTION OF TERMINALS

GND (Pin 33)

Circuit grounding potential

V_{DD} (Pin 23)

Main power supply

OSC₀ (Pin 17)

Input of internal oscillation circuit at one side of crystal resonator and ceramic vibrator.

OSC₁ (Pin 16)

Output of internal oscillation circuit at the other side of crystal resonator and ceramic vibrator (not TTL compatible)

PA, PB (Pins 19 ~ 22 and 24 ~ 27)

These are quasi-bidirectional ports for 4-bit parallel I/O. To input data from these ports, it is necessary to write "1" to them beforehand. When nothing is applied to their terminals, the content of output ports is written in them, so they can also be used as registers. In addition, it is possible to use them to make an 8-bit parallel output depending on instructions.

PK (Pins 28 ~ 31)

Input ports for 4-bit parallel input with no latching function.

PH (Pin 14)

Input port with latching function to be set by negative logical signal.

This terminal is set at the time when the negative logical signal is applied to it from the outside. It is reset automatically after execution of the test instruction of this port.

RESET (Pin 18)

Reset must be active for greater than 1 machine cycle.

The RESET signal, when input, has priority over all of other signals and performs the following functions:

- (1) Resets all bits of the program counter;
- (2) Resets the timer counter and timer flag;
- (3) Resets the port pointer;
- (4) Resets the accumulator;
- (5) Resets I/O ports PA and PB;
- (6) Resets the input port PH flag;
- (7) Initializes the output port PLCD for LCD; and
- (8) Resets the machine cycle to M₁.

Since the $\overline{\text{RESET}}$ terminal is pulled up to V_{DD} by an internal resistor (approx. 800kΩ), it is possible to activate power ON/reset by connecting it to an external capacitor.

SYNC (Pin 15)

This is a general-purpose synchronous signal output. The signal is output at the beginning of each machine cycle. Output constant of this signal is used also as clock pulse to external devices.

The cycle of SYNC becomes 32 times that of the original oscillation (8μs when the clock pulse is 4MHz).

PLCD 1 ~ 6 (Pins 1 ~ 13 and 34 ~ 60)

These are 7-bit and 5-bit parallel output ports, respectively. They are used to drive an LCD (static type). Specification of each port is done by the port pointer (PP) as shown in the table below;

	Content of PP				Port Specified
	b ₃	b ₂	b ₁	b ₀	
x	0	0	0	0	PLCD1
x	0	0	0	1	PLCD2
x	0	1	0	0	PLCD3
x	0	1	1	1	PLCD4
x	1	0	0	0	PLCD5
x	1	0	1	1	PLCD6 ~ 4
x	1	1	0	0	PLCD6 5 and BI
x	1	1	1	1	---

X: Don't Care

BI: 7 Segment Decoder PLA Blank Input

The data of b₀ of the internal 4-bit bus is written to b₀ of PLCD6, and that of b₃ to BI.

COMMON (Pin 32)

This is a COMMON output terminal. The output signal is connected to the common electrode of static type LCD. The frequency of the COMMON signal output is given with the following equation:

$$f(\text{COM}) = f(\text{OSC})/2^{17}$$

Where the basic clock f(OSC) is 4.19304 MHz, f(COM) becomes 32 Hz (duty ratio: 50%).

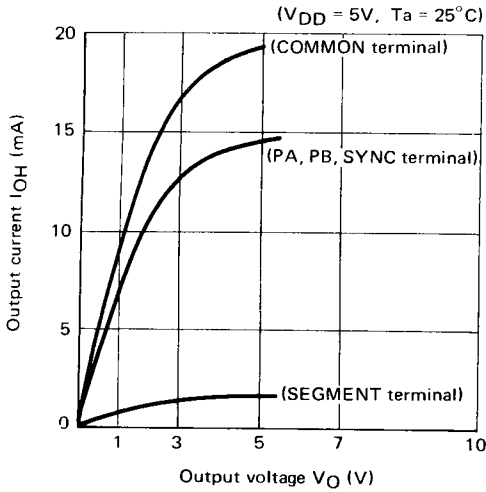
INSTRUCTIONS LIST

Mnemonic	Description	Instruction Code								Byte	Cycle
		7	6	5	4	3	2	1	0		
CLA	Clear Accumulator	0	0	0	1	0	0	0	0	1	1
CLL	Clear DP _L	0	0	1	0	0	0	0	0	1	1
CLH	Clear DP _H	0	1	1	0	0	0	0	0	1	1
LAI	Load Accumulator with Immediate	0	0	0	1	l ₃	l ₂	l ₁	l ₀	1	1
LLI	Load DP _L with Immediate	0	0	1	0	l ₃	l ₂	l ₁	l ₀	1	1
LHI	Load DP _H with Immediate	0	1	1	0	l ₀	l ₁	l ₀	1	1	
L	Load Accumulator with Memory	1	0	0	1	0	1	0	0	1	1
LAL	Load Accumulator with DP _L	0	1	0	1	0	1	0	1	1	1
LLA	Load DP _L with Accumulator	0	1	0	1	0	1	0	0	1	1
LAW	Load Accumulator with W Register	1	0	0	0	0	1	0	0	1	1
SI	Store Accumulator to Memory then Increment DP _L	1	0	0	1	0	0	0	0	1	1
LWA	Load W Register with Accumulator	1	0	0	0	0	0	0	0	1	1
LPA	Load Port Pointer with Accumulator	0	1	0	1	1	0	0	0	1	1
LTI	Load Timer with Immediate "0" (Clear Timer & TMF)	0	1	1	0	1	0	0	0	1	1
X	Exchange Accumulator with Memory	1	0	0	1	1	0	0	0	1	1
INA	Increment Accumulator	0	0	0	0	0	0	0	1	1	1
INL	Increment DP _L	0	1	0	1	0	1	1	1	1	1
INM	Increment Memory	0	1	0	1	1	1	0	1	1	1
INW	Increment W Register	1	0	0	0	1	0	0	0	1	1
DCA	Decrement Accumulator	0	0	0	0	1	1	1	1	1	1
DCL	Decrement DP _L	0	1	0	1	0	1	1	0	1	1
DCM	Decrement Memory	0	1	0	1	1	1	0	0	1	1
CAO	Complement Accumulator of One	0	1	0	1	0	0	0	0	1	1
RAL	Rotate Accumulator Left through Carry	0	1	0	0	0	1	1	1	1	1
AC	Add Memory to Accumulator with Carry	0	1	0	0	1	1	0	0	1	1
AS	Add Memory to Accumulator, Skip if Carry	0	1	0	0	1	1	0	1	1	1
AIS	Add Immediate to Accumulator, Skip if Carry	0	0	0	0	l ₃	l ₂	l ₁	l ₀	1	1
DAS	Decimal adjust Accumulator in Subtraction	0	1	0	1	1	0	1	0	1	1
CM	Compare Accumulator with Memory	0	1	0	1	1	1	0	1	1	1
SMB	Set Memory Bit	1	0	1	1	1	0	l ₁	l ₀	1	1
RMB	Reset Memory Bit	1	0	1	1	1	1	l ₁	l ₀	1	1
TAB	Test Accumulator Bit	1	0	1	0	0	0	l ₁	l ₀	1	1
TMB	Test Memory Bit	1	0	1	0	0	1	l ₁	l ₀	1	1
THB	Test H Port Bit	1	0	1	0	1	1	0	0	1	1
TTM	Test Time flag	1	0	1	0	1	1	1	0	1	1
TC	Test Carry flag	0	1	0	0	0	0	1	0	1	1
SC	Set Carry flag	0	1	0	0	0	0	0	0	1	1
RC	Reset Carry flag	0	1	0	0	0	0	0	1	1	1
J	Jump	0	0	1	1	0	l ₁₀	l ₉	l ₈	2	2
JC	Jump in Current Page	1	1	l ₅	l ₄	l ₃	l ₂	l ₁	l ₀	1	1
JA	Jump with Accumulator	0	1	0	0	0	0	1	1	1	1
CAL	Call Subroutine	0	0	1	1	1	l ₁₀	l ₉	l ₈	2	2
RT	Return from Subroutine	0	1	0	1	1	0	0	1	1	1
OTD	Output Table Data	0	1	1	1	0	0	0	1	1~15	2
OA	Output Accumulator to Port A	0	1	1	1	0	0	1	0	1	1
OB	Output Accumulator to Port B	0	1	1	1	0	0	1	1	1	1
OP	Output Accumulator to Port designated Port Pointer	0	1	1	1	0	1	0	0	1	1
OPM	Output Memory to Port P designated Port Pointer	0	1	1	1	0	1	1	0	1	1
IA	Input Port A in Accumulator	0	1	1	1	1	0	1	0	1	1
IB	Input Port B in Accumulator	0	1	1	1	1	0	1	1	1	1
IK	Input Port K in Accumulator	0	1	1	1	1	1	0	0	1	1
NOP	No Operation	0	0	0	0	0	0	0	0	1	1

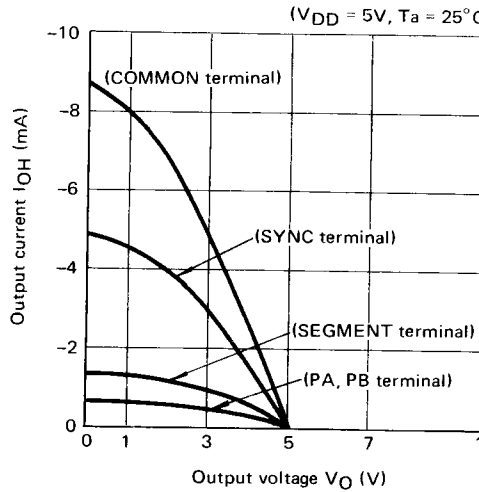
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TYPICAL PERFORMANCE CURVES

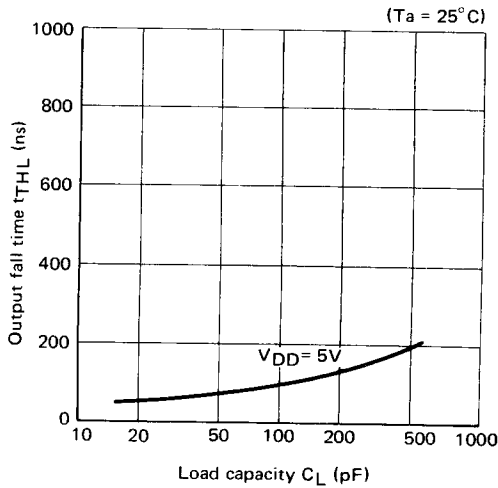
Output Current (I_{OL}) TYP



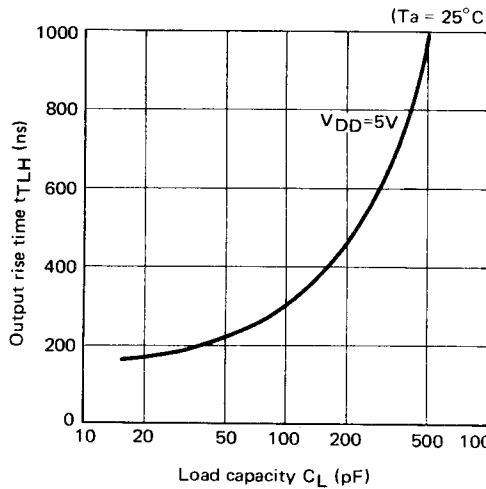
Output Current (I_{OH}) TYP



$t_{THL} - C_L$ Characteristic TYP

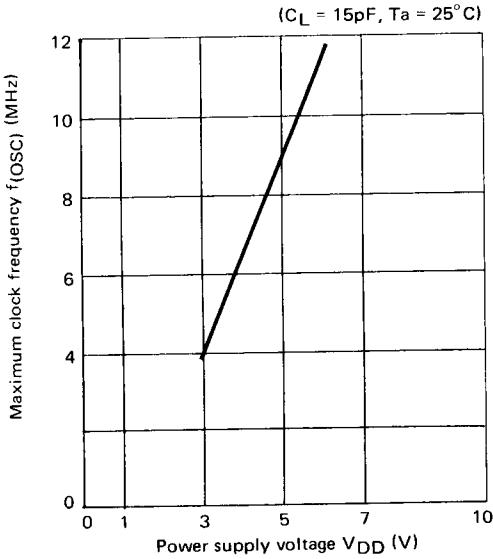


$t_{TLH} - C_L$ Characteristic TYP

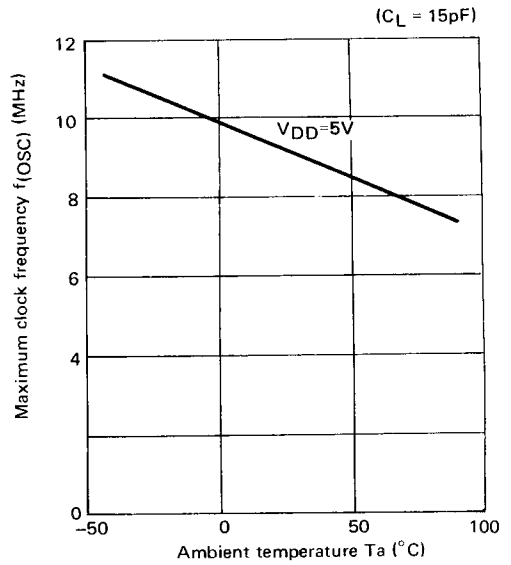


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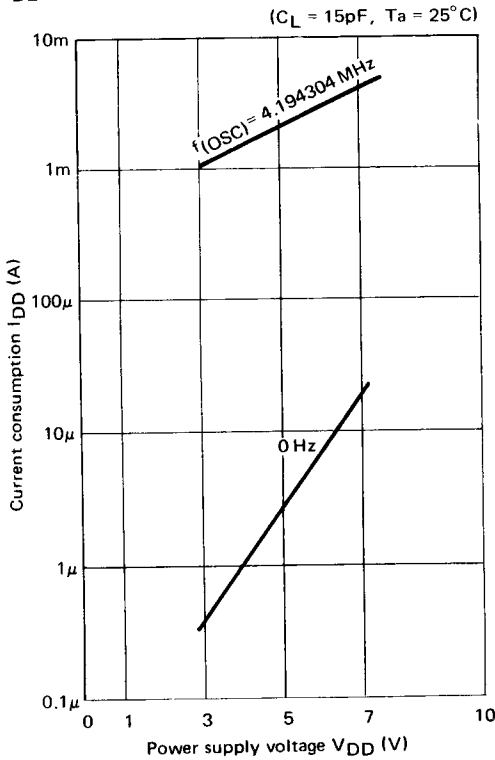
f(OSC) – V_{DD} Characteristic TYP



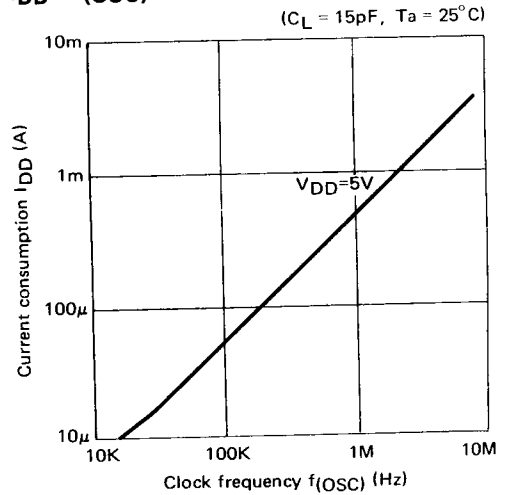
f(OSC) – T_a Characteristic TYP



I_{DD} – V_{DD} Characteristic TYP



I_{DD} – f(OSC) Characteristic TYP



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MSM58422

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER WITH FLT DRIVER

GENERAL DESCRIPTION

OKI's MSM58422 is a low-power, high-performance 4-bit single-chip microcontroller implemented in complementary metal oxide semiconductor technology.

Integrated within the one chip is a mask ROM of 1536×8 bits, RAM of 40×4 bits, 10 input/output ports 11-bit timer-counter, clock oscillator, 4-bit parallel arithmetic circuit, 40 static FLT drivers etc.

MSM58422 has an instruction set which consists of 4-bit arithmetic instructions, Boolean (bit manipulation instructions (bit-set, bit-reset, bit-test), data input/output instructions, and 8-bit code translation (Table data out) instructions.

Also the pseudo-bilateral ports are used for connection to the buses of other 8-bit systems.

FEATURES

- Low Power Consumption CMOS 4-bit One-Chip Microcomputer
- 100% Static Logic
- 1536×8 bits MASK ROM
- 8-bit Interface Bus
- 1 Stack Register
- 52 Instructions
- +5V Single Power Supply
- 60-Pin Flat Package
- Built-in 11-bit Timer
- 94% of the 52 Instructions and 1 Byte and 1 Machine Cycle
- Integrated with 10 Input/Output Ports and 40 Static FLT Driver Circuit
- PK and PH Input contain Schmidt Trigger Circuits

FUNCTIONAL BLOCK DIAGRAM

