OTI012 STANDARD MODE PINOUT
Standard Mode Pin-Out Assignment if pin 28 tied to Vss

Pin	Pin Name	Type	Comments	Pin	Pin Name	Type	Comments
1	Vss	P	Vss	41	Vss	P	Vss
2	RAD[6]	O	RA6	42	UD[3]	B	D3
3	RAD[7]	O	RA7	43	UD[4]	B	D4
4	RAD[8]	O	RA8	44	UD[5]	B	D5
5	RAD[9]	O	RA9	45	UD[6]	B	D6
6	RAD[10]	O	RA10	46	UD[7]	B	D7
7	RAD[11]	O	RA11	47	URS	I	RS
8	RAD[12]	O	RA12	48	URDB	I	/RD
9	RAD[13]	O	RA13	49	UWRB	I	/WR
10	RAD[14]	O	RA14	50	UCSB	I	/CS
11	RAD[15]	O	RA15	51	UNITB	O	/INT
12	RWEB	O	/RWE	52	Vss	P	Vss
13	Vss	P	Vss	53	RESETB	I	/RESET
14	ROEB	O	/ROE	54	HCSB	I	/ENABLE
15	N/C	-	Unused	55	HWRB	I	/HWR
16	RD[7]	B	IO8	56	HRDB	I	/HRD
17	RD[6]	B	IO7	57	HCMDB	I	/CMD
18	RD[5]	B	IO6	58	HWAITB	O	/WAIT
19	RD[4]	B	IO5	59	RDTENB	O	/DTEN
20	RD[3]	B	IO4	60	HSTENB	O	/STEN
21	RD[2]	B	IO3	61	HEOPB	O	/EOP
22	RD[1]	B	IO2	62	RCSB	O	/RCS
23	RD[0]	B	IO1	63	-	O	Unused
24	Vss	P	Vss	64	Vss	P	Vss
25	XIN	I	XTAL	65	HD[7]	B	HD7
26	XOUT	O	XTAL	66	HD[6]	B	HD6
27	TEST1	I	TESTA	67	HD[5]	B	HD5
28	ENHANCE	I	0-Standard 1-Enhanced	68	HD[4]	B	HD4
29	DCSEL	I	CSEL	69	HD[3]	B	HD3
30	DLMSEL	I	LMSL	70	HD[2]	B	HD2
31	Vdd	P	Vdd	71	HD[1]	B	HD1
32	DLRCK	I	LRCK	72	HD[0]	B	HD0
33	DSDATA	I	SDATA	73	Vdd	P	Vdd
34	DBCK	I	BCK	74	HSELDRQB	I	/SELDRQ
35	N/C	-	Unused	75	RAD[0]	O	RA0
36	DC2PO	I	C2PO	76	RAD[1]	O	RA1
37	MCK	O	MCK	77	RAD[2]	O	RA2
38	UD[0]	B	D0	78	RAD[3]	O	RA3
39	UD[1]	B	D1	79	RAD[4]	O	RA4
40	UD[2]	B	D2	80	RAD[5]	O	RA5

OTI012 ENHANCED MODE PIN-OUT ASSIGNMENT
Enhanced Mode Pin-Out Assignment if pin28 is tied to Vdd

Pin	Pin Name	Type	Comments	Pin	Pin Name	Type	Comments
1	Vss	P	Vss	41	Vss	P	Vss
2	RAD[6]	O	RA6	42	UD[3]	B	D3
3	RAD[7]	O	RA7	43	UD[4]	B	D4
4	RAD[8]	O	RA8	44	UD[5]	B	D5
5	RAD[9]	O	RA9	45	UD[6]	B	D6
6	RAD[10]	O	RA10	46	UD[7]	B	D7
7	RAD[11]	O	RA11	47	URS	I	RS
8	RAD[12]	O	RA12	48	URDB	I	/RD
9	RAD[13]	O	RA13	49	UWRB	I	/WR
10	RAD[14]	O	RA14	50	UCSB	I	/CS
11	RAD[15]	O	RA15	51	UNITB	O	/INT
12	RWEB	O	/RWE	52	Vss	P	Vss
13	Vss	P	Vss	53	RESETB	I	/RESET
14	ROEB	O	/ROE	54	HCSB	I	/ENABLE
15	HA1	I	Host Address 1	55	HWRB	I	/HWR
16	RD[7]	B	IO8	56	HRDB	I	/HRD
17	RD[6]	B	IO7	57	HA0	I	Host Address 0
18	RD[5]	B	IO6	58	HDRQ	O	Host Data Request
19	RD[4]	B	IO5	59	HDRQEB	O	Host DRQ Enable
20	RD[3]	B	IO4	60	HFBLB	O	Host First Byte Latch
21	RD[2]	B	IO3	61	HFBC	O	Host First Byte Cycle
22	RD[1]	B	IO2	62	RCSB	O	/RCS
23	RD[0]	B	IO1	63	HRSTB	O	Reset from Host
24	Vss	P	Vss	64	Vss	P	Vss
25	XIN	I	XTAL	65	HD[7]	B	HD7
26	XOUT	O	XTAL	66	HD[6]	B	HD6
27	EJECT	I	Disk Door Eject Switch	67	HD[5]	B	HD5
28	ENHANCE	I	0-Standard 1-Enhanced	68	HD[4]	B	HD4
29	DCSEL	I	CSEL	69	HD[3]	B	HD3
30	DLMSEL	I	LMSL	70	HD[2]	B	HD2
31	Vdd	P	Vdd	71	HD[1]	B	HD1
32	DLRCK	I	LRCK	72	HD[0]	B	HD0
33	DSDATA	I	SDATA	73	Vdd	P	Vdd
34	DBCK	I	BCK	74	HSELDRQB	I	/SELDRQ
35	HDACKB	I	Host Data Acknowledge From DMA controller	75	RAD[0]	O	RA0
36	DC2PO	I	C2PO	76	RAD[1]	O	RA1
37	MCK	O	MCK	77	RAD[2]	O	RA2
38	UD[0]	B	D0	78	RAD[3]	O	RA3
39	UD[1]	B	D1	79	RAD[4]	O	RA4
40	UD[2]	B	D2	80	RAD[5]	O	RA5