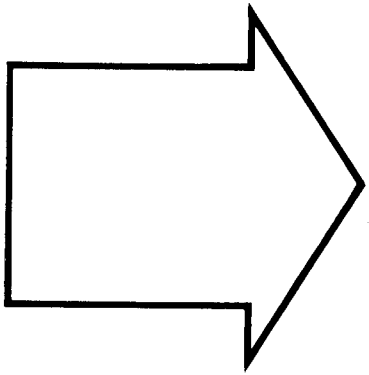


Table of Contents

PAL® (Programmable Array Logic) Devices
HAL® (Hard Array Logic) Devices

Features/Benefits

- Reduces SSI/MSI chip count greater than 4 to 1
- Saves space with SKINNYDIP® and PLCC packages
- Reduces IC inventories substantially
- Expedites and simplifies prototyping and board layout
- PALASM® 2 silicon compiler provides easy design entry
- Security fuse reduces possibility of copying by competitors

Description

The PAL device family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The HAL device family utilizes standard Low-Power Schottky TTL process and automated mask pattern generation directly from logic equations to provide a semi-custom gate array for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The PAL device lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL/HAL device transfer function is the familiar sum of products. Like the PROM, the PAL device has a single array of fusible links. Unlike the PROM, the PAL device is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array).

In addition the PAL/HAL device provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability
- Exclusive-OR gates

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D-type flip-flops which are loaded on the low-to-high transition of the clock. PAL/HAL device Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets. PALASM 2 software automatically generates a similar diagram, called the fuse plot.

The entire PAL device family is programmed using inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL device is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

To design a HAL, the user first programs and debugs a PAL device using PALASM 2 software and the "PAL DEVICE DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer-processed and assigned a bit pattern number, e.g., H01234.

Monolithic Memories will provide a PAL device sample for customer qualification. The user then submits a purchase order for a HAL of the specified bit pattern number, e.g., HAL18L4 H01234. For details on ordering HAL devices, please refer to the brochure, *ProPAL, HAL, and ZHAL Devices: The Logical Solutions for Volume Programmable Logic*, available from Monolithic Memories.

Register Bypass (MegaPAL Devices)

Outputs within a bank must either be all registered or all combinatorial. Whether or not a bank of registers is bypassed depends on how the outputs are defined in the equations. A colon followed by an equal sign [: =] specifies a registered output with feedback which is updated after the low-to-high transition of the clock. An equal sign [=] defines a combinatorial output which bypasses the register. Registers are bypassed in banks of eight. Bypassing a bank of registers eliminates the feedback lines for those outputs.

Output Polarity

Output polarity is defined by comparison of the pin list and the equations. If the logic sense of a specific output in the pin list is different from the logic sense of that output as defined by its equation, the output is inverted or active low polarity. If the logic sense of a specific output in the pin list is the same as the logic sense of that output as defined by its equation, the output is active high polarity. Note that the P, RA, RS, and MegaPAL devices have programmable output polarity.

Product Term Sharing (RS, MegaPAL Devices)

The basic configuration is sixteen product terms shared between two output cells. For a typical output pair, each product term can be used by either output; but, since product term sharing is exclusive, a product term can be used by only one output, not both. If equations call for an output pair to use the same product term, two product terms are generated, one for each output. This should be taken into account when writing equations. PAL device assemblers configure product terms automatically.

Product Term Editing

A unique feature of product term sharing is the ability to edit the design after the device has been programmed. Without this feature, a new PAL device had to be programmed if the user needed to change his design. Product term editing allows the user to delete an unwanted product term and reprogram a previously unused product term to the desired fuse pattern. This feature is made possible by the product term sharing architecture. Since each product term can be routed to either output in a given pair by selecting one of two steering fuses, it is possible to blow both of the steering fuses thereby completely disabling that product term. Once disabled, that product term is powered down, saving typically 0.25mA. The desired change may now be programmed into one of the previously unused product terms corresponding to that output pair. Additional edits can be made as long as there are unused product terms for the output in question.

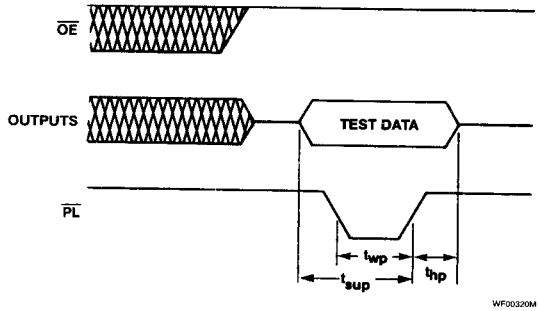
PRESET Feature (PAL64R32 only)

Register banks of eight may be PRESET to all highs on the outputs by setting the PRESET pin (PS) to a Low level. Note from the Logic Diagram that when the state of an output is High, the state of the register is Low due to the inverting tri-state buffer.

TTL-Level Preload Features (RA, MegaPAL Devices)

Preload pins have been added to enable the testability of each state in state-machine design. Typically, for a modulo-n counter or a state machine there are many unreachable states for the registers. These states, and the logic which controls them are untestable without a way to "set-in" the desired starting state of the registers. In addition, long test sequences are sometimes needed to test a state machine simply to reach those starting states which are legal. Since complete logic verification is needed to ensure the proper exit from "illegal" or unused states, a way to enter these states must be provided. The ability to preload a given bank of registers is provided in this device.

To use the preload feature, several steps must be followed. First, a high level on an assertive-low output enable pin disables the outputs for that bank of registers. Next, the data to be loaded is presented at the output pins. This data is then loaded into the register by placing a low level on the PRELOAD pin, PRELOAD is asynchronous with respect to the clock.



Programmable Set and Reset (RA Family only)

In each SMAC, two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1. If the reset product line is high, the register output becomes a logic 0. The operation of the programmable set and reset overrides the clock. Note that set and reset are in reference to the register, independent of polarity.

Individually Programmable Register Bypass (RA Family only)

If both the set and reset product lines are high, the sum-of-products bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

Programmable Clock (RA Family only)

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.

Small 20 Series

	INPUTS	OUTPUTS	POLARITY	STANDARD		HALF POWER	
				t_{PD} (ns)	I_{CC} (mA)	t_{PD} (ns)	I_{CC} (mA)
PAL10H8	10	8	HIGH	35	90	65	40
PAL12H6	12	6	HIGH	35	90	65	40
PAL14H4	14	4	HIGH	35	90	65	40
PAL16H2	16	2	HIGH	35	90	65	40
PAL16C1	16	2	BOTH	40	90	65	40
PAL10L8	10	8	LOW	35	90	65	40
PAL12L6	12	6	LOW	35	90	65	40
PAL14L4	14	4	LOW	35	90	65	40
PAL16L2	16	2	LOW	35	90	65	40

Description

The Small 20 Series is made up of nine combinatorial 20-pin PAL devices. They implement simple combinatorial logic, with no feedback. Each has sixteen product terms total, divided among the outputs, with two to sixteen product terms per output.

Polarity

Both active high and active low versions are available for each architecture. The 16C1 offers both polarities of its single output.

Performance

Two performance options are available. The standard series has a propagation delay (tpd) of 35 nanoseconds (ns), except for the 16C1 at 40ns. Standard supply current is 90 milliamps (mA). The half-power version consumes only 40mA, with a speed of 65ns.

DIP Pinouts

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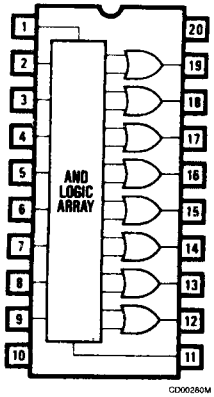

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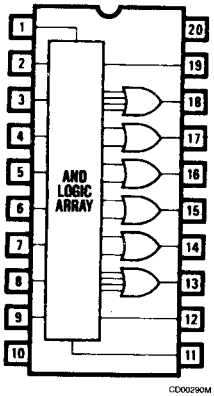

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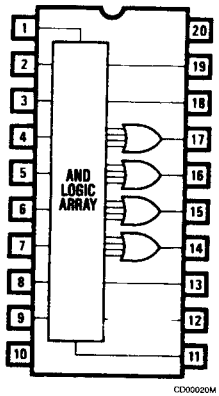

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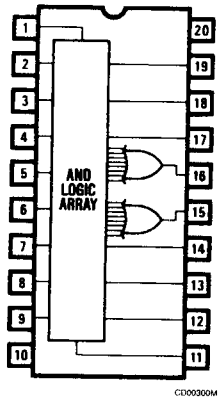

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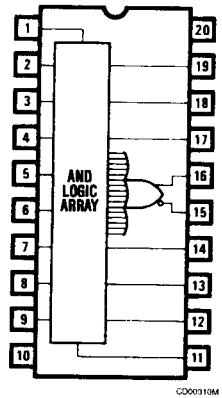

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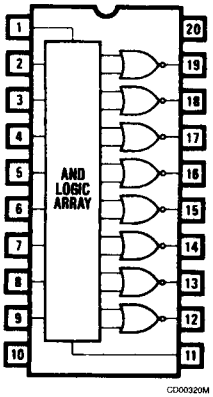

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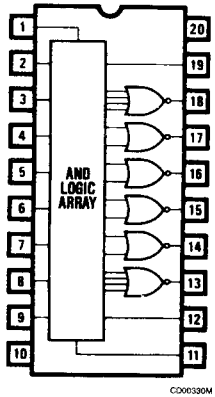

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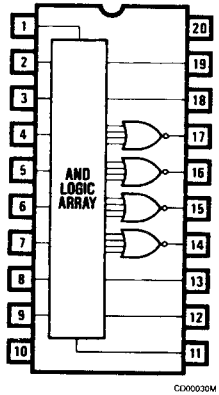

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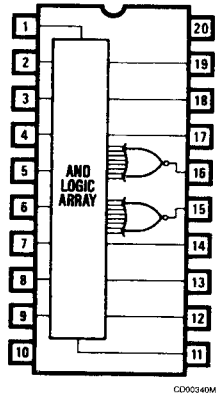

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PLCC Pinouts

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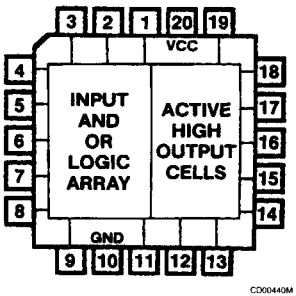

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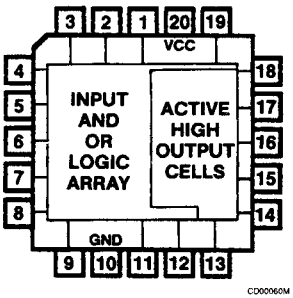

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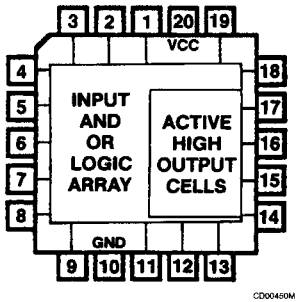

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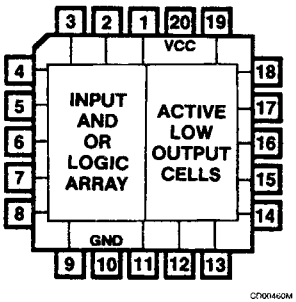

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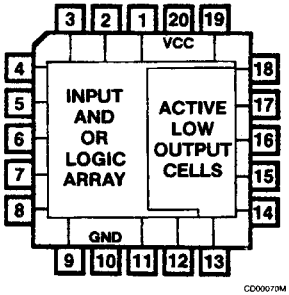

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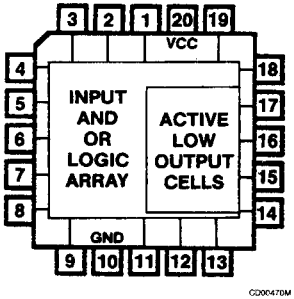

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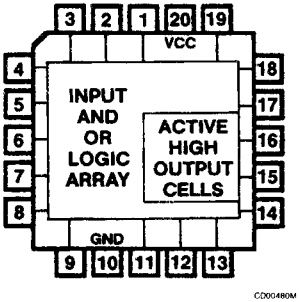

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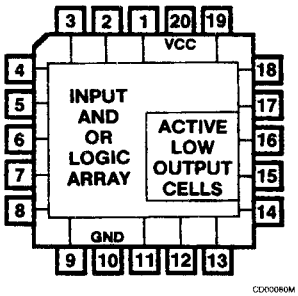

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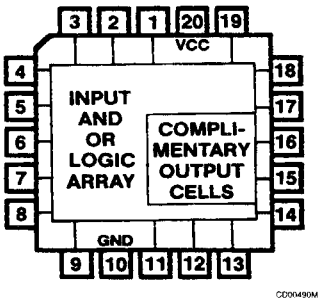


2

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OS}[2]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				55	90	mA

Switching Characteristics

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	Except 16C1	R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	35	ns
		16C1			25	45		25	40	

1. These are absolute values with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

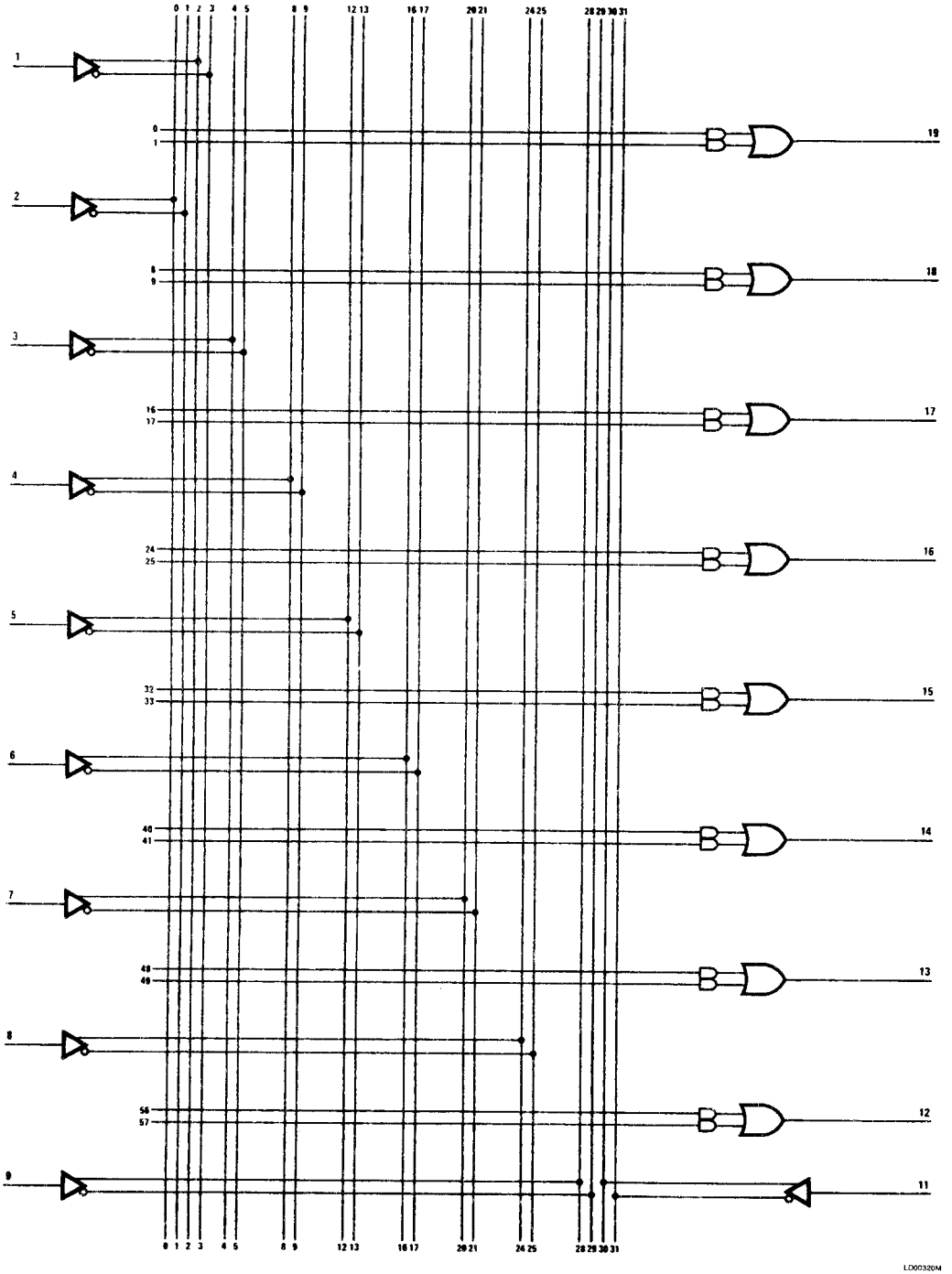
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 4mA		0.3	0.5	V
			Com	I_{OL} = 4mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −1mA	2.4	2.8		V
			Com	I_{OH} = −1mA				
I_{OS}[2]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				30	45	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	R_1 = 1.12kΩ R_2 = 2.2kΩ		45	80		45	60	ns

1. These are absolute values with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

10H8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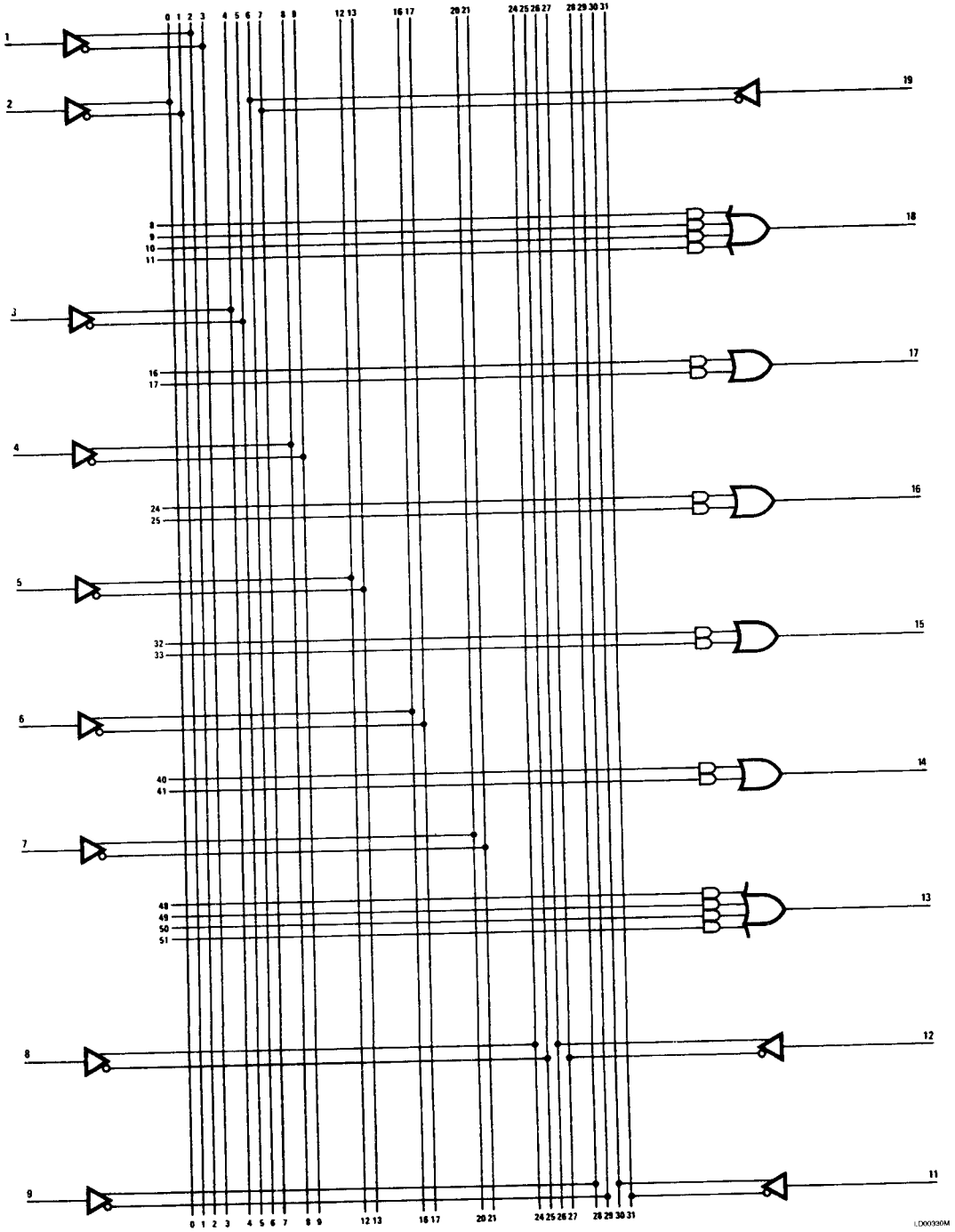
12H6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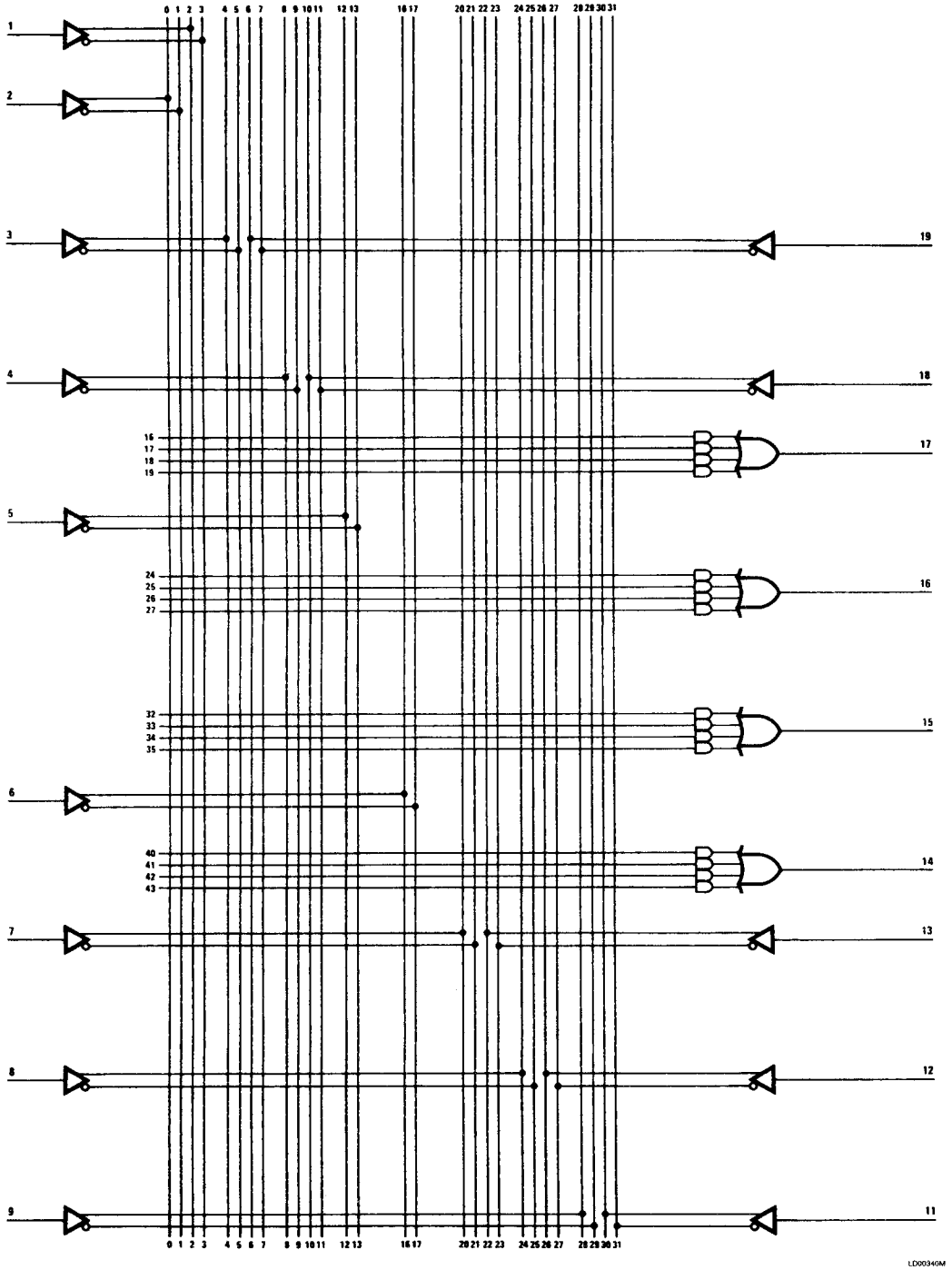
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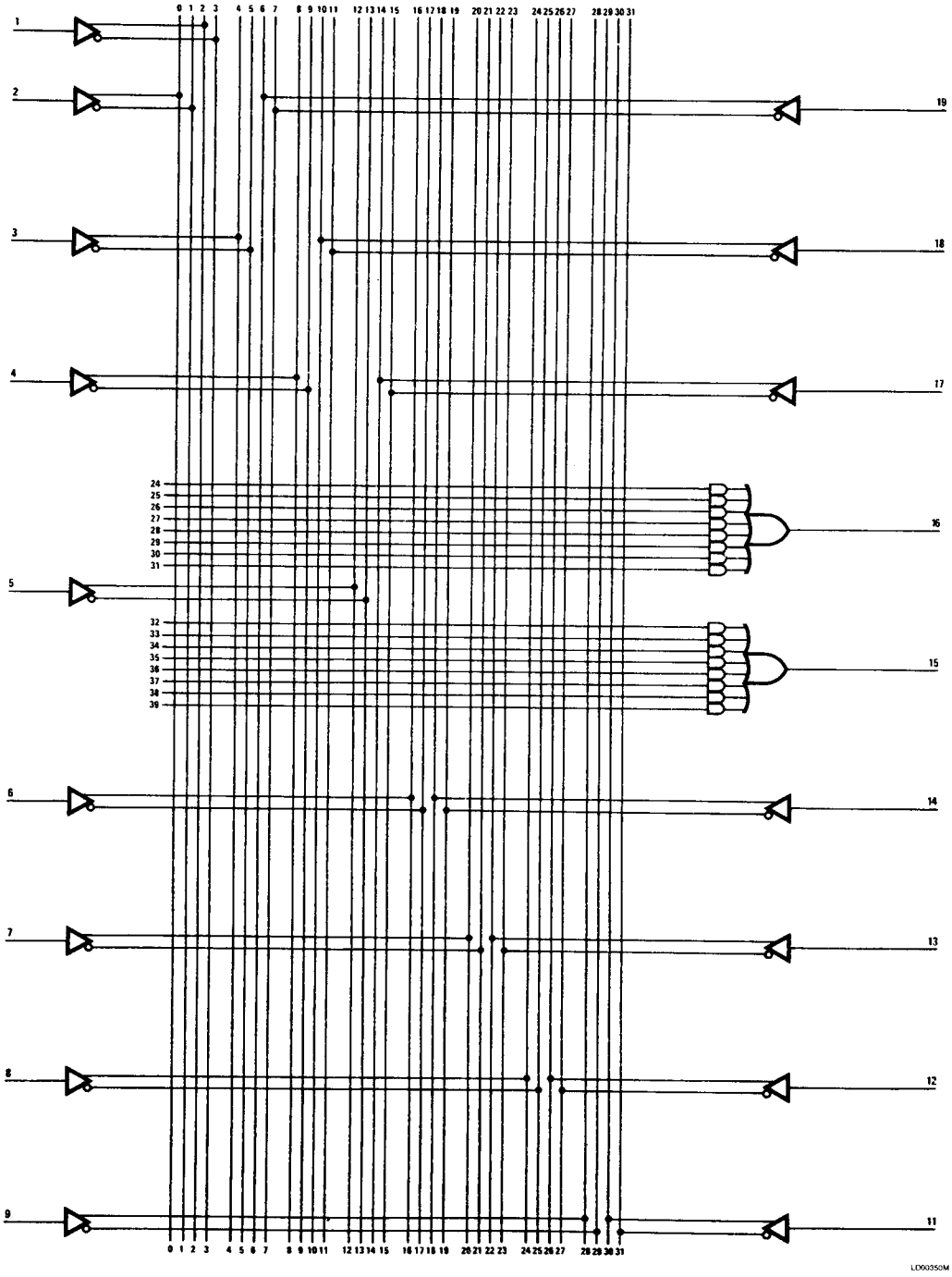
16H2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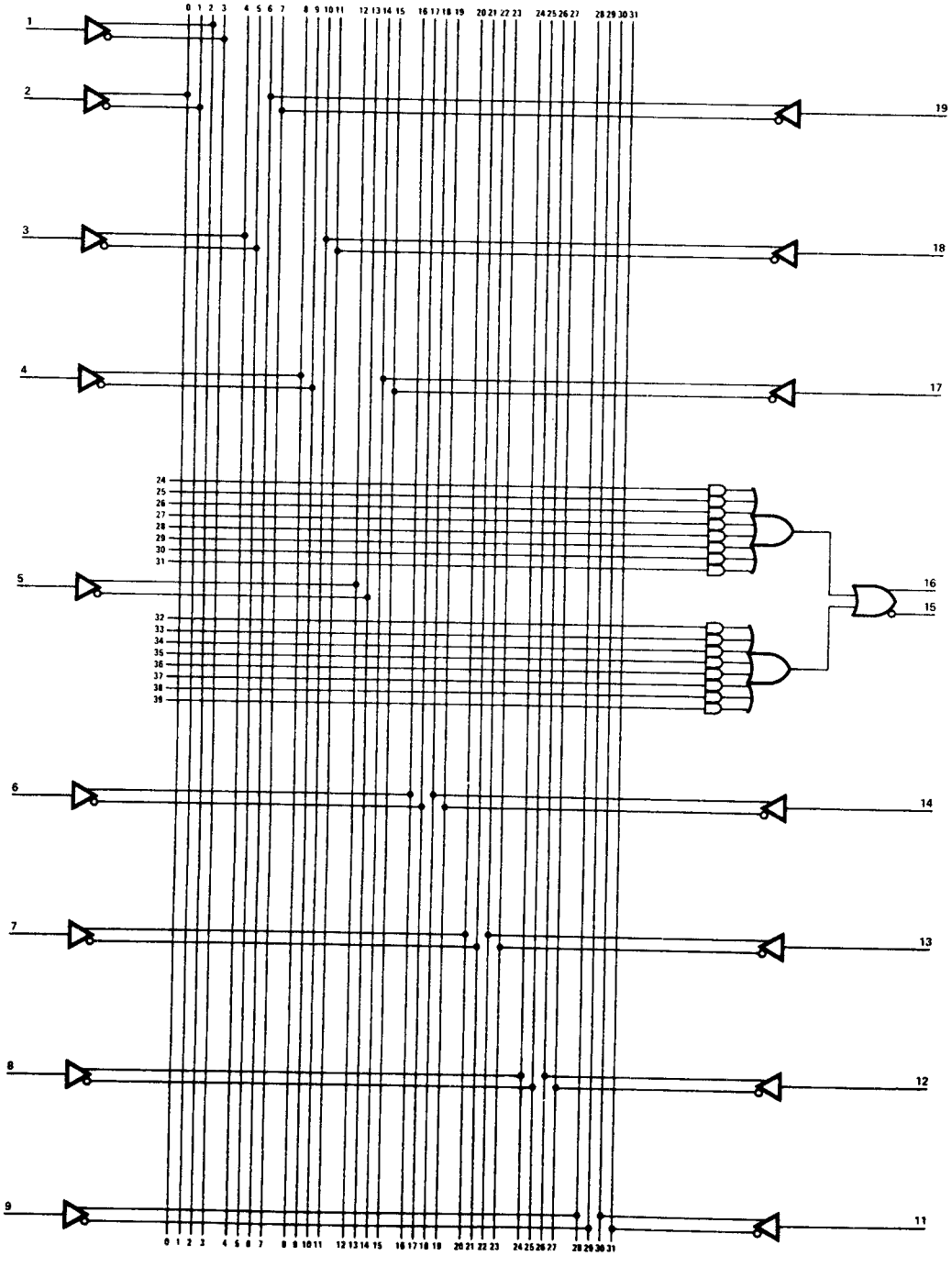
16C1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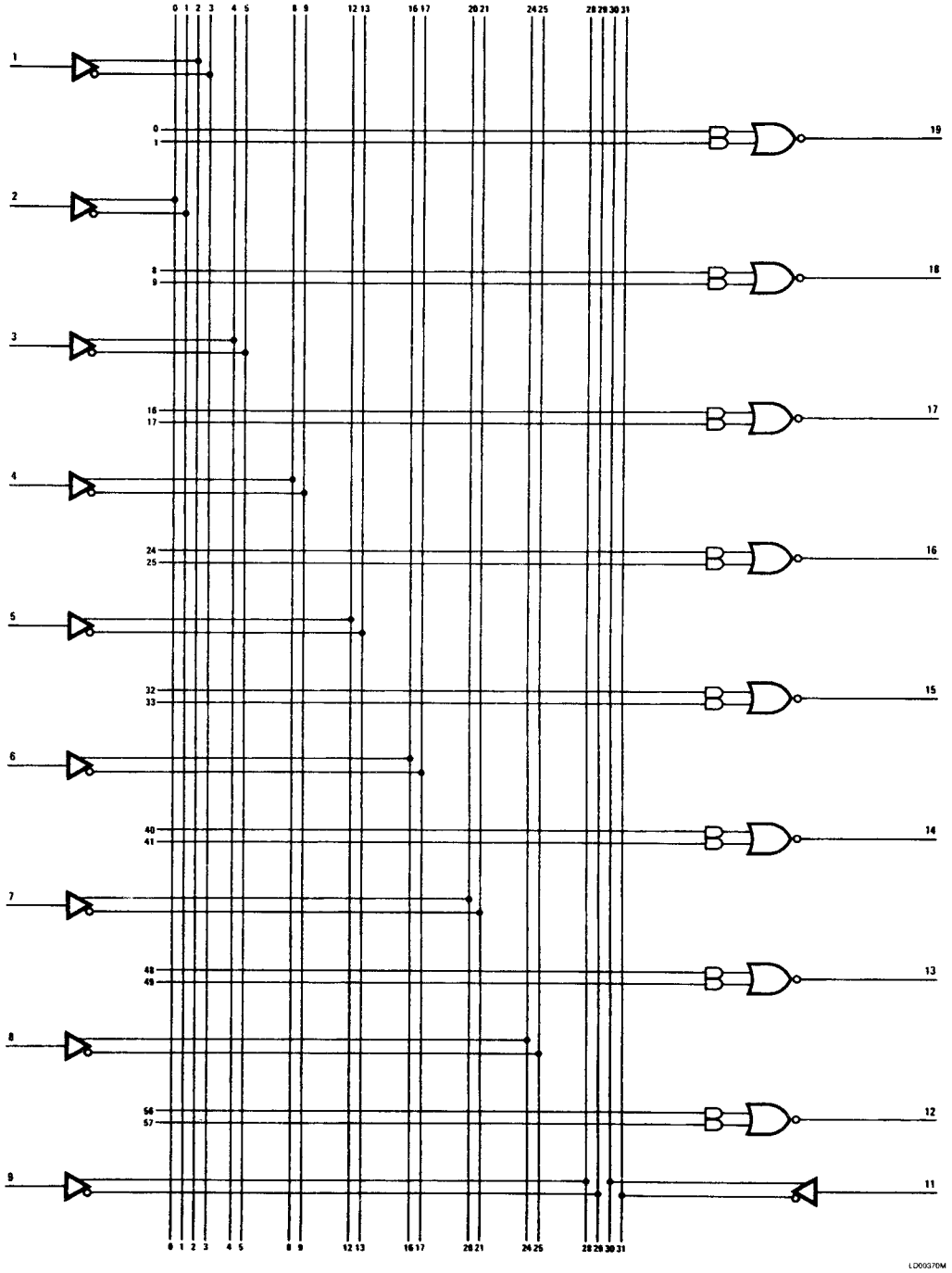
10L8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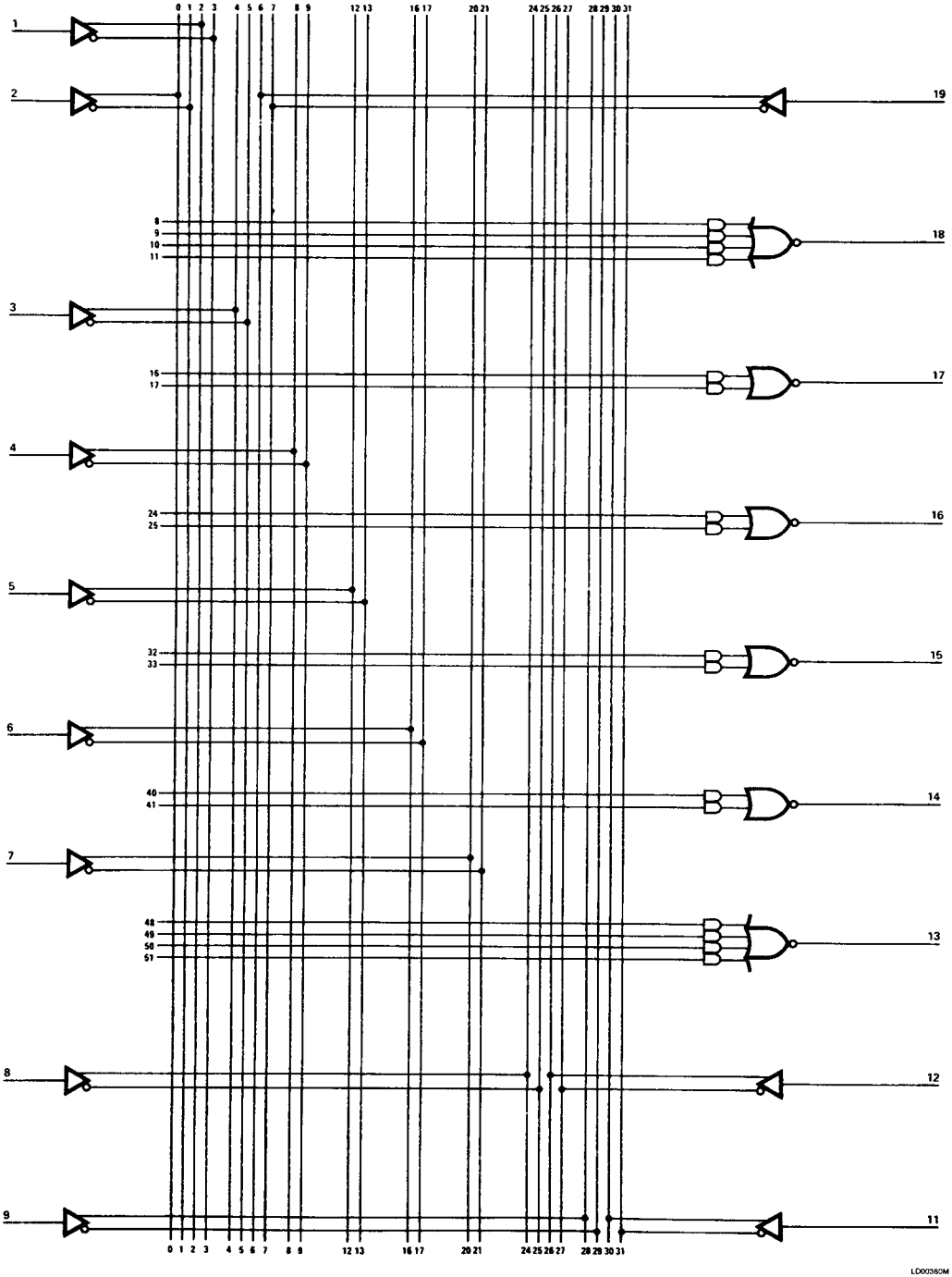
LD00370M

16L6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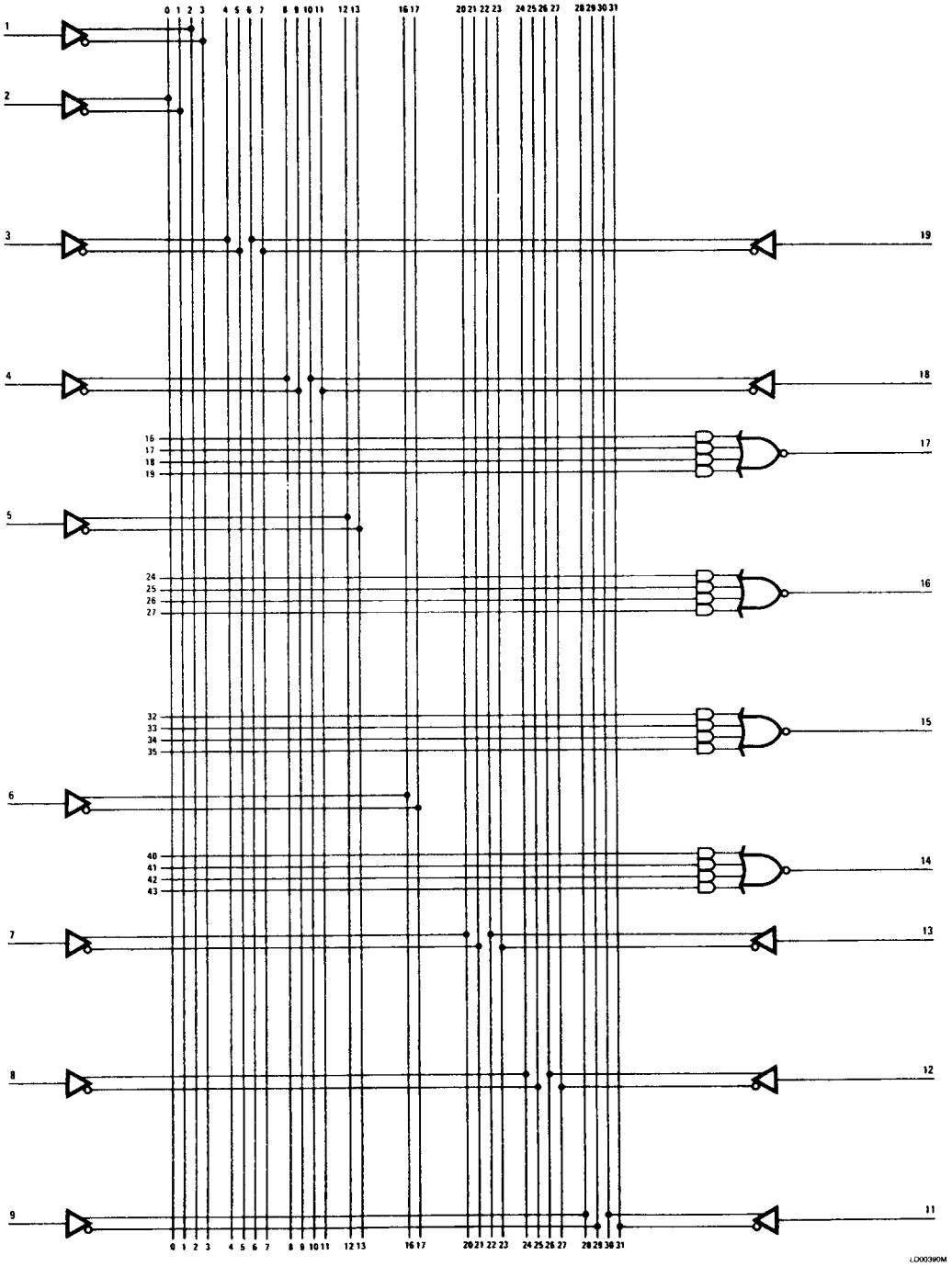
14L4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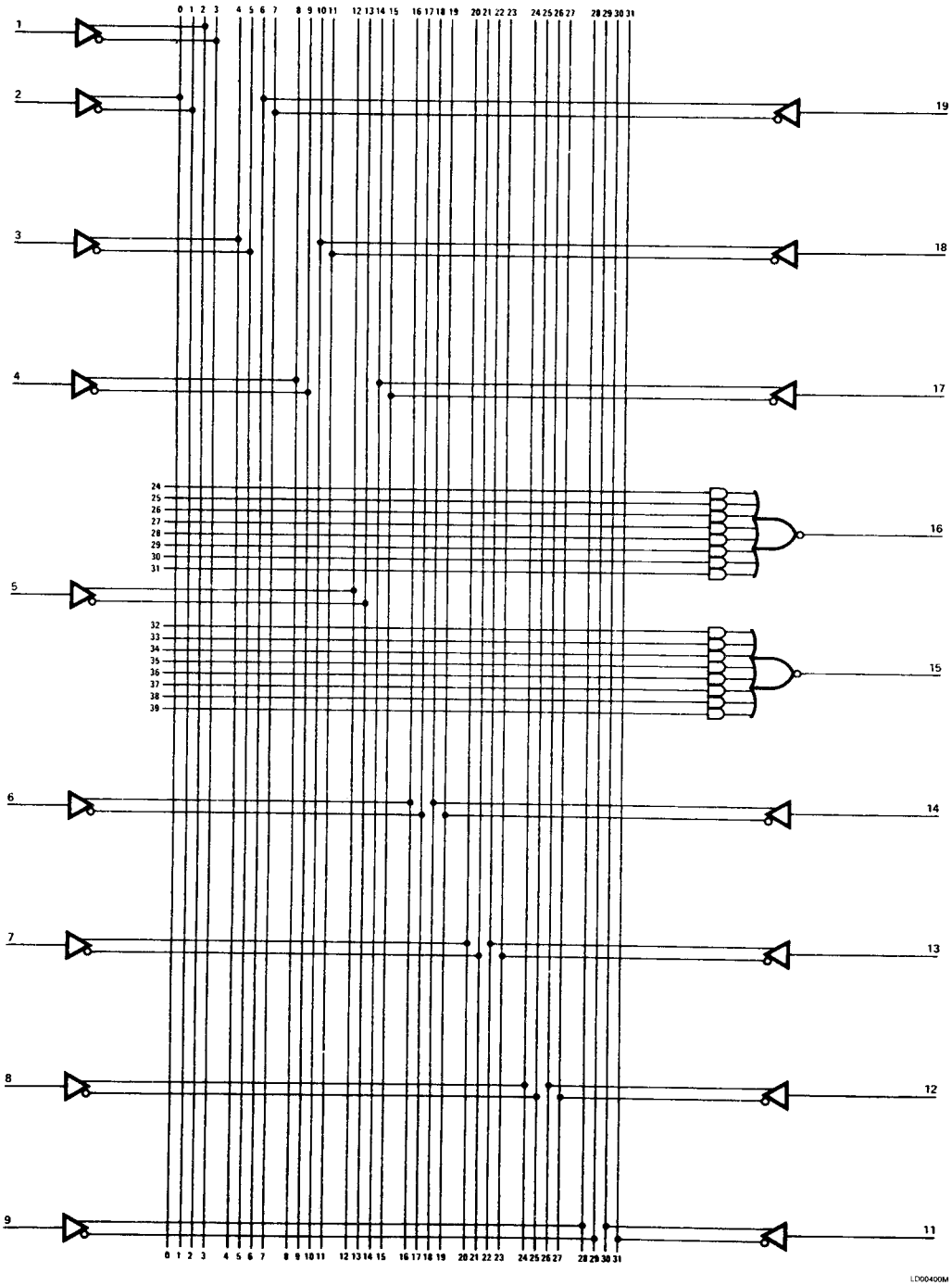
LD00390M

16L2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LD00400M

Medium 20 Series

	DEDICATED INPUTS	OUTPUTS	
		COMBINATORIAL	REGISTERED
PAL16L8	10	8 (6 I/O)	0
PAL16R8	8	0	8
PAL16R6	8	2 I/O	6
PAL16R4	8	4 I/O	4

Description

The Medium 20 Series offers the four most popular PAL device architectures. It also provides the fastest PAL devices in the industry.

The Medium 20 Series consists of four devices, each with sixteen array inputs and eight outputs. The devices have either 0, 4, 6, or 8 registered outputs, with the remaining being combinatorial. Each of the registered outputs feeds back into the array, for sequential designs. The combinatorial outputs also feed back into the array, except for two of the outputs on the 16L8. This feedback allows the output to also operate as an input if the output is disabled.

Enable

The combinatorial outputs are enabled by a product term. The registered outputs are enabled by a common enable pin.

Polarity

All outputs are active low.

Performance

Several speed/power versions are available:

Suffix	t_{PD} (ns)	I_{CC} (mA)
(standard)	35	180
A	25	180
A-2	35	90
A-4	55	50
B or BP*	15	180
B-2	25	90
B-4	35	55
D	10	180

* contact Monolithic Memories for datasheet

The D Series offers the fastest TTL programmable logic devices in the industry, at 10ns tpd.

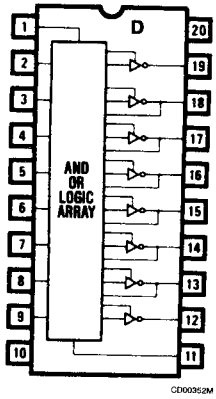
Preload and Power-up Reset

The BP Series offers register preload for device testability. The registers can be preloaded from the outputs by using supervoltages (see waveforms at end of section) in order to simplify functional testing. The PAL20BP Series also offers Power-up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

2

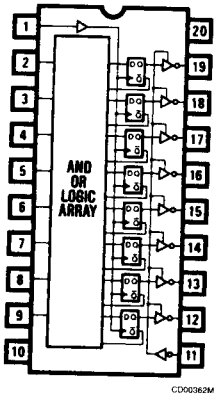
DIP Pinouts

16L8/A/A-2/A-4/
B/B-2/B-4/D



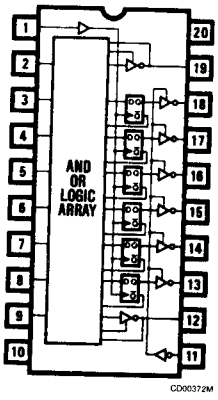
CD00352M

16R8/A/A-2/A-4/
B/B-2/B-4/D



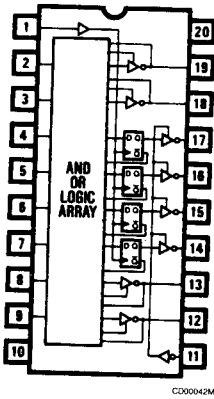
CD00362M

16R6/A/A-2/A-4/
B/B-2/B-4/D



CD00372M

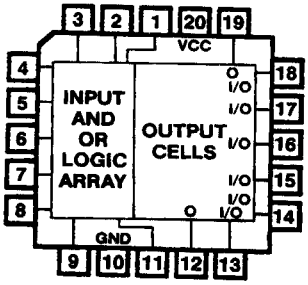
16R4/A/A-2/A-4/
B/B-2/B-4/D



CD00042M

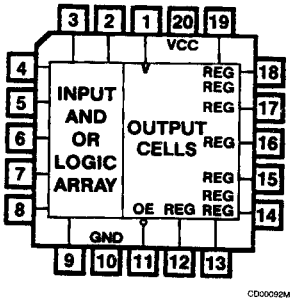
PLCC Pinouts

16L8/A/A-2/A-4/
B/B-2/B-4/D



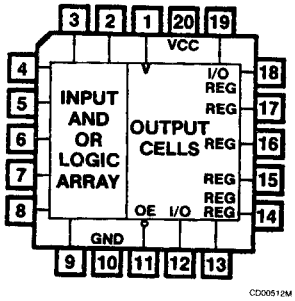
CD00502M

16R8/A/A-2/A-4/
B/B-2/B-4/D



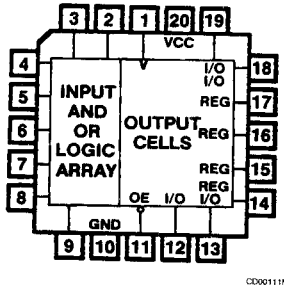
CD00092M

16R6/A/A-2/A-4/
B/B-2/B-4/D



CD00512M

16R4/A/A-2/A-4/
B/B-2/B-4/D



CD00111M

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1]			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	25	10		ns
		High	25	10		
t_{su}	Set up time from input or feedback to clock	16R8, 16R6, 16R4	35	25		ns
t_h	Hold time		0	−15		ns
T_A	Operating free-air temperature		0		75	°C
T_C	Operating case temperature					°C

Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage						0.8	V
V_{IH}[2]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Com	I_{OL} = 24mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	Com	I_{OH} = −3.2mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}[3]				V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	16R4, 16R6, 16R8, 16L8			120	180	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL			UNIT
				MIN	TYP	MAX	
t_{PD}	Input or feedback to output	16R6, 16R4, 16L8	R_1 = 200Ω, R_2 = 390Ω		25	35	ns
t_{CLK}	Clock to output or feedback				15	25	ns
t_{PZX}	Pin 11 to output enable except 16L8				15	25	ns
t_{PXZ}	Pin 11 to output disable except 16L8				15	25	ns
t_{PZX}	Input to output enable	16R6, 16R4, 16L8			25	35	ns
t_{PXZ}	Input to output disable	16R6, 16R4, 16L8			25	35	ns
f_{MAX}	Maximum frequency	16R8, 16R6, 16R4		16	25		MHz

1. The PAL20 Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	10		15	10		ns
		High	20	10		15	10		
t_{su}	Set up time from input or feedback to clock	16R8A, 16R6A, 16R4A	30	15		25	15		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −2mA	2.4	2.8		V
			Com	I_{OH} = −3.2mA				
I_{OZL}[2]	Off-state output current	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}[2]				V_O = 2.4V			100	μA
I_{OS}[3]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	16R6A, 16R4A, 16L8A	$R_1 = 200\Omega$ $R_2 = 390\Omega$		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 11 to output enable except 16L8A				10	25		10	20	ns
t_{PXZ}	Pin 11 to output disable except 16L8A				11	25		11	20	ns
t_{PZX}	Input to output enable	16R6A, 16R4A, 16L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	16R6A, 16R4A, 16L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	16R8A, 16R6A, 16R4A		20	40		28.5	40		MHz

2

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNI
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback to clock	16R6A-2, 16R4A-2, 16R8A-2	50	25		35	25		ns
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −2mA	2.4	2.8		V
			Com	I_{OH} = −3.2mA				
I_{OZL}[2]	Off-state output current	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}[2]				V_O = 2.4V			100	μA
I_{OS}[3]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	16L8A-2, 16R6A-2, 16R4A-2	R_1 = 200Ω, R_2 = 390Ω		25	50		25	35	ns
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable except 16L8A-2				15	25		15	25	ns
t_{PZX}	input to output enable	16L8A-2, 16R6A-2, 16R4A-2			25	45		25	35	ns
t_{PXZ}	Input to output disable	16L8A-2, 16R6A-2, 16R4A-2			25	45		25	35	ns
f_{MAX}	Maximum frequency	16R8A-2, 16R6A-2, 16R4A-2		14	25		16	25		MHz

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Operating Conditions

SYMBOL	PARAMETER			MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock		Low	40	20		30	20		ns
			High	40	20		30	20		
t_{su}	Set up time from input or feedback to clock	16R8A-4, 16R6A-4, 16R4A-4		90	45		60	45		ns
t_h	Hold time			0	−15		0	−15		ns
T_A	Operating free-air temperature			−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 4mA		0.3	0.5	V
			Com	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −1mA	2.4	2.8		V
			Com	I_{OH} = −1mA				
I_{OZL}[2]	Off-state output current	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}[2]				V_O = 2.4V			100	μA
I_{OS}[3]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				30	50	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	16R6A-4, 16R4A-4, 16L8A-4	R_1 = 800Ω, R_2 = 1.56kΩ		35	75		35	55	ns
t_{CLK}	Clock to output or feedback				20	45		20	35	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable – except 16L8A-4				15	40		15	30	ns
t_{PZX}	Input to output enable	16R6A-4, 16R4A-4, 16L8A-4			30	65		30	50	ns
t_{PXZ}	Input to output disable	16R6A-4, 16R4A-4, 16L8A-4			30	65		30	50	ns
f_{MAX}	Maximum frequency	16R8A-4, 16R6A-4, 16R4A-4		8	18		11	18		MHz

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1]			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	10	6		ns
		High	10	5		
t_{su}	Setup time from input or feedback to clock	16R8B 16R6B 16R4B	15	10		ns
t_h	Hold time		0	−10		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL			UNIT
				MIN	TYP	MAX	
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL			UNIT
				MIN	TYP	MAX	
t_{PD}	16L8B, 16R4B, 16R6B input or feedback to output		Commercial R_1 = 200Ω R_2 = 390Ω		12	15	ns
t_{CLK}	Clock to output or feedback except 16L8B				8	12	ns
t_{PZX}	Pin 11 to output enable except 16L8B				10	15	ns
t_{PXZ}	Pin 11 to output disable except 16L8B				10	15	ns
t_{PZX}	Input to output enable	16R6B, 16R4B, and 16L8B			12	22	ns
t_{PXZ}	Input to output disable	16R6B, 16R4B, and 16L8B			12	15	ns
f_{MAX}	16R8B, 16R6B, 16R4B Maximum frequency	Feedback		37	45		MHz
		No feedback		50	55		

1. The PAL20B Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1]			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	15	10		ns
		High	15	10		
t_{su}	Setup time from input or feedback to clock	16R8B-2 16R6B-2 16R4B-2	25	15		ns
t_h	Hold time		0	−10		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL			UNIT
				MIN	TYP	MAX	
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−100	−250	mA
I_{CC}	Supply current	V_{CC} = MAX			60	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL			UNIT
			MIN	TYP	MAX	
t_{PD}	Input or feedback to output 16L8B-2, 16R4B-2, and 16R6B-2	Commercial R_1 = 200Ω R_2 = 390Ω		17	25	ns
t_{CLK}	Clock to output or feedback except 16L8B-2			10	15	ns
t_{PZX}	Pin 11 to output enable except 16L8B-2			10	20	ns
t_{PXZ}	Pin 11 to output disable except 16L8B-2			11	20	ns
t_{PZX}	Input to output enable 16R6B-2, 16R4B-2, and 16L8B-2			10	25	ns
t_{PXZ}	Input to output disable 16R6B-2, 16R4B-2, and 16L8B-2			13	25	ns
f_{MAX}	Maximum frequency 16R8B-2, 16R6B-2, and 16R4B-2		28.5	40		MHz

1. The PAL20B-2 Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1] MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	25	10		ns
		High	25	10		
t_{su}	Setup time from input or feedback to clock	16R8B-4 16R6B-4 16R4B-4	35	25		ns
t_h	Hold time		0	−10		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −1mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−100	−250	mA
I_{CC}	Supply current	V_{CC} = MAX			30	55	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 16L8B-4, 16R4B-4, and 16R6B-4	R_1 = 800Ω R_2 = 1.56KΩ		25	35	ns
t_{CLK}	Clock to output or feedback except 16L8B-4			15	25	ns
t_{PZX}	Pin 11 to output enable except 16L8B-4			15	25	ns
t_{PXZ}	Pin 11 to output disable except 16L8B-4			15	25	ns
t_{PZX}	Input to output enable 16R6B-4, 16R4B-4, and 16L8B-4			25	35	ns
t_{PXZ}	Input to output disable 16R6B-4, 16R4B-4, and 16L8B-4			25	35	ns
f_{MAX}	Maximum frequency 16R8B-4, 16R6B-4, and 16R4B-4		16	25		MHz

1. The PAL20B-4 Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Operating Conditions

SYMBOL	PARAMETER			COMMERCIAL[1] MIN	COMMERCIAL[1] TYP	COMMERCIAL[1] MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
t_w	Width of clock	Low	16R8D, 16R6D, 16R4D	8	6		ns
		High		8	5		
t_{su}	Setup time from input or feedback to clock			10	8		ns
t_h	Hold time			0	−6		ns
T_A	Operating free-air temperature			0	25	75	°C

Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			200	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	3.4		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA
C_{IN}	Input Capacitance	V_{IN} = 2.0V@f = 1MHz			2		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V@f = 1MHz			4		
$C_{CLK, EN}$	Clock/Enable Capacitance	$V_{CLK, EN}$ = 2.0V@f = 1MHz			9		

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL			UNIT
				MIN	TYP	MAX	
t_{PD}	Input or feedback to output 16L8D, 16R6D, 16R4D		$R_1 = 200\Omega$ $R_2 = 390\Omega$	3	8	10	ns
t_{CLK}	Clock to output or feedback except 16L8D			2	6	8	ns
t_{PZX}	Pin 11 to output enable except 16L8D			3	8	10	ns
t_{PXZ}	Pin 11 to output disable except 16L8D			3	8	10	ns
t_{PZX}	Input to output enable 16L8D, 16R6D, 16R4D			1	8	10	ns
t_{PXZ}	Input to output disable 16L8D, 16R6D, 16R4D			1	8	10	ns
f_{MAX}	Maximum frequency 16R8D, 16R6D, 16R4D	Feedback		55.5	70		MHz
		No feedback		62.5	75		

1. The PAL20D Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Metastability

Metastability is a condition which can occur in any latch or flip-flop if the minimum setup or hold times are violated. In most cases, the flip-flop will either react to the input or remain in its current state, both of which are stable results. The flip-flop can also reach an "in-between" condition called the metastable state, which is stable only if there is no noise in the system and the flip-flop is perfectly balanced. This metastable condition lasts until the flip-flop falls into one of its two stable states, which can take longer than the normal response time.

The PAL20D Series exhibits better metastability characteristics than most other registered devices. It is less likely to enter the metastable state and recovers faster to a stable state. As a result, the PAL20D Series can make an excellent synchronizer circuit, and the metastability characteristics have been specified for designs in which the setup and hold times may not always be met.

Metastability Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL			UNIT
			MIN	TYP	MAX	
p	Poisson process rate		0.85	1.05		ns^{-1}
k	MTBF constant			0.8	1.0	μs^{-1}
t_{MET}	Minimum recovery time in asynchronous mode	MTBF = 10 years f_d = (1/3)f d = 3		20	30	ns
f_{MET}	Maximum frequency in asynchronous mode	MTBF = 10 years f_d = (1/3)f d = 3	21	26		MHz

Definition of Variables

MTBF (Mean Time Between Failures): the average time between metastable occurrences that cause a violation of the device specifications. Metastability characteristics are calculated at an arbitrary MTBF of 10 years for the convenience of the user.

p (Poisson process rate): experimentally calculated factor which determines the slope of the curve of probability of failure.

k (MTBF constant): experimentally calculated factor which determines the magnitude of the curve of probability of failure.

tsu (setup time): the specified minimum time interval allowed between the application of a data signal at a specified device input pin (pin 9 on the device under test) and a subsequent clock transition. For the PAL20D Series, tsu is 10 nanoseconds.

tCLK (clock to output time): the specified maximum time interval between a clock transition and the availability of valid signals at an output pin. For the PAL20D Series, tCLK is 8 nanoseconds.

fMAX (maximum frequency): specified maximum frequency for the device under test. Calculated as 1/(tsu + tCLK). For the PAL20D Series, this calculates to 55.5 Megahertz.

f(clock frequency): actual clock frequency for the device under test.

f_d (data frequency): actual data frequency for a specified input to the device under test.

d (data ratio): the ratio of the clock frequency to the data frequency (f/f_d).

t(time delay): the additional time allowed per period beyond that required by the specifications. t is the actual time between clock transitions beyond the required period of (tsu + tCLK).

tMET (metastability recovery time): minimum t required to guarantee recovery from metastability, with specified test conditions.

fMET (metastability frequency): maximum f clock frequency to limit metastability failures, with specified test conditions.

Metastability Equations

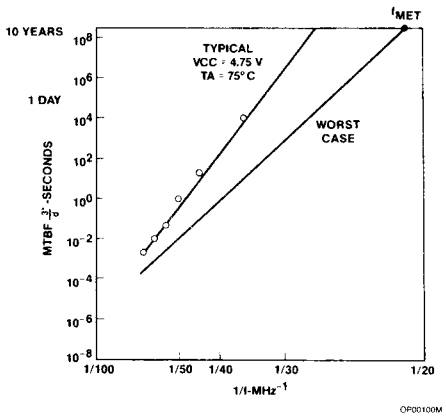
$MTBF = k\ (d/3)\ (1/f)^2\ e^{(p/f)}$

$fMAX = 1/(tsu + tCLK)$

$f = 1/(tsu + tCLK + t)$

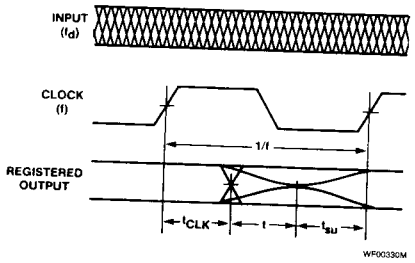
$f = d\ (f_d)$

Metastability vs. Clock Frequency

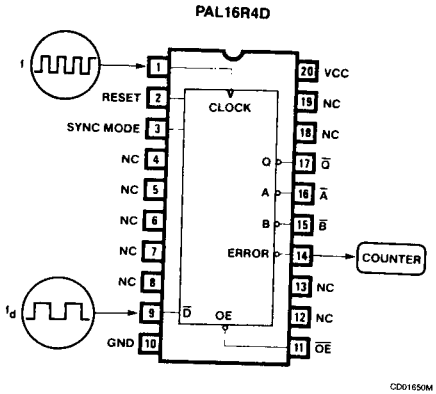


*Normalized to d = 3; multiply by 3/d for other data frequencies.

Metastability Waveforms



Metastability Test Circuit

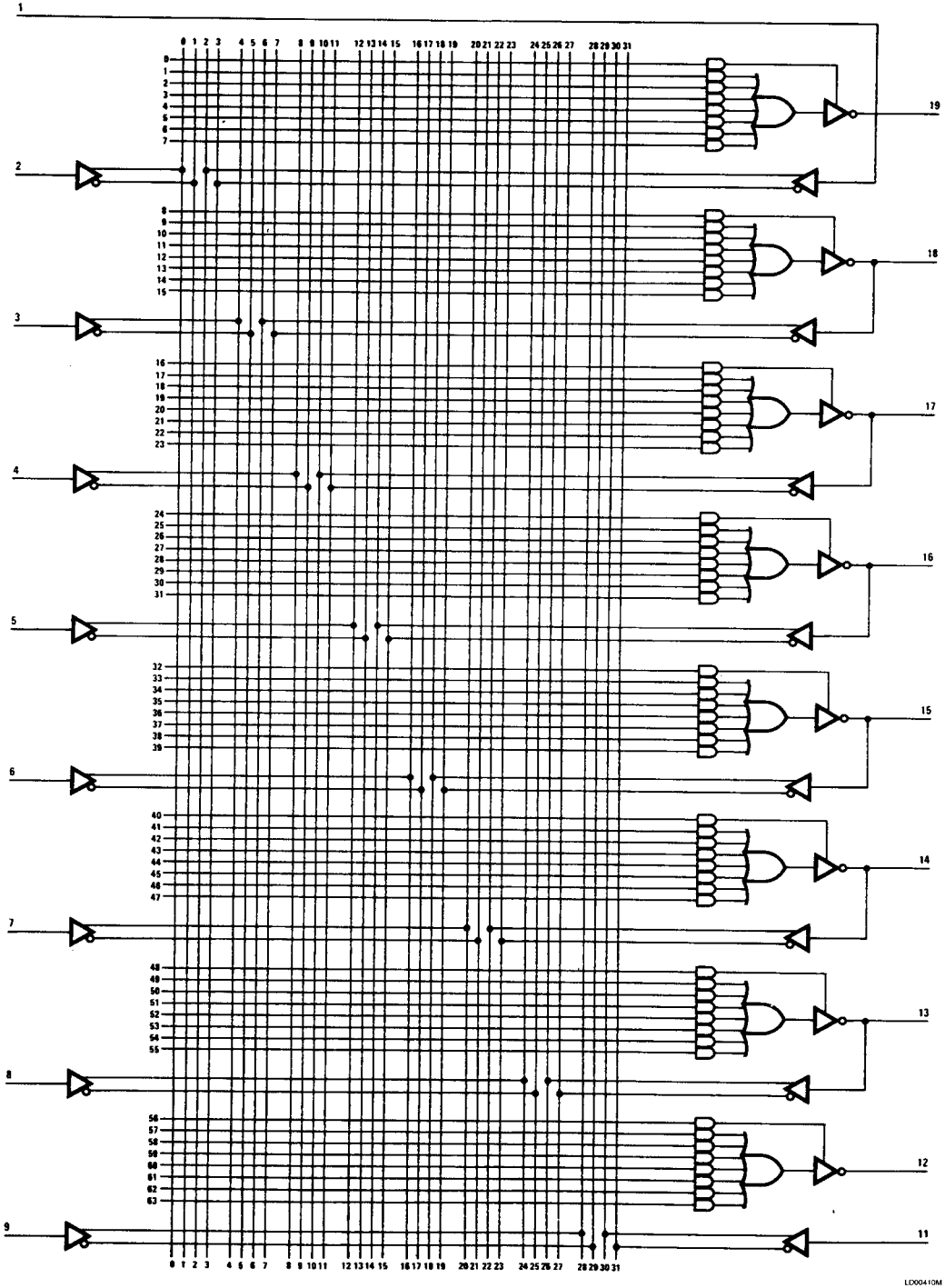


Metastability Test Pattern File

```
CHIP Metastability_Test PAL16R4

CLOCK RESET SYNC_MODE NC NC NC NC NC /D GND
/OE NC NC /ERROR /B /A /Q NC NC VCC

EQUATIONS

Q      := /Q* SYNC_MODE     ;TOGGLE SYNCHRONOUS INPUT (TESTS f MAX)
        +  D*/SYNC_MODE     ;TOGGLE ASYNCHRONOUS INPUT (TESTS META.)

A      :=  A*/Q             ;HOLD A (IF NOT ERROR)
        + /A* Q             ;TOGGLE A (IF NOT ERROR)
        +  ERROR            ;SET A IF ERROR

B      :=  B*/Q*/ERROR      ;HOLD B IF NOT ERROR, OR RESET
        + /B* Q*/ERROR      ;TOGGLE B IF NOT ERROR, OR RESET

ERROR := /A*/B              ;COMPARE A AND B,
        +  A* B             ; ERROR GOES HIGH IF A EQUALS B
        +  RESET            ;INITIALIZE A AND B TO OPPOSITE PHASES
```

TB02030M

16L8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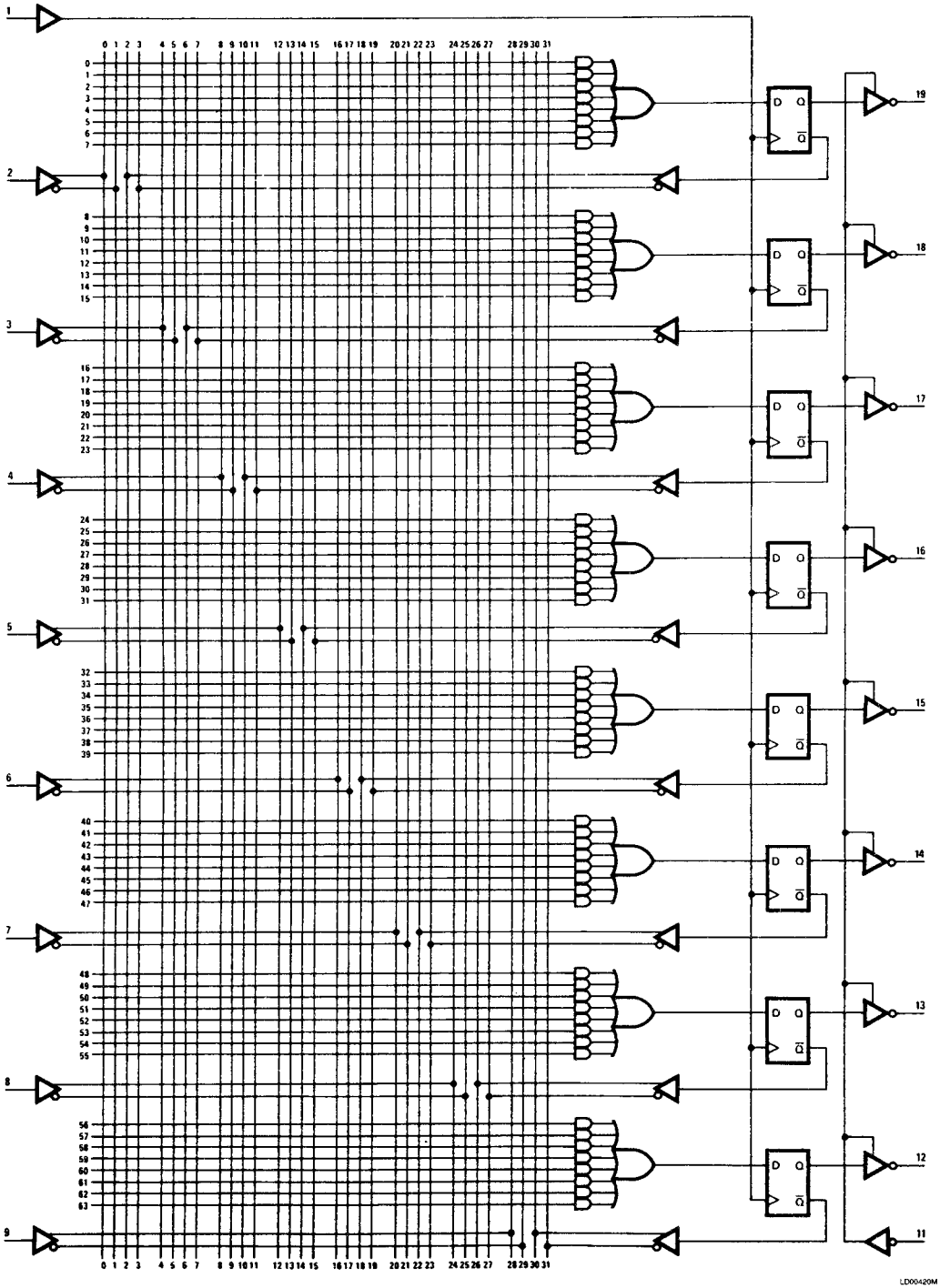
LD00410M

16R8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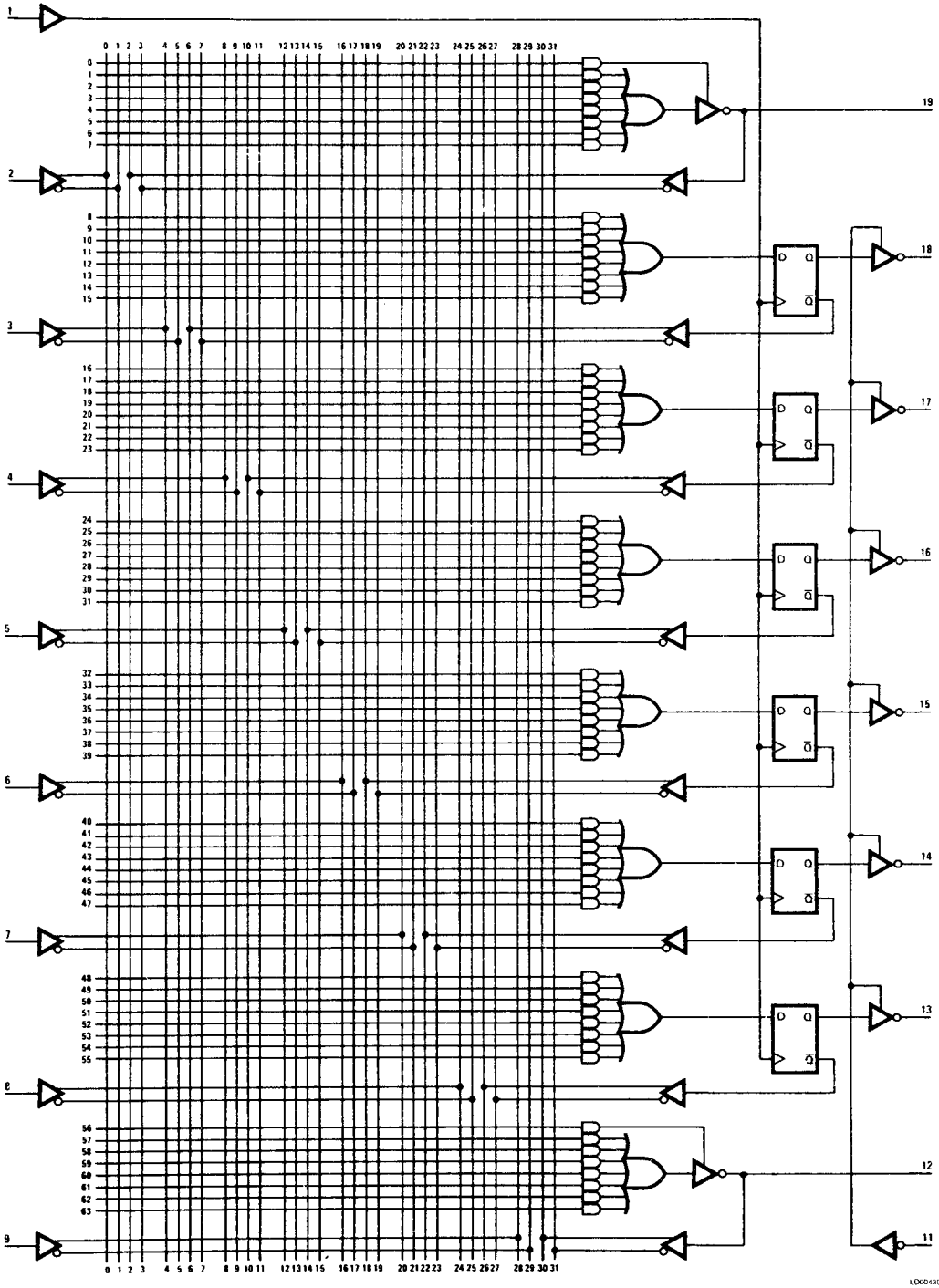
LD00420M

16R6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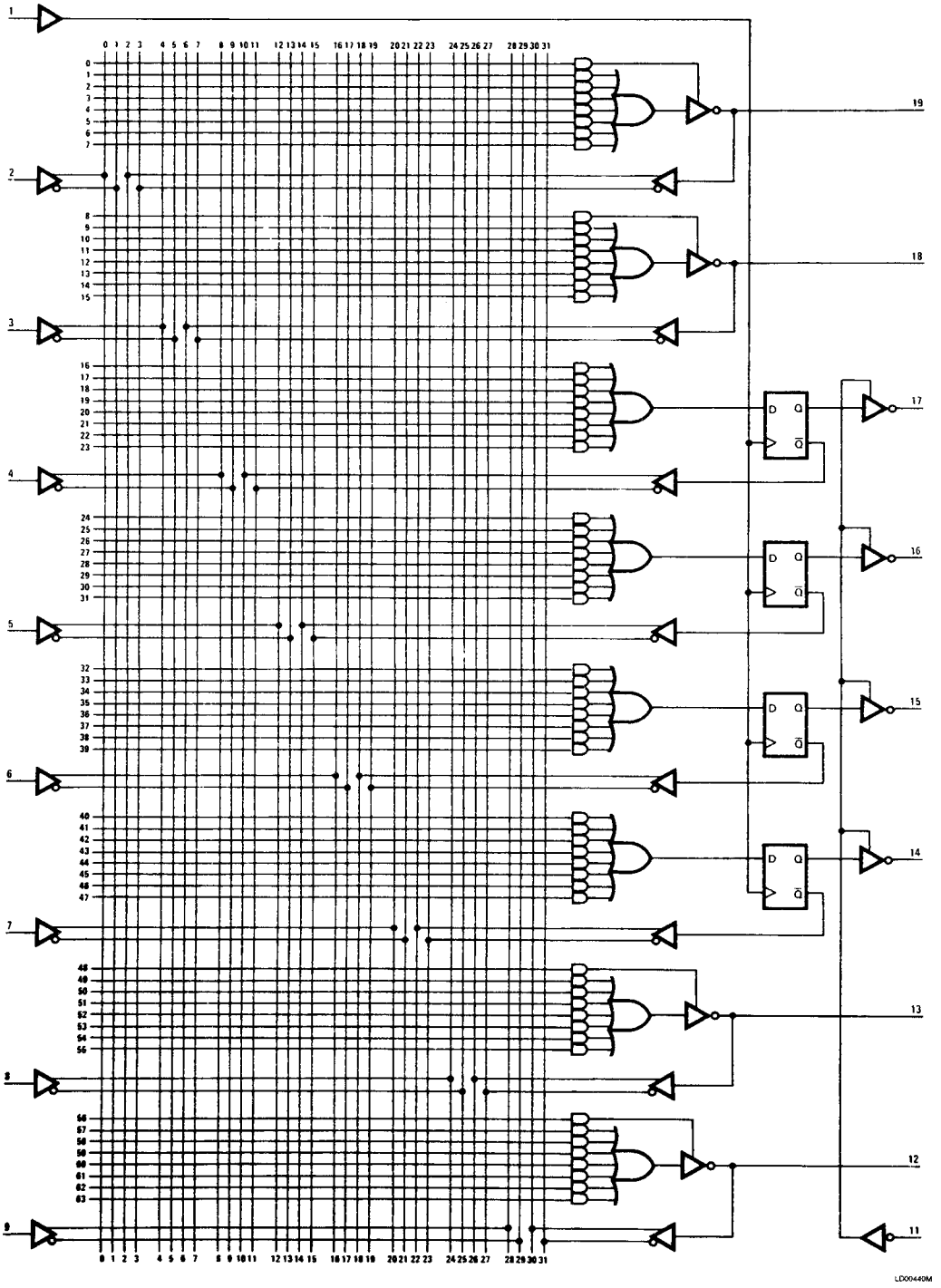
LD0043DM

16R4



Medium 20PA Series

	ARRAY INPUTS	OUTPUTS		t_{PD}* (ns)	I_{CC} (mA)
		COMBINATORIAL	REGISTERED		
PAL16P8A	16	8	0	25/30	180
PAL16RP8A	16	0	8	25/30	180
PAL16RP6A	16	6	2	25/30	180
PAL16RP4A	16	4	4	25/30	180

* 25ns active low, 30ns active high

Description

The Medium 20PA Series is equivalent to the Medium 20 Series, with the addition of programmable polarity. With programmable polarity unused, these devices are equivalent to the Medium 20A Series.

Polarity

Each of these devices offers programmable polarity on each output. If the polarity fuse is unused, the output is active low. If the polarity fuse is programmed, the output is inverted to active high.

Preload and Power-up Reset

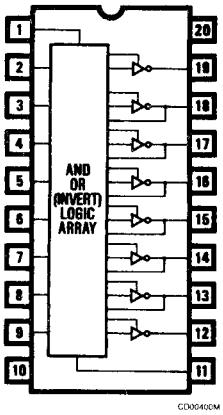
Each device also offers register preload for device testability. The registers can be preloaded from the outputs by using supervoltages (see waveforms at end of section) in order to simplify functional testing. This series also offers Power-up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

Performance

Performance varies according to the use of the programmable polarity. Active low outputs have a tpd of 25ns, while active high outputs have a tpd of 30ns due to the extra inversion. All devices consume 180mA maximum ICC.

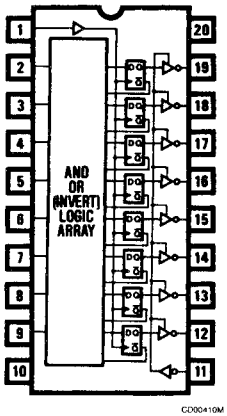
DIP Pinouts

16P8A



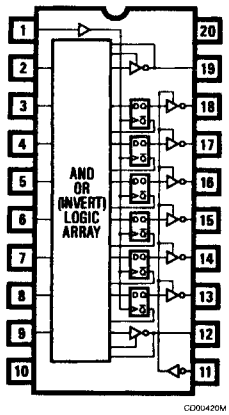
CD00400M

16RP8A



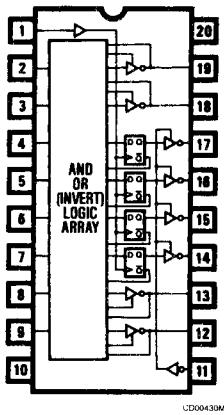
CD00410M

16RP6A



CD00420M

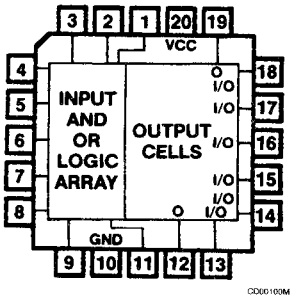
16RP4A



CD00430M

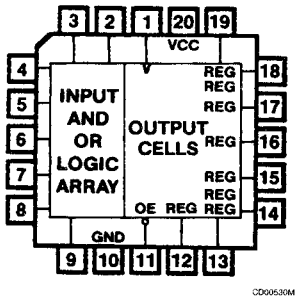
PLCC Pinouts

16P8A



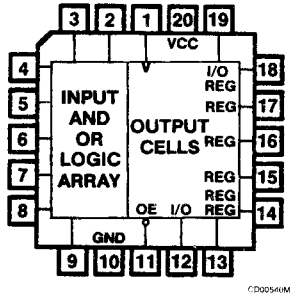
CD00100M

16RP8A



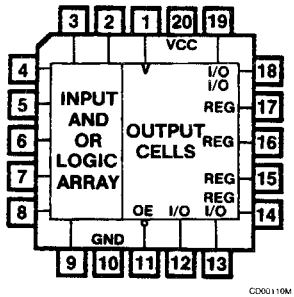
CD00530M

16RP6A



CD00540M

16RP4A



CD00110M

Operating Conditions

SYMBOL	PARAMETER			COMMERCIAL[1] MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
t_w	Width of clock	Low		20	14		ns
		High		10	6		
t_{su}	Setup time from input or feedback to clock	16RP8A 16RP6A 16RP4A	Polarity fuse intact	25	15		ns
			Polarity fuse blown	30	20		
t_h	Hold time			0	−10		ns
T_A	Operating free-air temperature			0		75	°C

Electrical Characteristics Over Operating Conditions

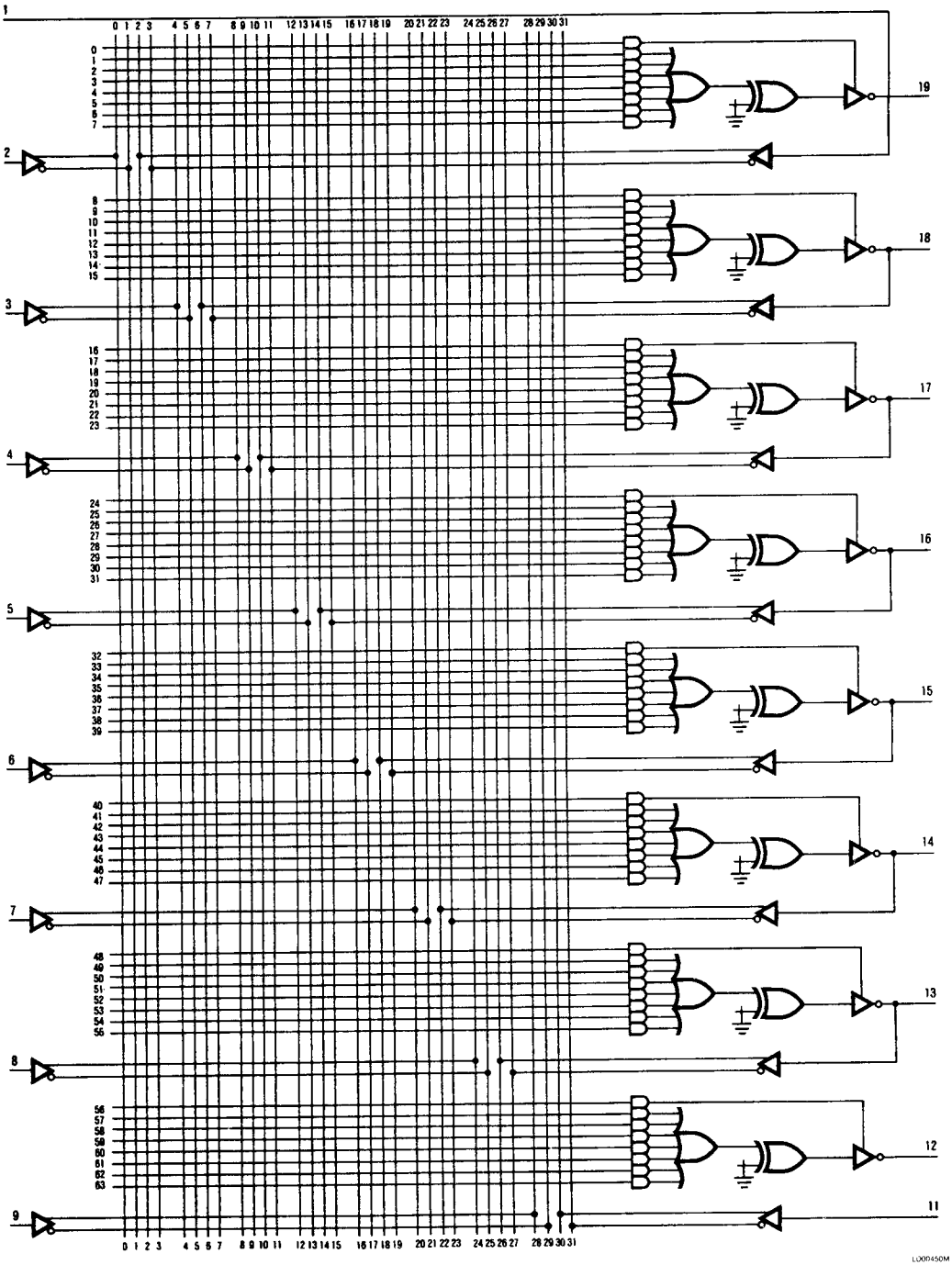
SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

1. The PAL20PA Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL			UNIT
				MIN	TYP	MAX	
t_{PD}	Input or feedback to output 16P8A, 16RP6A, 16RP4A	Polarity fuse intact	$R_1 = 200\Omega$ $R_2 = 390K\Omega$		15	25	ns
		Polarity fuse blown			20	30	
t_{CLK}	Clock to output or feedback				10	15	ns
t_{PZX}	Pin 11 to output enable except 16P8A				10	20	ns
t_{PXZ}	Pin 11 to output disable except 16P8A				11	20	ns
t_{PZX}	Input to output enable	16RP6A, 16RP4A, and 16P8A			10	25	ns
t_{PXZ}	Input to output disable	16RP6A, 16RP4A, and 16P8A			13	25	ns
f_{MAX}	Maximum frequency 16RP8A, 16RP6A, 16RP4A	Polarity fuse intact		28.5	40		MHz
		Polarity fuse blown		25	33		

16P8A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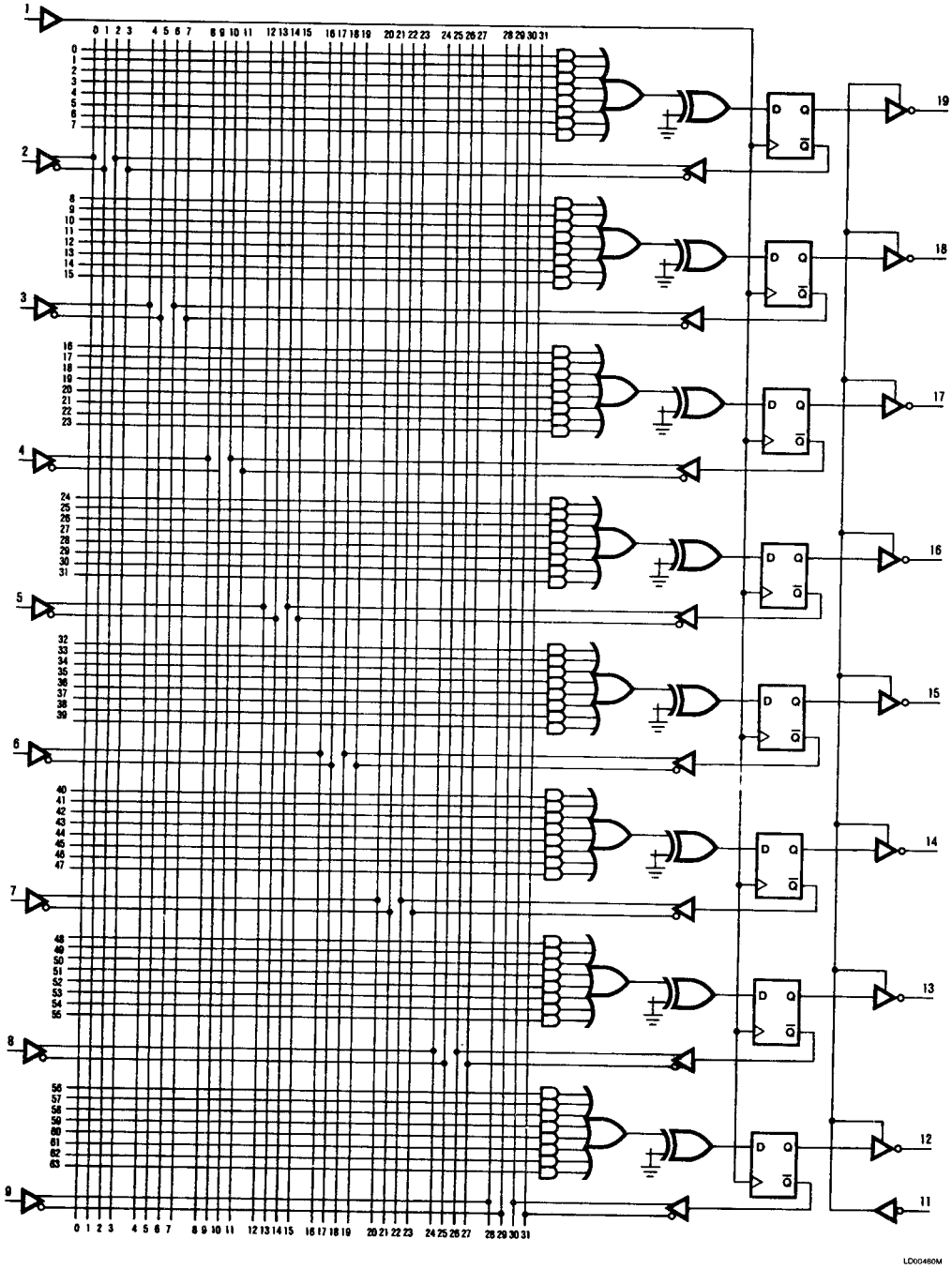
L000450M

16RP8A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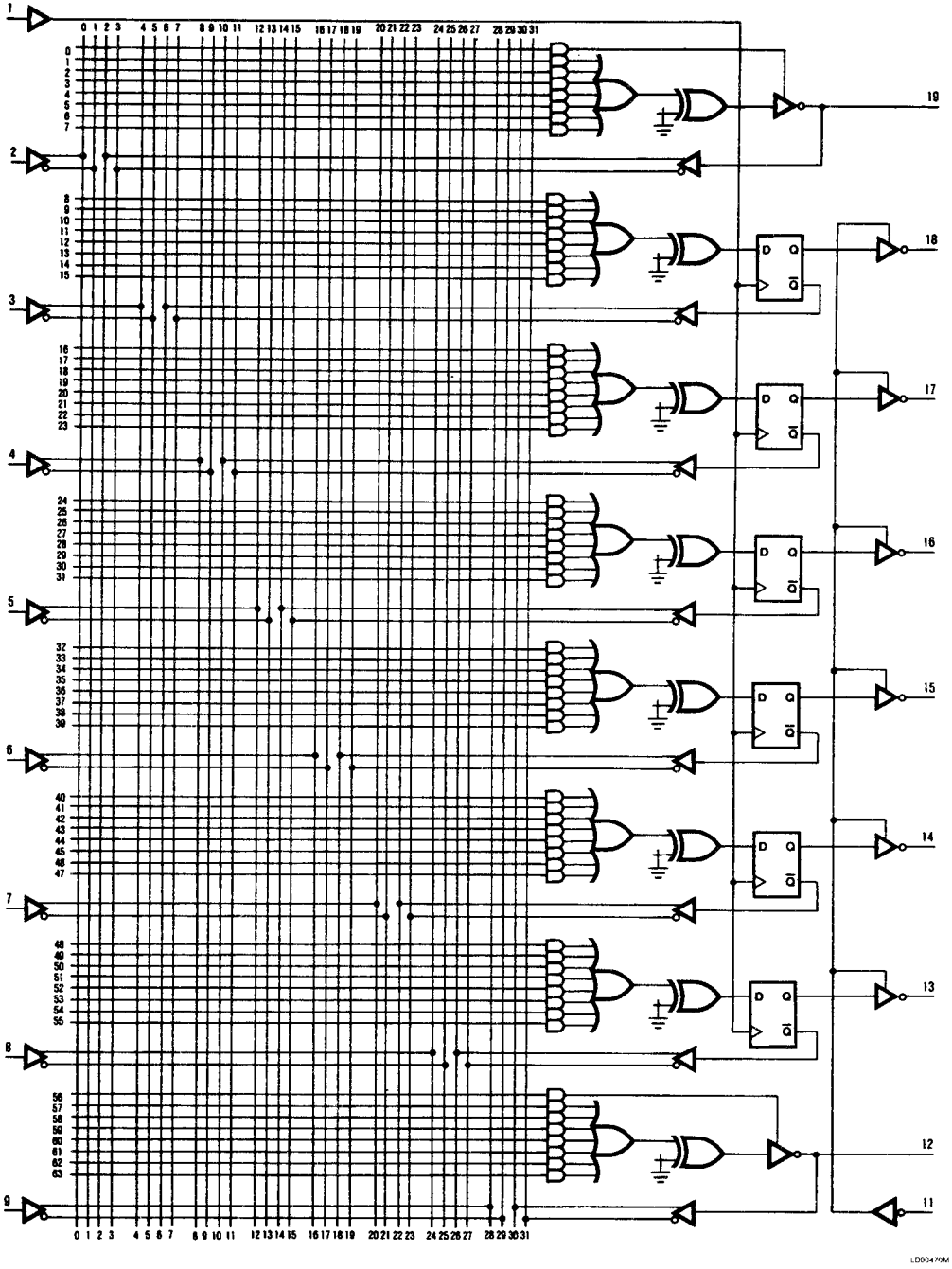
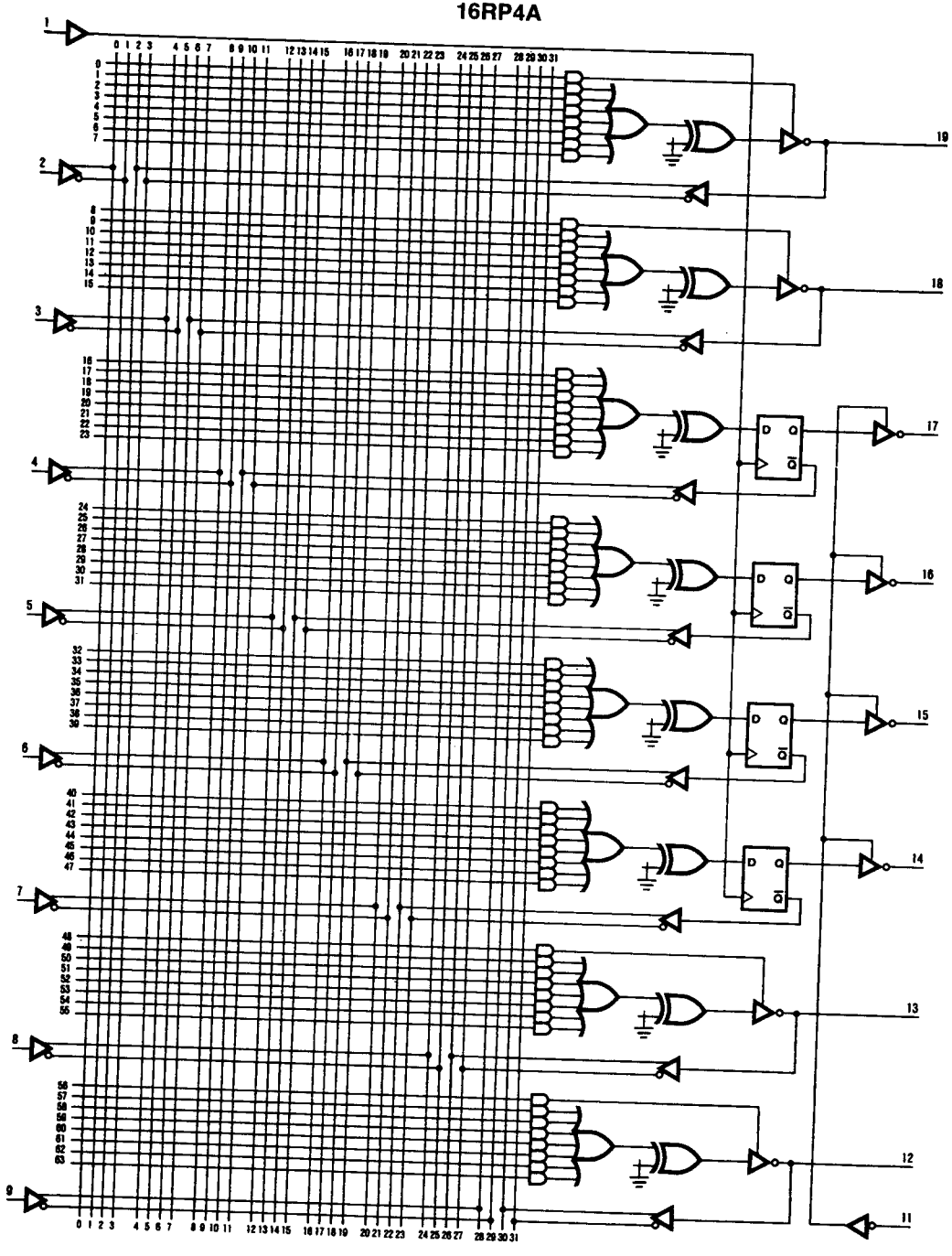
LD00460M

16RP6A



LD00470M

16RP4A



L000480M

Large 20 Arithmetic Series

	ARRAY INPUTS	OUTPUTS		PRODUCT TERMS
		COMBINATORIAL	REGISTERED	
PAL16X4	16	4	4	64
PAL16A4	16	4	4	74

Description

The PAL16X4 and PAL16A4 have arithmetic gated feedback. These are specialized devices for arithmetic applications.

Arithmetic Gated Feedback

The arithmetic functions (add, subtract, greater than, and less than) are implemented by addition of gated feedback to the features of the XOR PAL device. The XOR at the input of the D-type flip-flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL device array. The flip-flop Q output is fed back to be gated with input terms A (Figure 13). This gated feedback provides any one of the sixteen possible Boolean combinations which are mapped in the Karnaugh map (Figure 14). Figure 15 shows how the PAL device array can be programmed to perform these sixteen operations. These features provide for versatile operations on two variables and facilitate the parallel generation of carrys necessary for fast arithmetic operations.

2

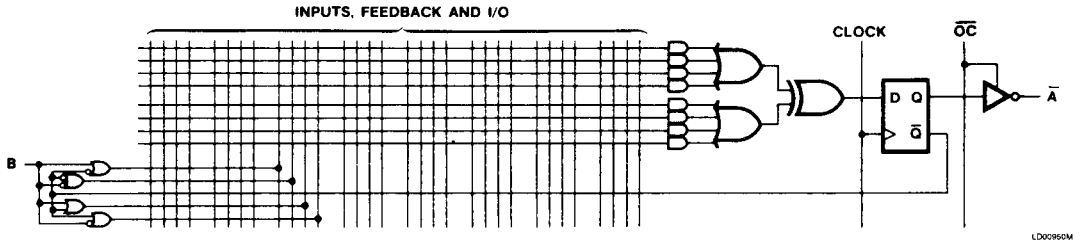


Figure 13

$\overline{(\bar{A}+B)\cdot(\bar{A}+\bar{B})}$ / $\overline{(A+\bar{B})\cdot(A+B)}$	--	-x	xx	x-
--	1	$\bar{A}+\bar{B}$	$\bar{A}$	$\bar{A}+B$
-x	A+B	A:+:B	$\bar{A}\cdot B$	B
xx	A	$A\cdot\bar{B}$	0	$A\cdot B$
x-	$A+\bar{B}$	$\bar{B}$	$\bar{A}*\bar{B}$	A:•:B

TB01630M

Figure 14

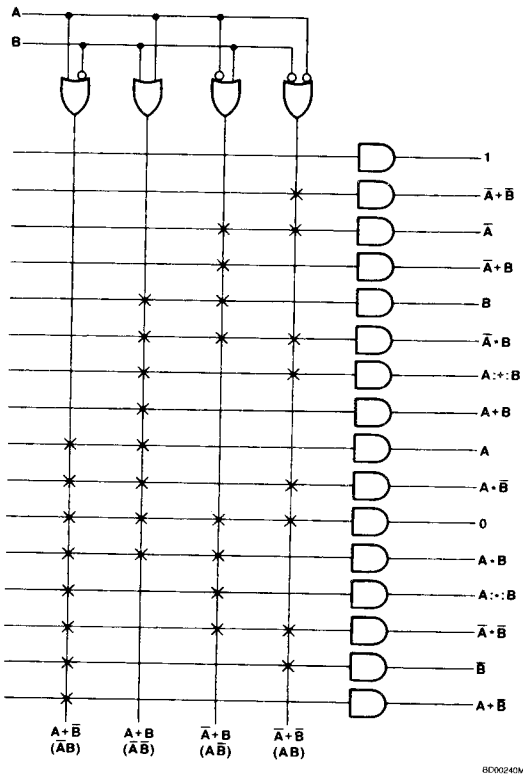
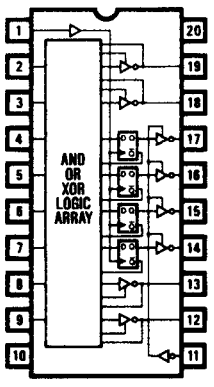


Figure 15

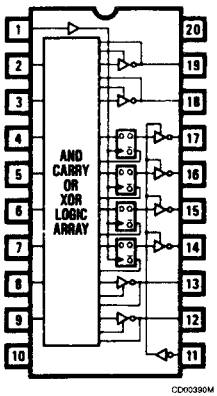
DIP Pinouts

16X4



CD00380M

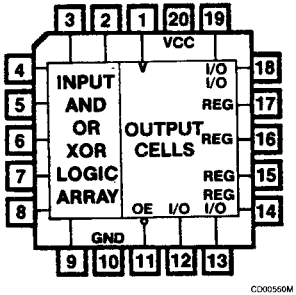
16A4



CD00390M

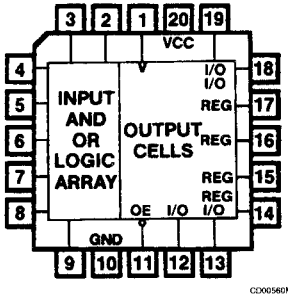
PLCC Pinouts

16X4



CD00560M

16A4



CD00560M

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback to clock		55	30		45	30		ns
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics

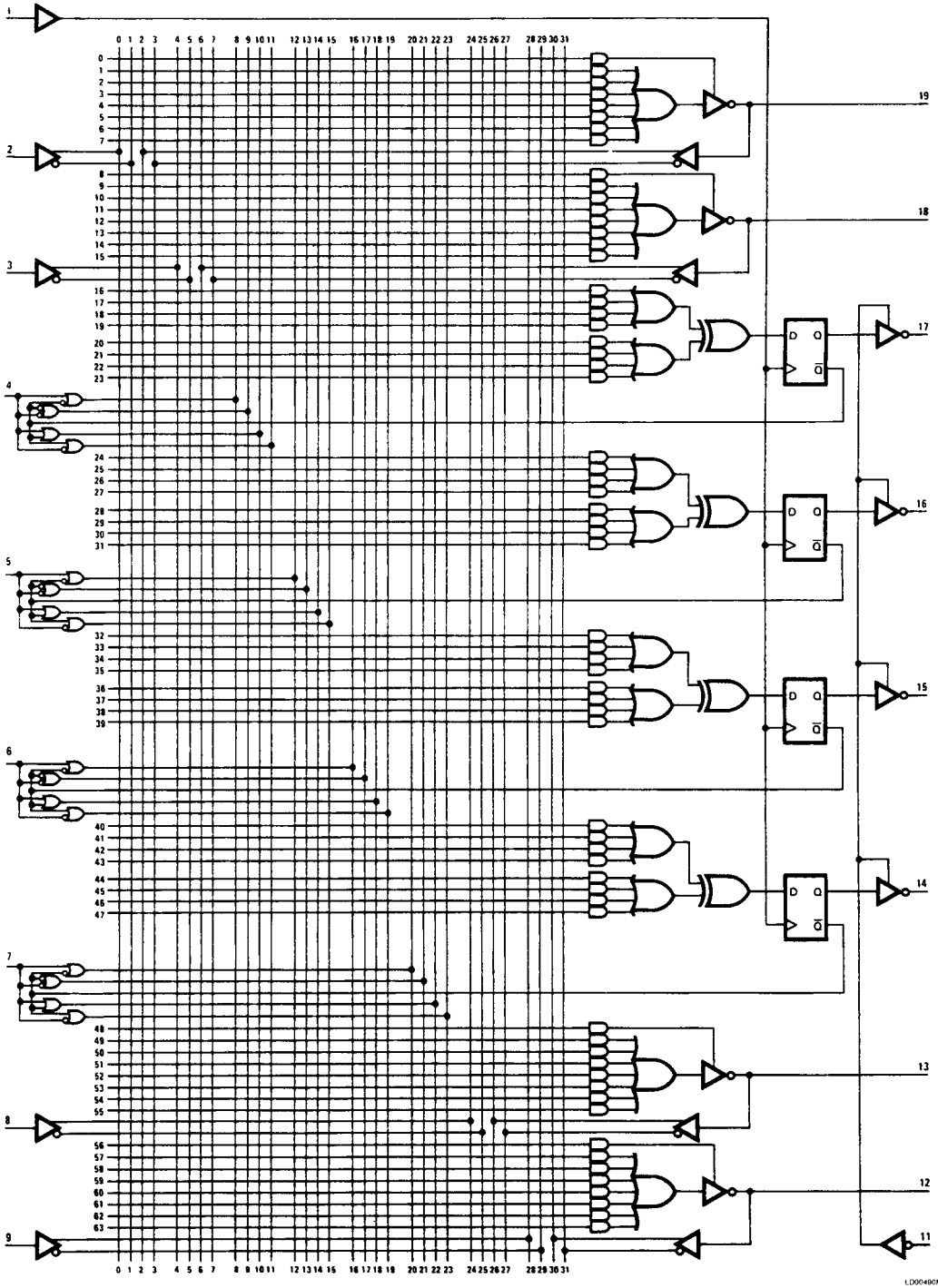
SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OL} = −2mA	2.4	2.8		V
			Com	I_{OL} = −3.2mA				
I_{OZL}[2]	Off-state output current	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}[2]				V_O = 2.4V			100	μA
I_{OS}[3]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	16X4			160	225	mA
			16A4			170	240	

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	R_1 = 200Ω, R_2 = 390Ω		30	45		30	40	ns
t_{CLK}	Clock to output or feedback			15	25		15	25	ns
t_{PZX}	Pin 11 to output enable			15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable			15	25		15	25	ns
t_{PZX}	Input to output enable			30	45		30	40	ns
t_{PXZ}	Input to output disable			30	45		30	40	ns
f_{MAX}	Maximum frequency		12	22		14	22		MHz

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

16X4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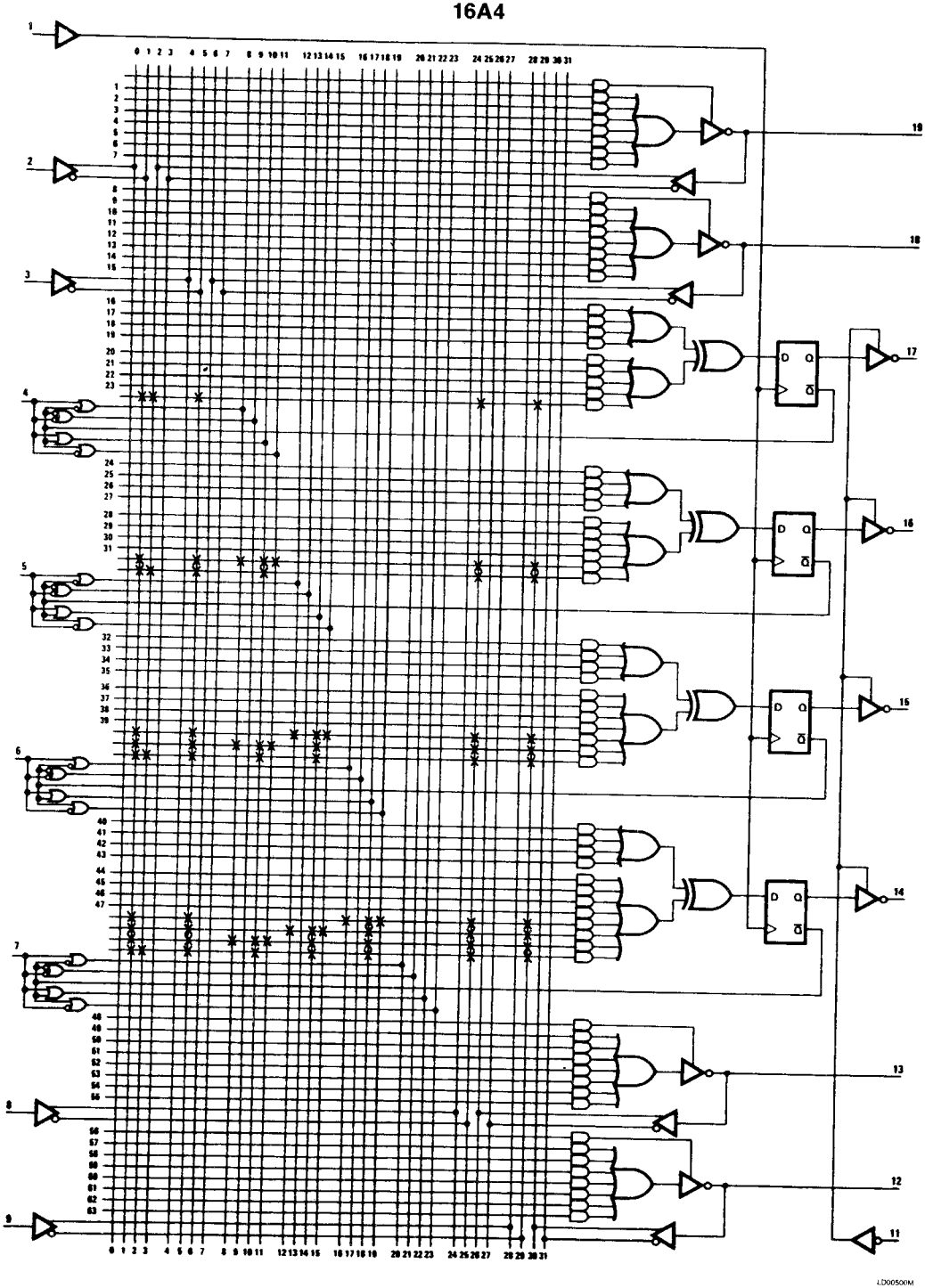
16A4



Large 20RA (PAL16RA8)

Description

The PAL16RA8 is a 20-pin registered asynchronous PAL device. It is a 20-pin version of the original asynchronous PAL device, the PAL20RA10. This versatile device features programmable clock, enable, set, and reset, all of which can operate asynchronously to other flip-flops in the same device. It also has individual flop-flop bypass, allowing this one device to provide any combination of registered and combinatorial outputs.

Programmable Clock

The clock input to each flip-flop comes from the programmable array, allowing the flip-flops to be clocked independently if desired.

Programmable Set and Reset

Each flip-flop has a product line for asynchronous set and one product for asynchronous reset. If the chosen product line is high, the flip-flop will set (become a logic HIGH), or reset (become a logic LOW). The sense of the output pin is inverted if the output is active low.

Programmable Polarity

Each flip-flop has individually programmable polarity. The unprogrammed state is active low.

Programmable Flip-flop Bypass

If both the set and reset product lines are high, the flip-flop is bypassed and the output becomes combinatorial. Thus each output can be configured to be registered or combinatorial.

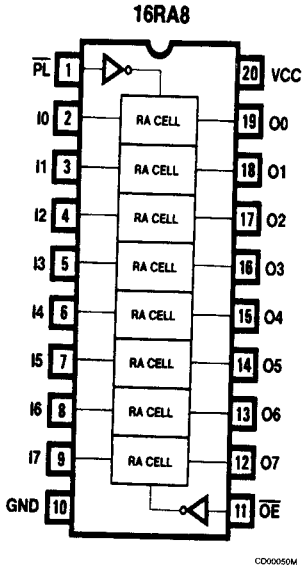
Programmable and Hard-Wired Three-State Outputs

The PAL16RA8 provides a product term dedicated to output control. There is also an output control pin (pin 11). The output is enabled if both the output control pin is low and the output control product term is high. If the output control pin is high all outputs will be disabled. If an output control product term is low, then that output will be disabled.

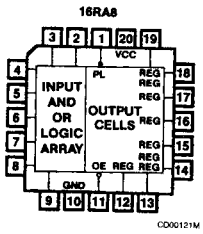
Register Preload and Power-up Reset

Each device also offers register preload for device testability. The registers can be preloaded from the outputs by using TTL level signals in order to simplify functional testing. This series also offers Power-up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

DIP Pinout



PLCC Pinout



Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1] MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock		20	13		ns
t_{wp}	Preload pulse width		35	15		ns
t_{su}	Setup time for input or feedback to clock		20	10		ns
t_{sup}	Preload setup time		25	5		ns
t_h	Hold time	Polarity fuse intact	10	−2		ns
		Polarity fuse blown	0	−6		
t_{hp}	Preload hold time		25	5		ns
T_A	Operating free-air temperature		0		75	°C
T_C	Operating case temperature					°C

Electrical Characteristics Over Operating Conditions

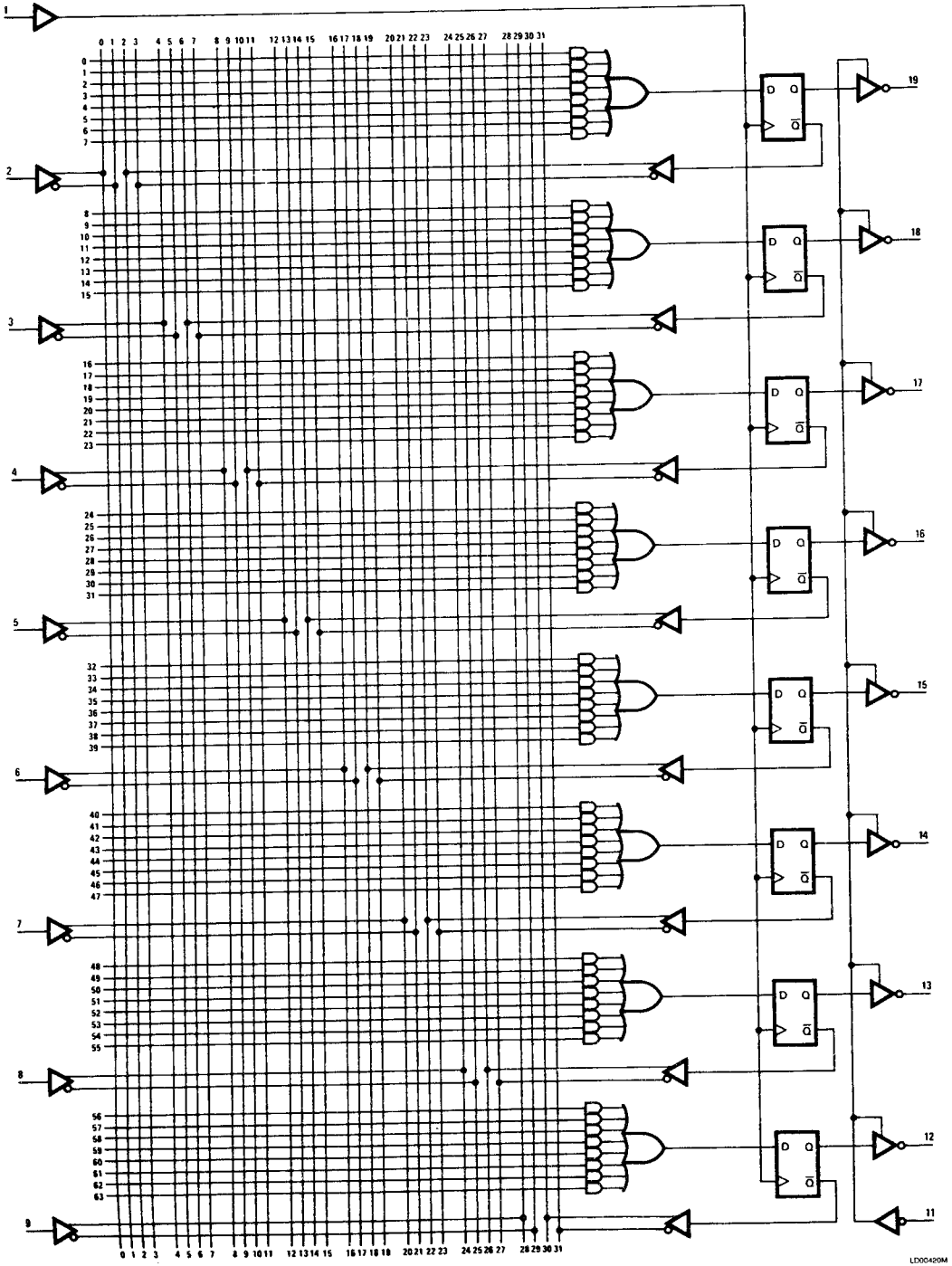
SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	2.8		V
I_{OZ}[3]	Off-state output current	V_{CC} = MAX	V_O = 2.4V/V_O = 0.4V	−100		100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			135	170	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output	Polarity fuse intact			20	30	ns
		Polarity fuse blown			25	35	
t_{CLK}	Clock to output or feedback			10	17	30	ns
t_S	Input to asynchronous set				22	35	ns
t_R	Input to asynchronous reset		R_1 = 560Ω		27	40	ns
t_{PZX}	Pin 11 to output enable		R_2 = 1.1KΩ		10	20	ns
t_{PXZ}	Pin 11 to output disable				10	20	ns
t_{PZX}	Input to output enable				18	30	ns
t_{PXZ}	Input to output disable				15	30	ns
f_{MAX}	Maximum frequency			20	35		MHz

1. The PAL20RA Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

16RA8


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
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LD00420M

Small 24 Series

	INPUTS	OUTPUTS	POLARITY	T_{PD} (ns)	I_{CC} (mA)
PAL12L10	12	10	LOW	40	100
PAL14L8	14	8	LOW	40	100
PAL16L6	16	6	LOW	40	100
PAL18L4	18	4	LOW	40	100
PAL20L2	20	2	LOW	40	100
PAL20C1	20	2	LOW	40	100

Description

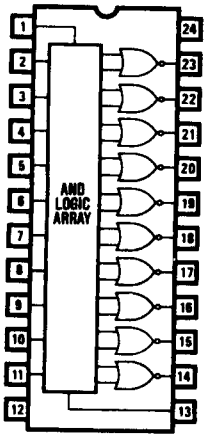
The Small 24 Series is made up of six combinatorial 24-pin PAL devices. They implement simple combinatorial logic, with no feedback.

Performance

The standard series has a propagation delay (tpd) of 40 nanoseconds (ns). Standard supply current is 100 milliamps (mA).

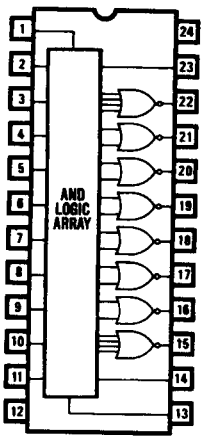
DIP Pinouts

12L10



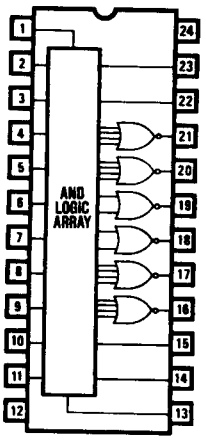
CD00580M

14L8



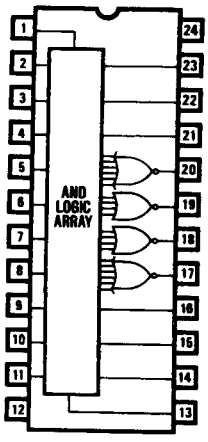
CD00590M

16L6



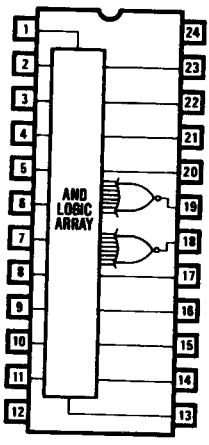
CD00130M

18L4



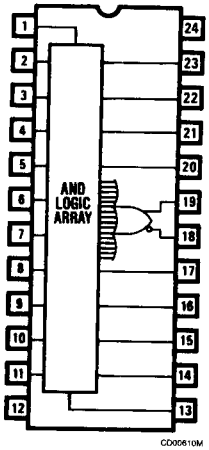
CD00570M

20L2



CD00600M

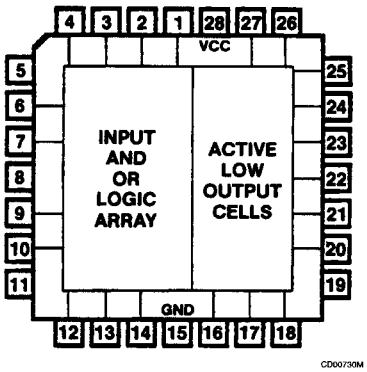
20C1



CD00610M

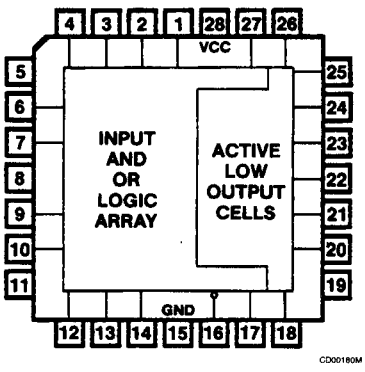
PLCC Pinouts

12L10



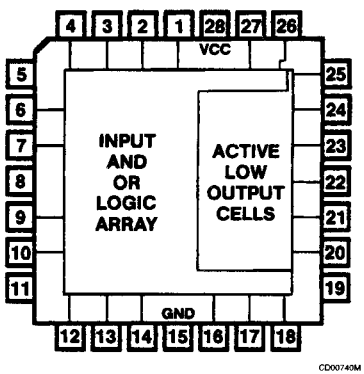
CD00730M

14L8



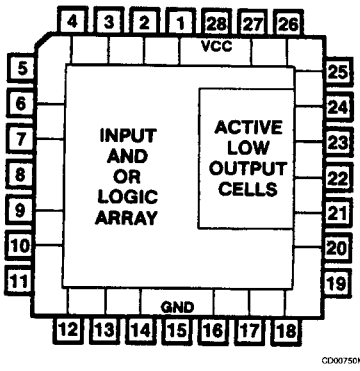
CD00180M

16L6



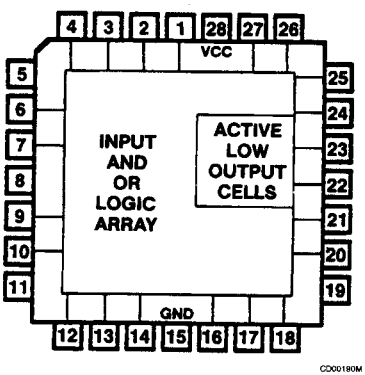
CD00740M

18L4



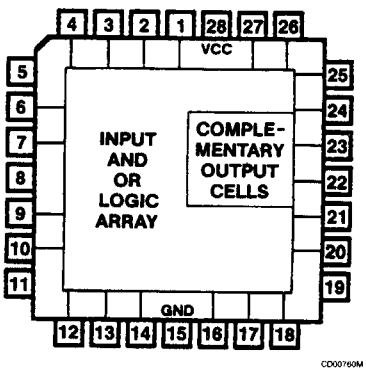
CD00750M

20L2



CD00180M

20C1



CD00760M

2

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55			0		75	°C
T_C	Operating case temperature			125				°C

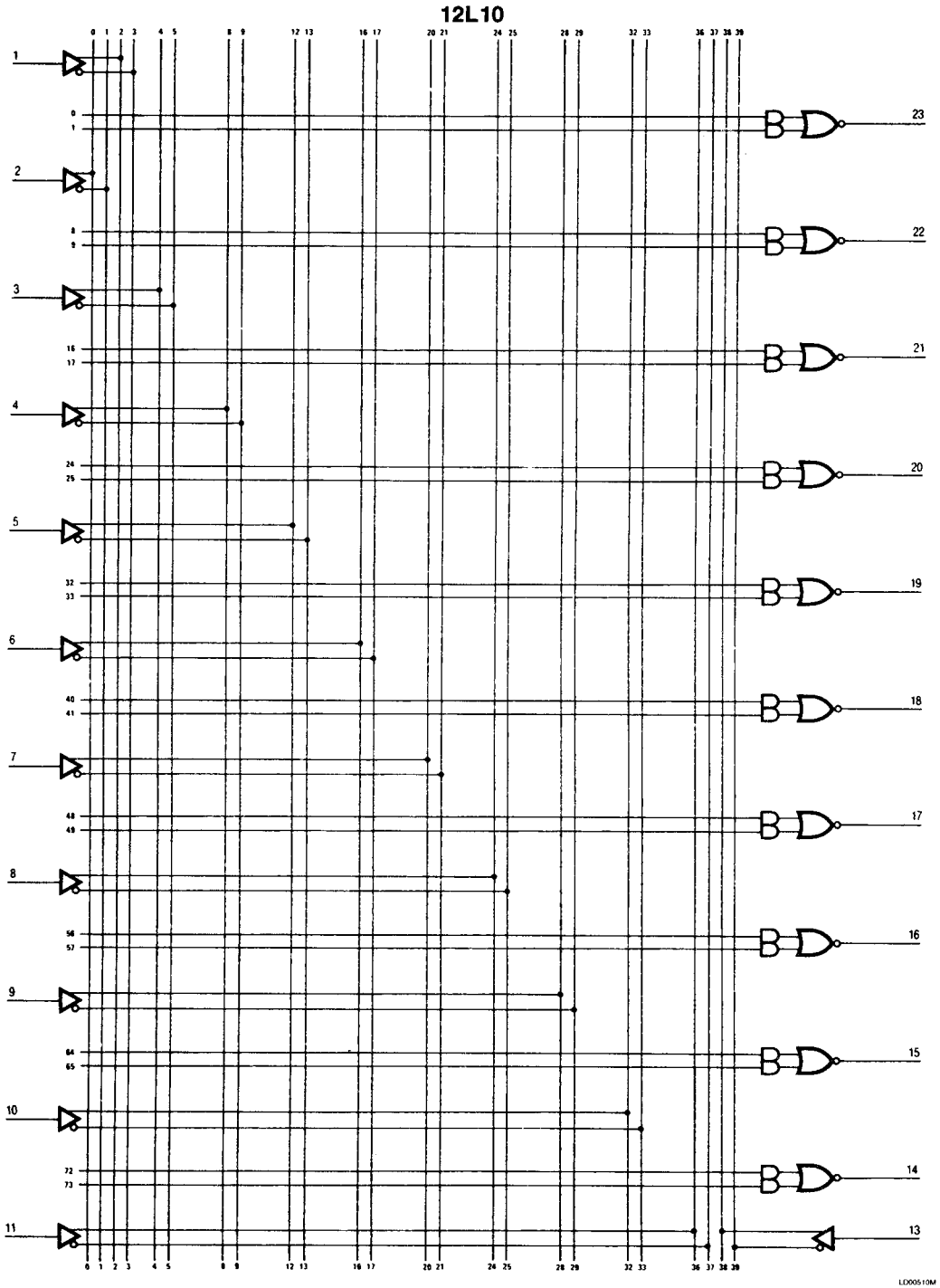
Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_1 = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OS}[2]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	R1 = 560Ω R2 = 1.1kΩ		25	45		25	40	ns

1. These are absolute values with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.


12L10
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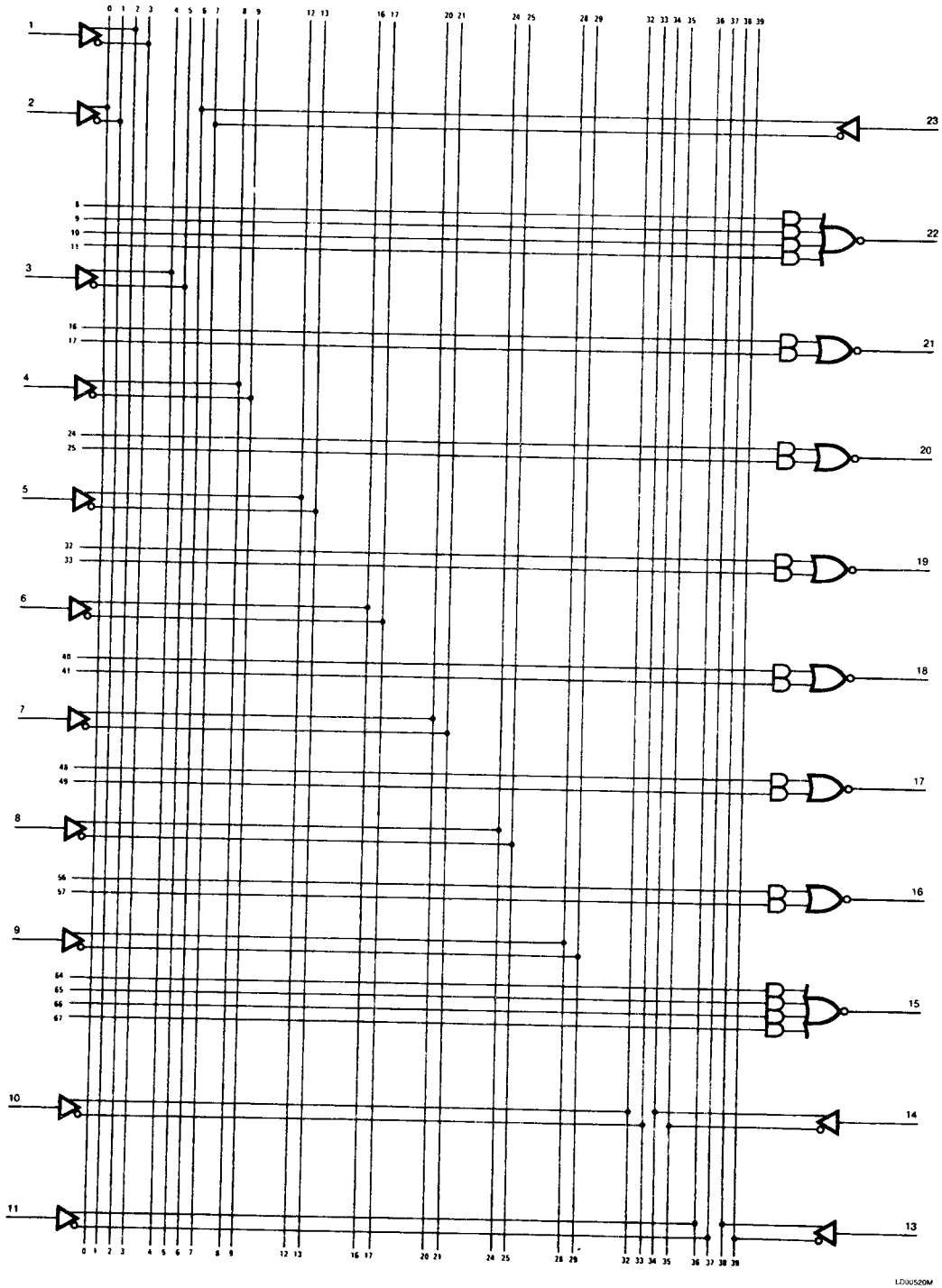
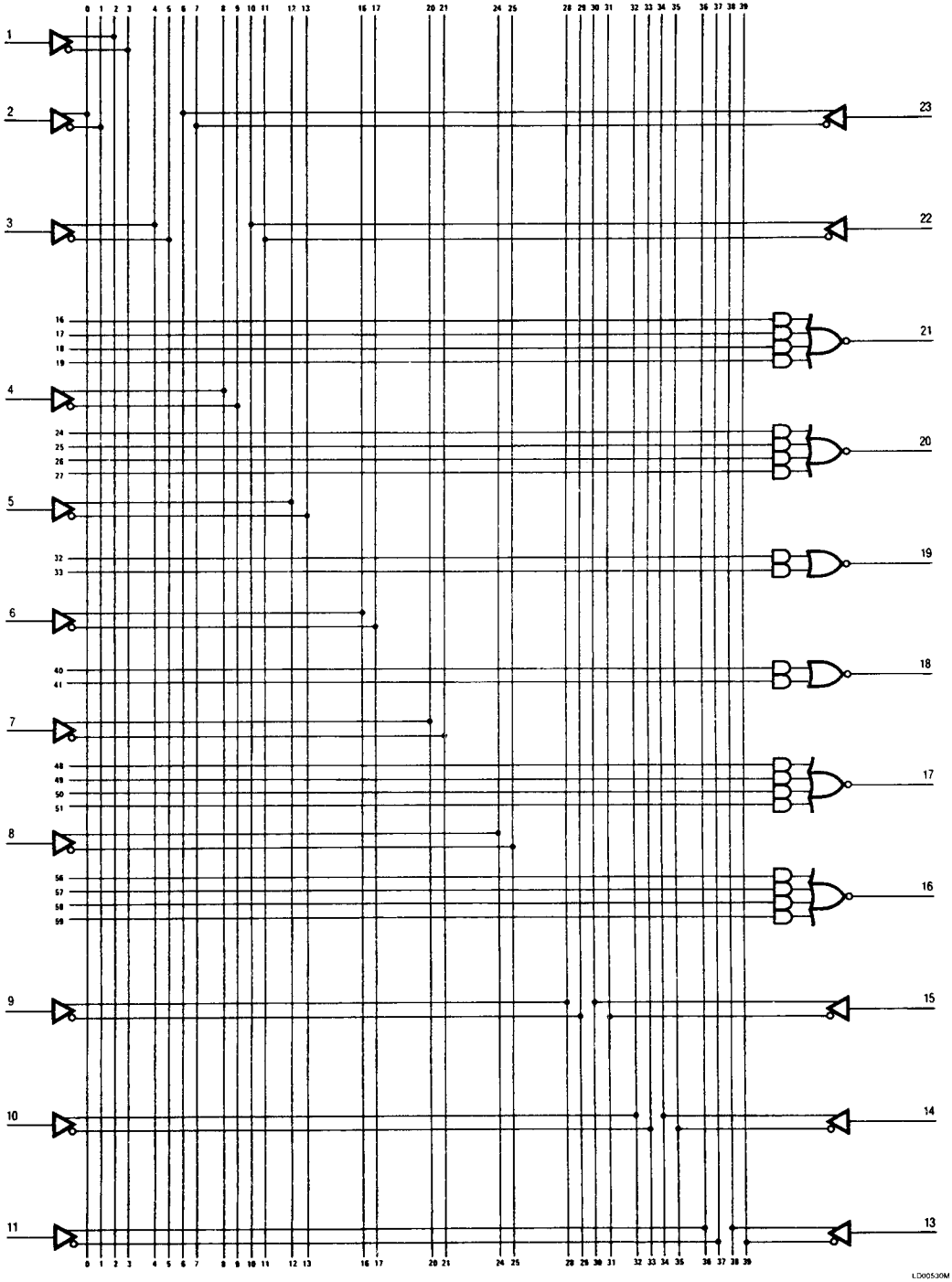
LD00510M

14L8



LD00520M

16L6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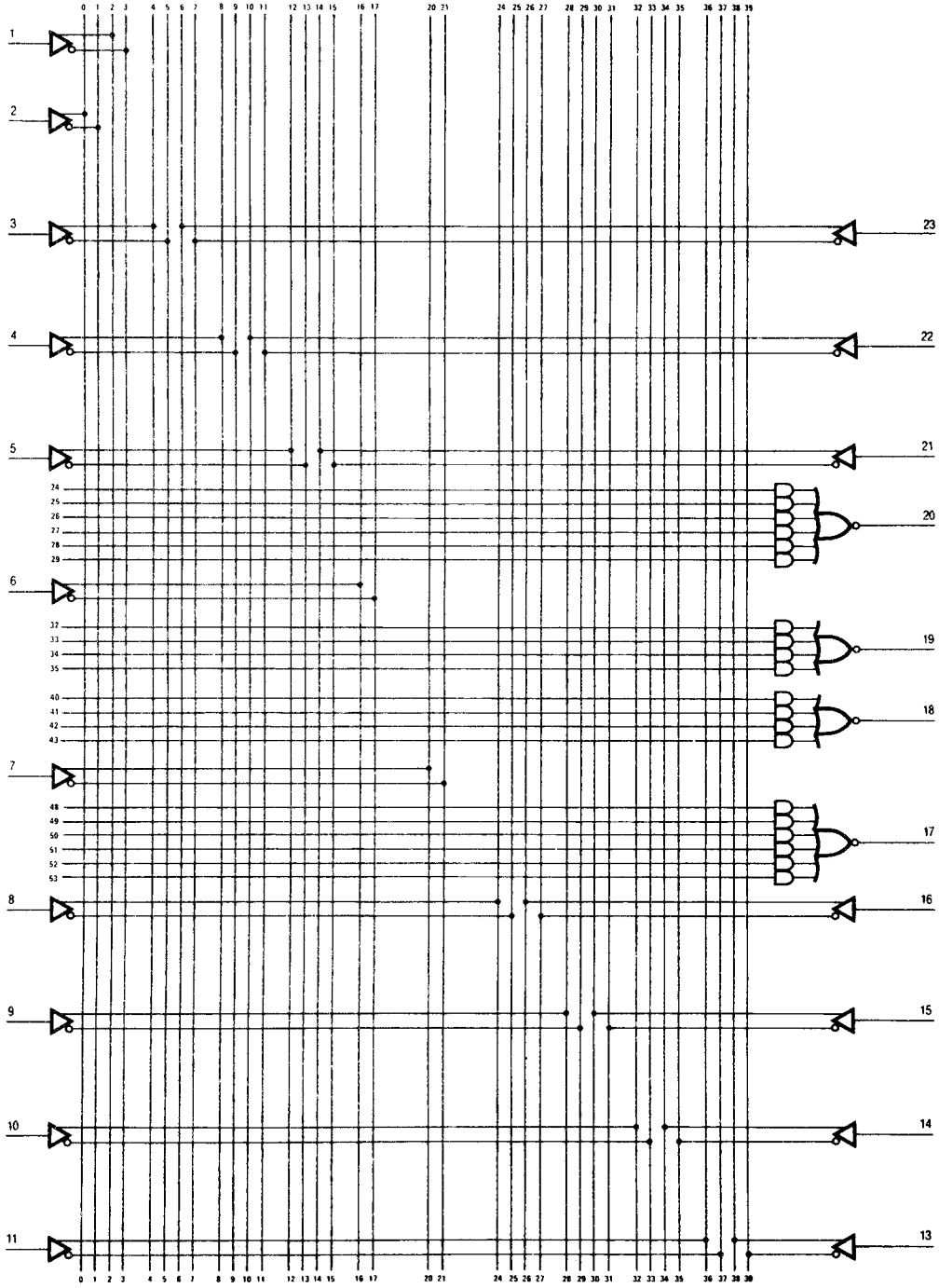
LD00530M

18L4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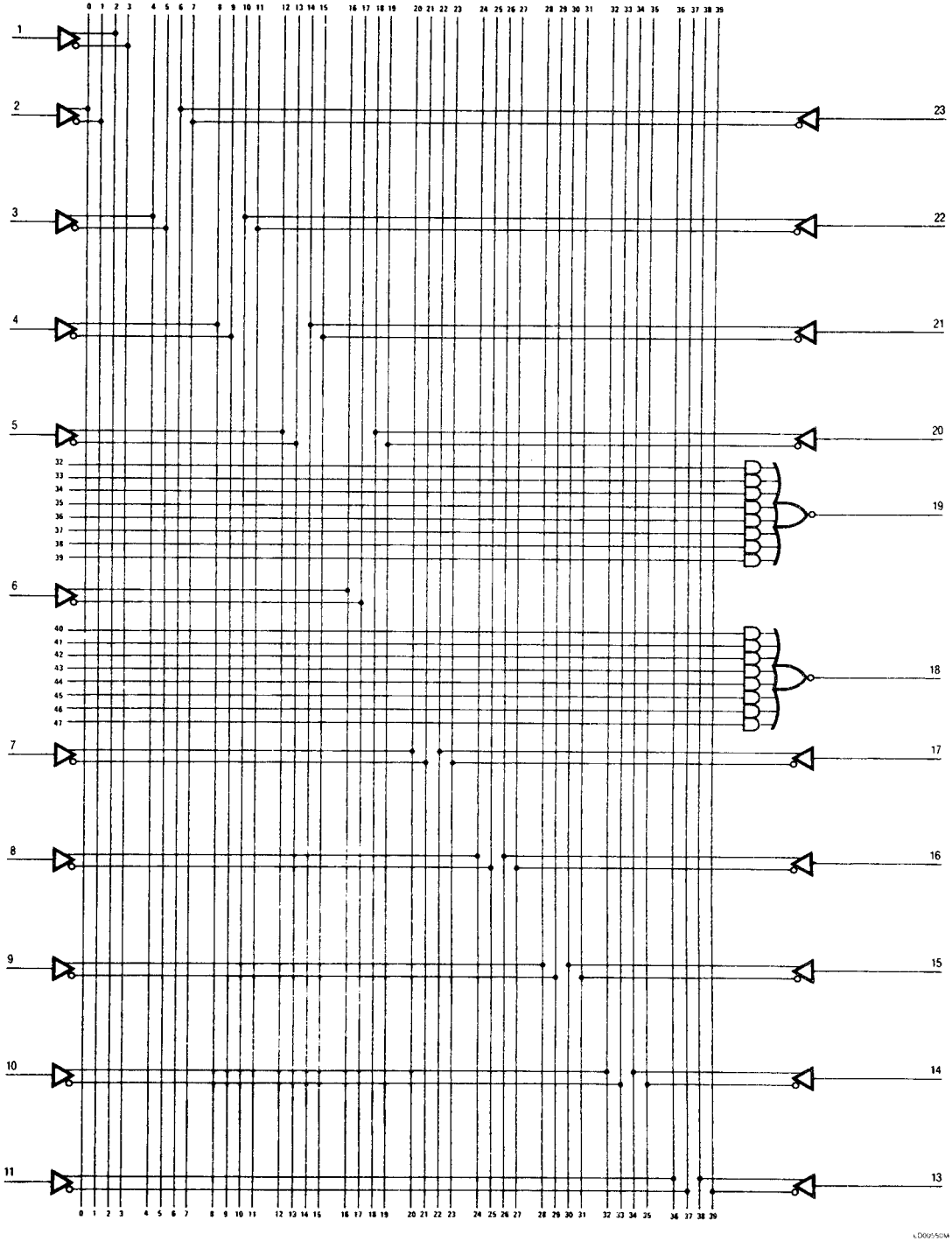
48 49 50 51 52 53
LD00540M

20L2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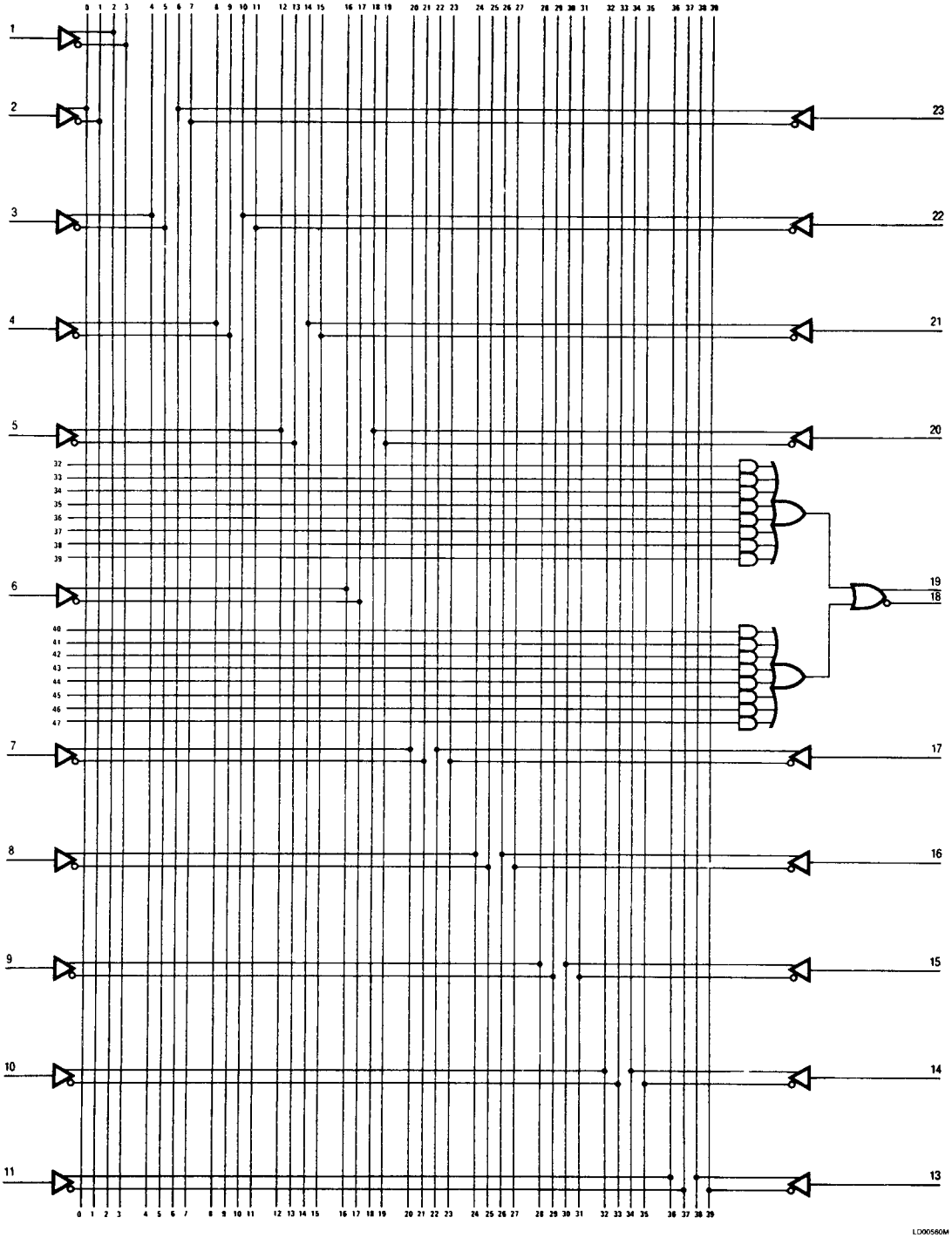
20C1



LD00560M

Small 24A Decoder Series

	INPUTS	OUTPUTS	t_{PD} (ns)	I_{CC} (mA)
PAL6L16A	6	16	25	90
PAL8L14A	8	14	25	90

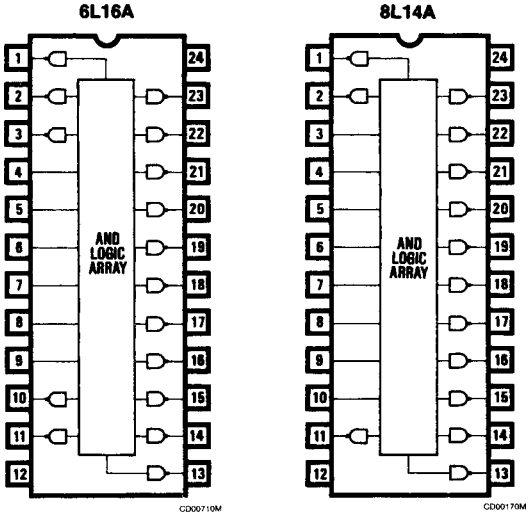
Description

The Small 24A Decoder Series provides a wide number of outputs, especially useful in decoding applications. These two parts implement simple combinatorial logic.

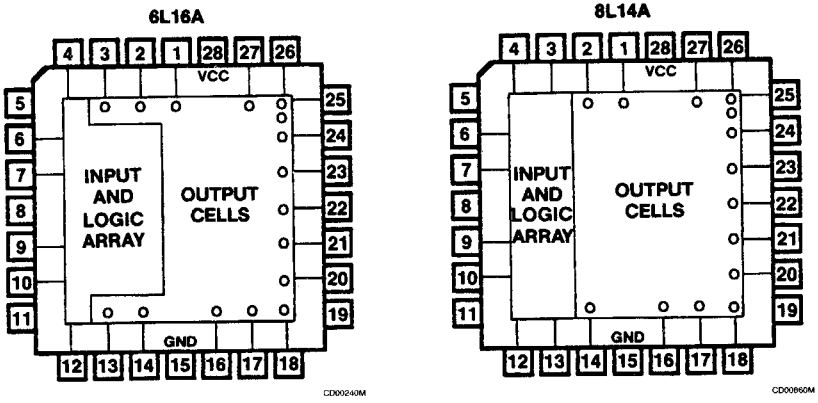
Performance

These devices offer 25ns speed at only 90mA supply current.

DIP Pinouts



PLCC Pinouts



Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL[1]			UNIT
		MIN	TYP	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
T_A	Operating free-air temperature	0	25	75	°C

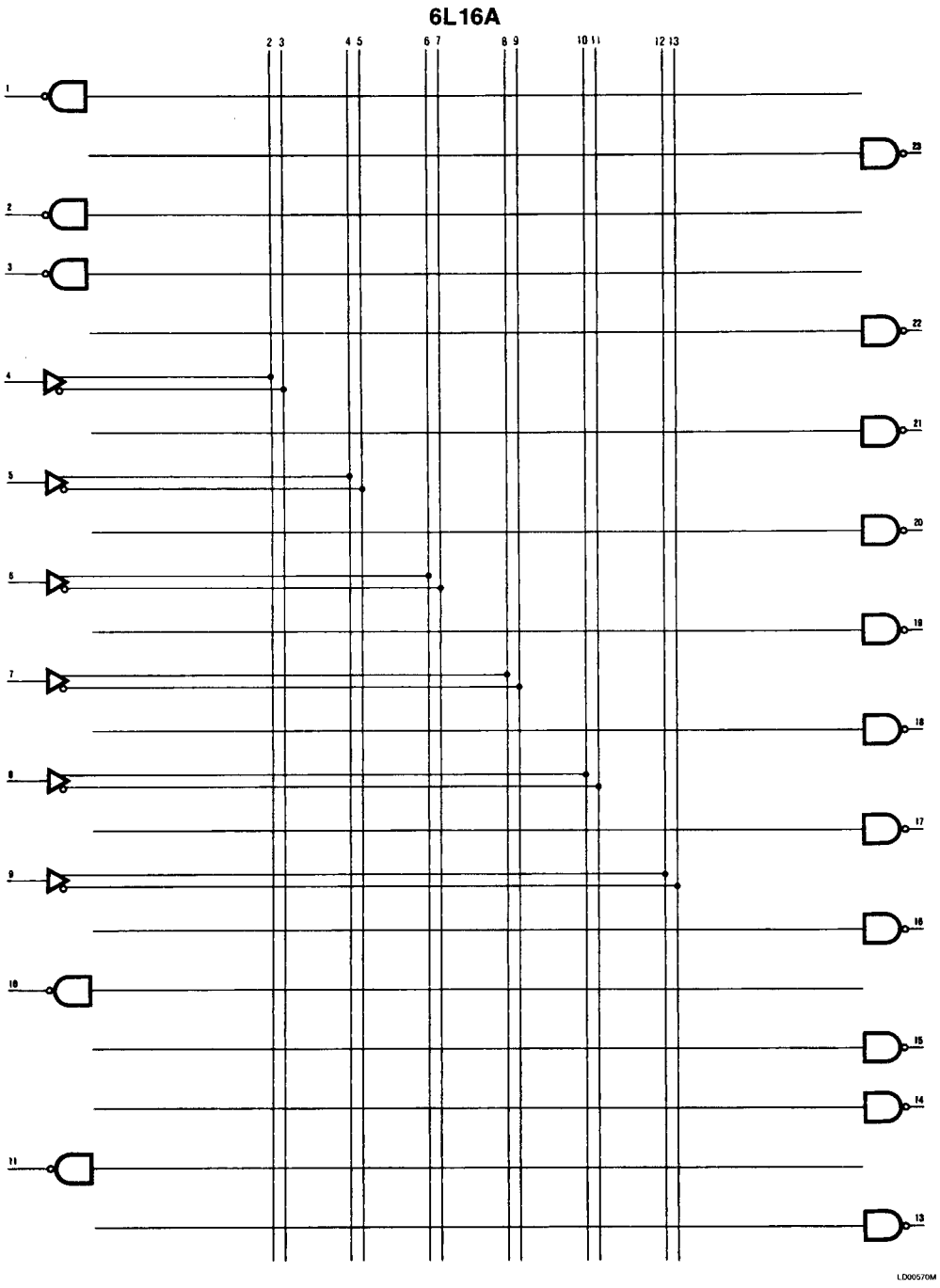
Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	2.8		V
I_{OS}[3]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			60	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL			UNIT
			MIN	TYP	MAX	
t_{PD}	Input to output propagation delay	R_1 = 560Ω R_2 = 1.1KΩ		15	25	ns

1. The PAL24A Decoder Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.


6L16A
2 3
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6 7
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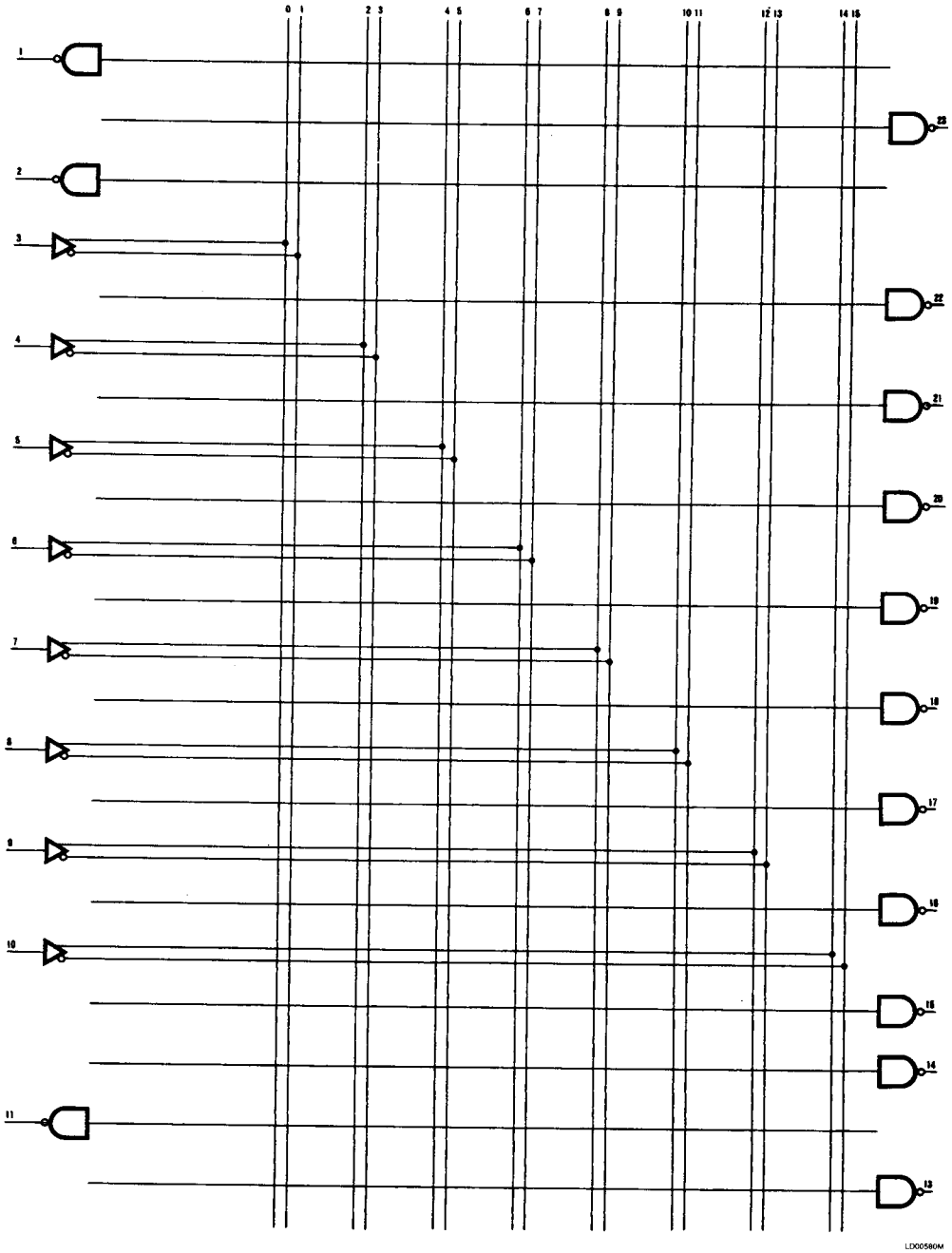
LD00570M

8L14A


0 1
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LD00580M

Medium 24 Series

	DEDICATED INPUTS	OUTPUTS	
		COMBINATORIAL	REGISTERED
PAL20L8	12	8 (6 I/O)	0
PAL20R8	10	0	8
PAL20R6	10	2 I/O	6
PAL20R4	10	4 I/O	4

Description

The Medium 24 Series consists of four devices, each with twenty array inputs and eight outputs. The devices have either 0, 4, 6, or 8 registered outputs, with the remaining being combinatorial. Each of the registered outputs feeds back into the array, for sequential designs. The combinatorial outputs also feed back into the array, except for two of the outputs on the 20L8. This feedback allows the output to also operate as an input if the output is disabled.

Enable

The combinatorial outputs are enabled by a product term. The registered outputs are enabled by a common enable pin.

Polarity

All outputs are active low.

Performance

Several speed/power versions are available:

Suffix	t_{PD} (ns)	I_{CC} (mA)
A	25	210
A-2	35	105
B	15	210
B-2 *	25	105

* contact Monolithic Memories for datasheet

Preload and Power-up Reset

The B-2 Series offers register preload for device testability. The registers can be preloaded from the outputs by using supervoltages (see waveforms at end of section) in order to simplify functional testing. The B-2 Series also offers Power-up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

CMOS ZPAL™ 24 Series

Features/Benefits

- CMOS technology provides zero standby power
- Lowest power 24-pin PAL® device family; consumes only 3mA/MHz
- 35ns maximum propagation delay
- Programmable replacement for CMOS/TTL logic
- Reduces chip count by greater than six to one
- Instant prototyping and easier board layout
- HC/HCT compatible for use in CMOS or TTL systems
- Offered over both the Commercial and Industrial temperature ranges
- Low-cost, one-time programmable SKINNYDIP® and PLCC packages save board space

Description

The CMOS ZPAL24 Series offers the first family of PAL devices with true CMOS power consumption. Under standby conditions (inputs and clock not changing), the devices consume a maximum current of 100μA, less than 1% that of the quarter-power PAL devices. This low power consumption allows the devices to be powered by a battery almost indefinitely.

While operating, the devices consume additional power only when the inputs or clock change. Power consumption is directly proportional to the frequency of changes to the inputs. I_{CC} is therefore specified as 3mA per 1MHz of operating frequency, starting from 5mA at 1MHz. Thus, the maximum current at 8MHz would be 5mA + 7x3mA, or 26mA.

The devices have HC and HCT compatible inputs and outputs for use in CMOS and TTL systems. This feature allows the ZPAL circuits to be used for direct replacement of discrete CMOS as well as TTL logic.

Areas of Application

- Portable computers
- Battery-operated instrumentation
- Low-power industrial equipment
- Standard CMOS/TTL logic replacement

Features

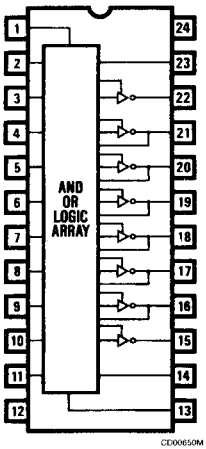
The CMOS ZPAL24 Series includes the four standard 24-pin PAL device architectures. All four devices have twenty array inputs and eight outputs, with varying numbers of registers: zero (20L8), four (20R4), six (20R6), and eight (20R8). The combinatorial outputs on the registered devices, and six of the outputs on the 20L8, are I/O pins that can be individually programmed as inputs or outputs. Each output register, a D-type flip-flop, also feeds back into the array, for implementation of synchronous state machine designs. Registered outputs are enabled by an external input, while the combinatorial outputs use a product term to control the enable function.

The basic PAL device architecture is a programmable AND array feeding a fixed OR array. The programmable AND array consists of a set of cells similar to those used in EPROMs. Erasable by UV light, the cells can be programmed and erased in the factory to ensure 100% programming and functional yields.

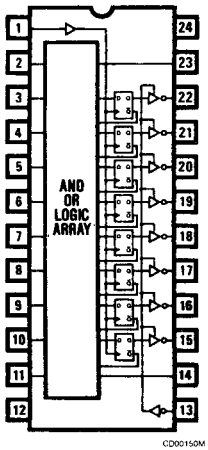
Windowed packages will be made available in the future, allowing erasure in the field. Windowed packages allow easy prototype testing and reconfiguration.

DIP Pinouts

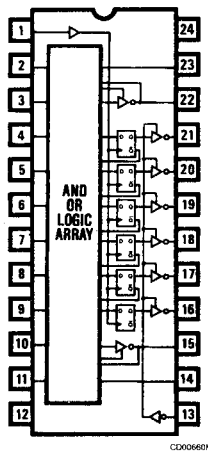
20L8A/A-2/B



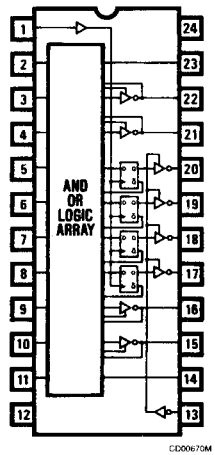
20R8A/A-2/B



20R6A/A-2/B

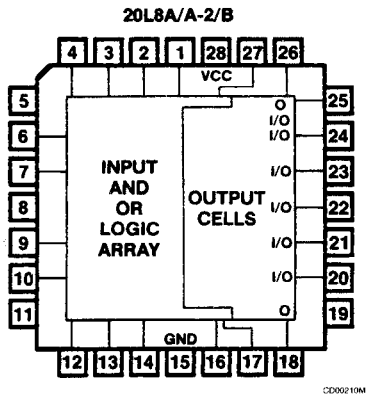


20R4A/A-2/B

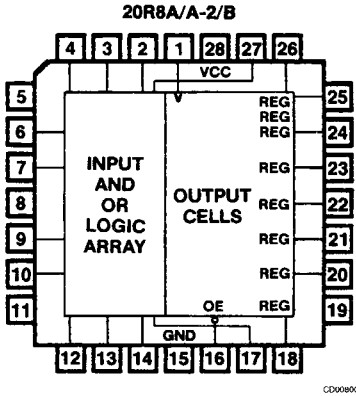


PLCC Pinouts

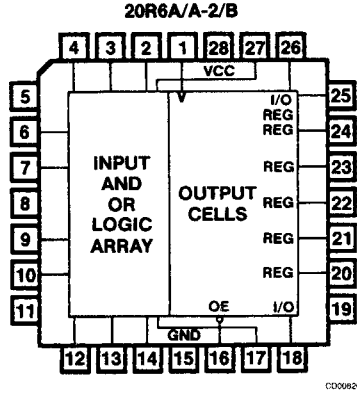
20L8A/A-2/B



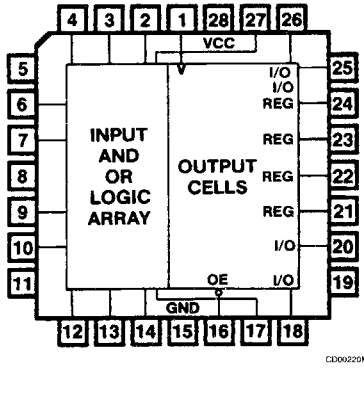
20R8A/A-2/B



20R6A/A-2/B



20R4A/A-2/B



Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	7		15	7		ns
		High	20	7		15	7		
t_{su}	Set up time from input or feedback to clock	20R8A 20R6A 20R4A	30	15		25	15		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −2mA	2.4	2.8		V
			Com	I_{OH} = −3.2mA				
I_{OZL}[2]	Off-state output current	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}[2]				V_O = 2.4V			100	μA
I_{OS}[3]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−90	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				160	210	mA

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	20R6A 20R4A 20L8A	$R_1 = 200\Omega$ $R_2 = 390\Omega$		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 13 to output enable except 20L8A				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable except 20L8A				11	25		11	20	ns
t_{PZX}	Input to output enable	20R6A 20R4A 20L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	20R6A 20R4A 20L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	20R8A 20R6A 20R4A		20	40		28.5	40		MHz

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1] MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	25	10		ns
		High	25	10		
t_{su}	Setup time from input or feedback to clock	20R8A-2, 20R6A-2, 20R4A-2	35	25		ns
t_h	Hold time		0	−15		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			80	105	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	TYP	MAX	COMMERCIAL MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output 20L8A-2 20R6A-2 20R4A-2	Commercial R_1 = 200Ω R_2 = 390Ω		25	50		25	35	ns
t_{CLK}	Clock to output or feedback except 20L8A-2			15	25		15	25	ns
$t_{PXZ/ZX}$	Pin 13 to output disable/enable except 20L8A-2			15	25		15	25	ns
t_{PZX}	Input to output enable 20L8A-2 20R6A-2 20R4A-2			25	45		25	35	ns
t_{PXZ}	Input to output disable 20L8A-2 20R6A-2 20R4A-2			25	45		25	35	ns
f_{MAX}	Maximum frequency 20R8A-2 20R6A-2 20R4A-2		14	19		16	19		MHz

1. The PAL24A-2 Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Operating Conditions

SYMBOL	PARAMETER			COMMERCIAL[1] MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
t_w	Width of clock	Low	20R8B, 20R6B, 20R4B	10	6		ns
		High		12	8		
t_{su}	Setup time from input or feedback to clock			15	10		ns
t_h	Hold time			0	−10		ns
T_A	Operating free-air temperature			0	25	75	°C

Electrical Characteristics Over Operating Conditions

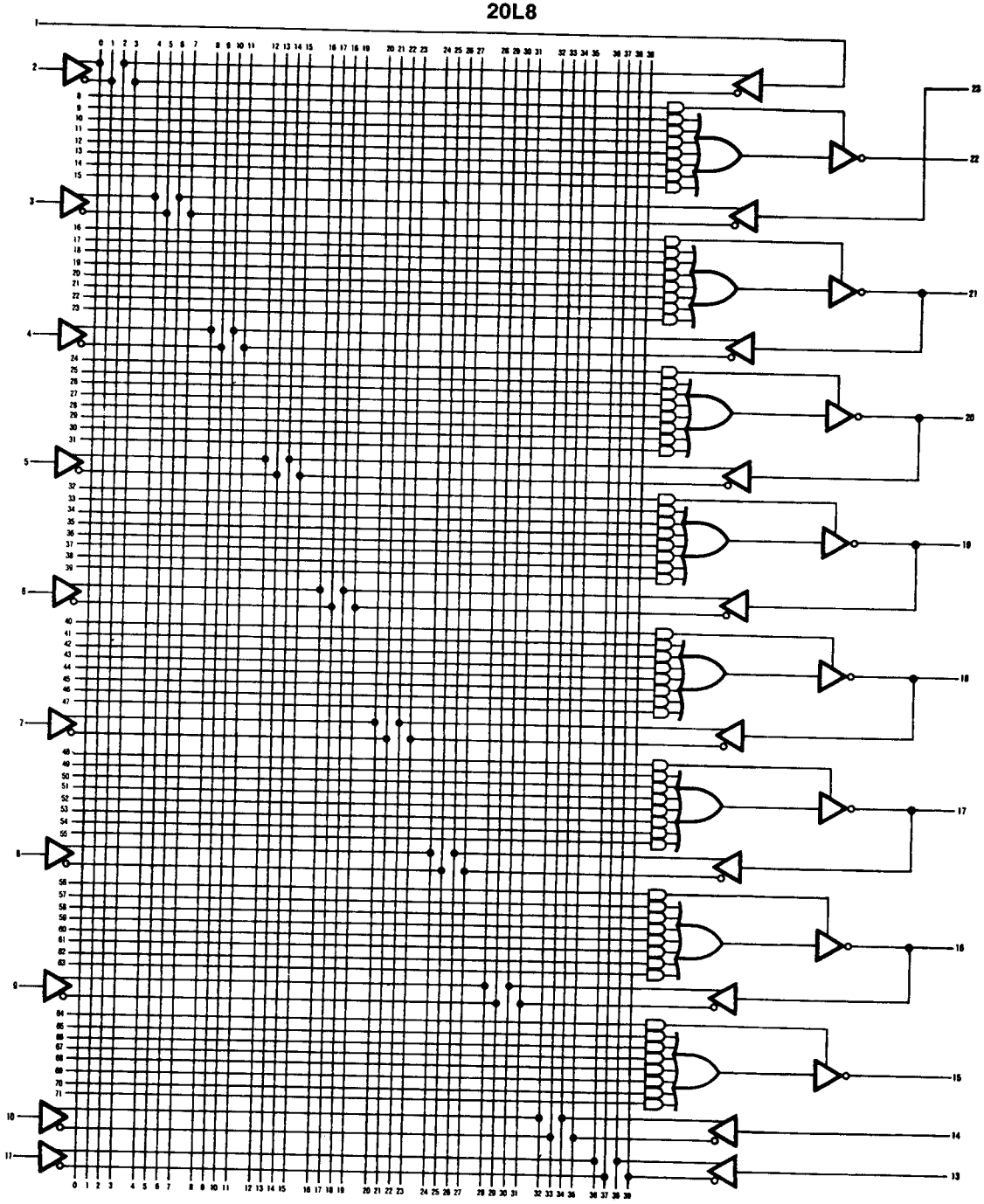
SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			140	210	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output 20L8B, 20R6B, 20R4B		Commercial R_1 = 200Ω R_2 = 390Ω		12	15	ns
t_{CLK}	Clock to output or feedback except 20L8B				8	12	ns
t_{PZX}	Pin 13 to output enable except 20L8B				10	15	ns
t_{PXZ}	Pin 13 to output disable except 20L8B				8	12	ns
t_{PZX}	Input to output enable 20R6B, 20R4B, 20L8B				12	18	ns
t_{PXZ}	Input to output disable 20R6B, 20R4B, 20L8B				12	15	ns
f_{MAX}	Maximum frequency 20R8B, 20R6B, 20R4B	Feedback		37	40		MHz
		No feedback		45	50		

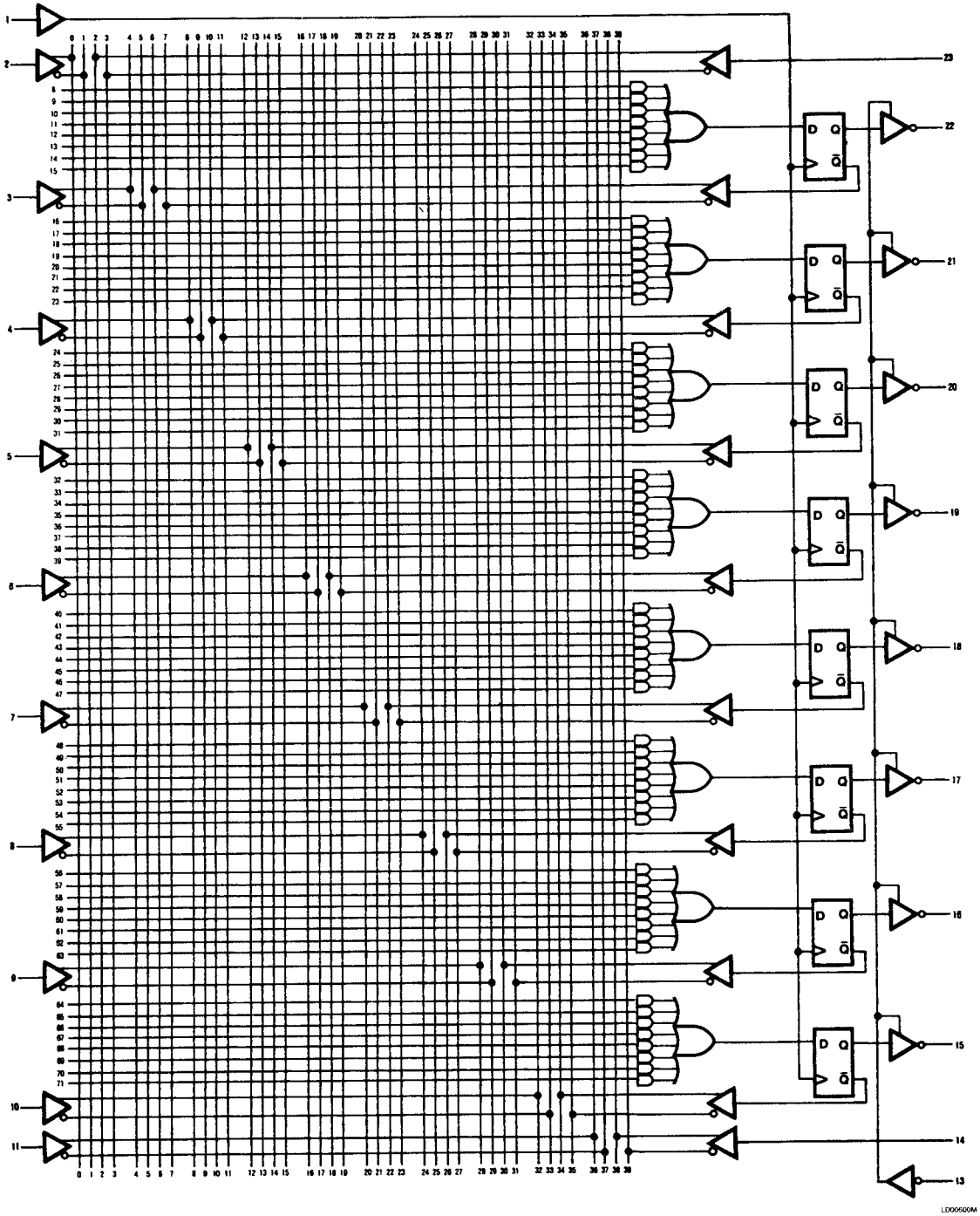
1. The PAL24B Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

20L8

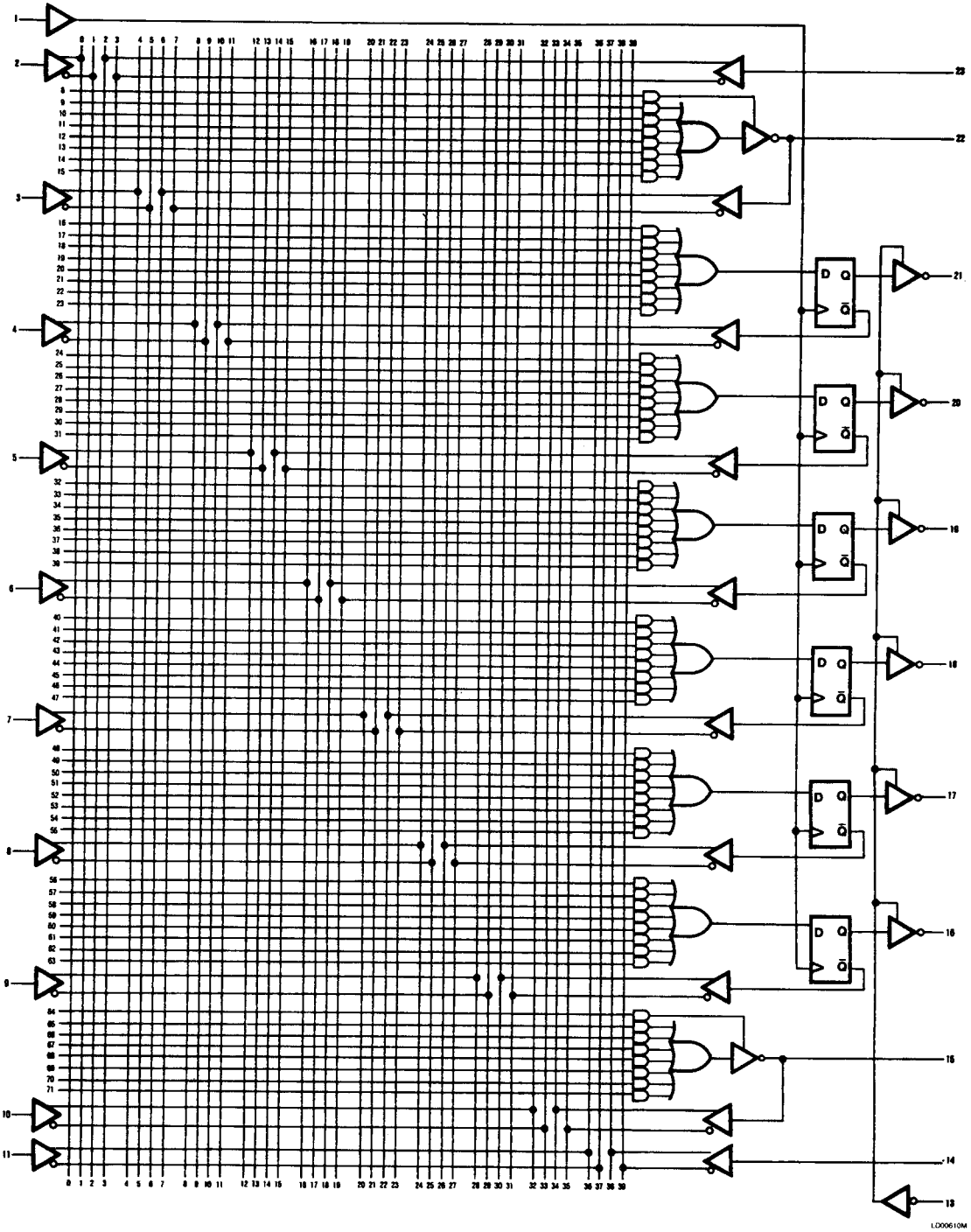


LD00590M

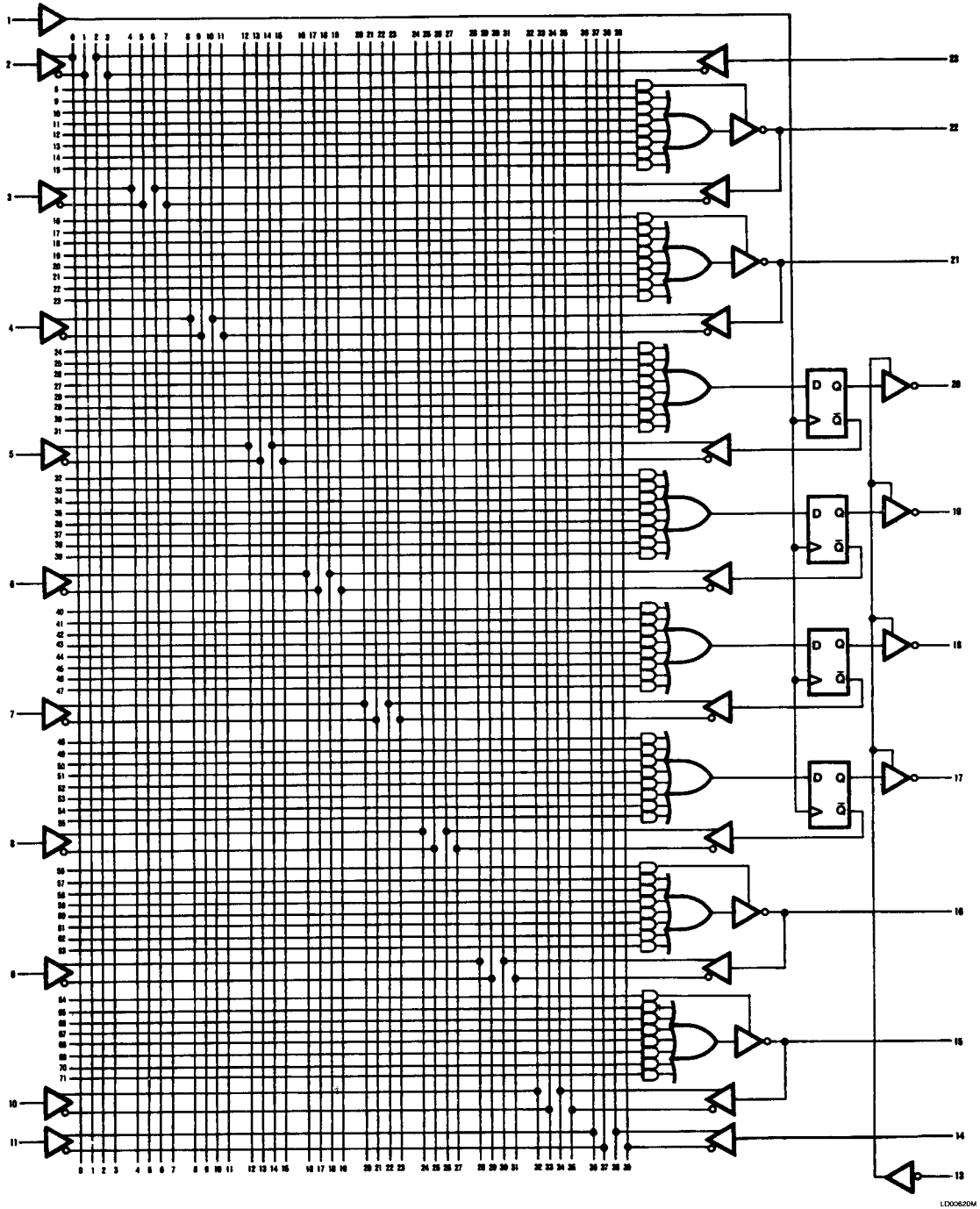
20R8



20R6



20R4



Medium 24X Series

	ARRAY INPUTS	OUTPUTS		STANDARD		HIGH SPEED	
		COMBINATORIAL	REGISTERED	t_{PD} (ns)	I_{CC} (mA)	t_{PD} (ns)	I_{CC} (mA)
PAL20L10	20	10	0	50	165	30	165
PAL20X10	20	0	10	50	180	30	180
PAL20X8	20	2	8	50	180	30	180
PAL20X4	20	6	4	50	180	30	180

Description

The PAL24X Series offers Exclusive-OR (XOR) gates preceding each register. The XOR gate has as its inputs two sums, each of two product terms. The XOR gate is very efficient for counting applications.

Enable

The combinatorial outputs are enabled by a product term. The registered outputs are enabled by a common enable pin.

Polarity

All outputs are active low.

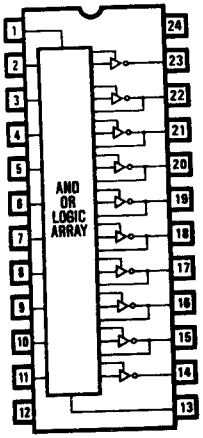
Preload and Power-up Reset

The 24XA Series offers register preload for device testability. The registers can be preloaded from the outputs by using supervoltages (see waveforms at end of section) in order to simplify functional testing. The 24XA Series also offers Power-up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

2

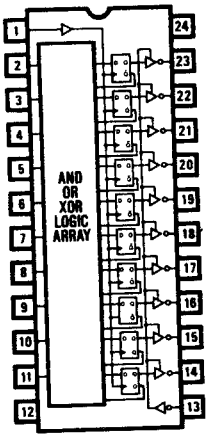
DIP Pinouts

20L10/A



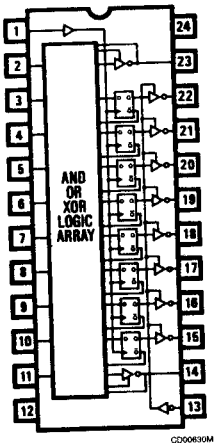
CD00620M

20X10/A



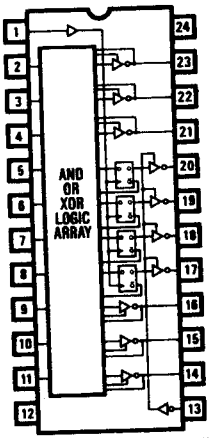
CD00140M

20X8/A



CD00630M

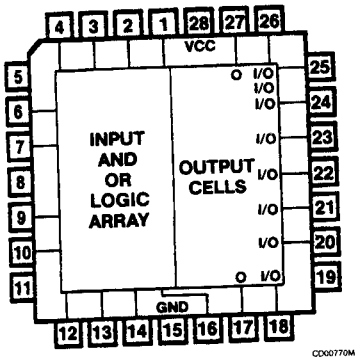
20X4/A



CD00640M

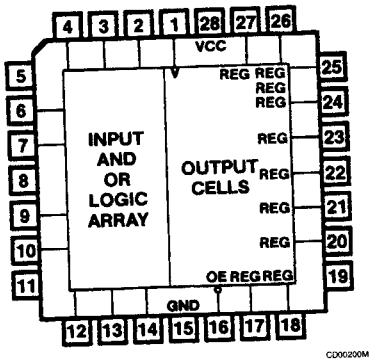
PLCC Pinouts

20L10/A



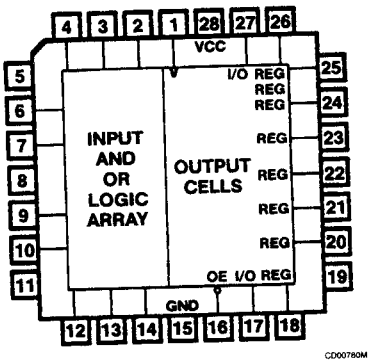
CD00770M

20X10/A



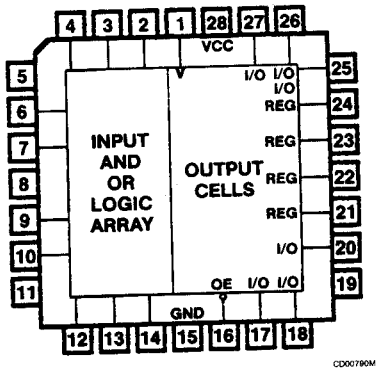
CD00200M

20X8/A



CD00780M

20X4/A



CD00790M

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40	20		35	20		ns
		High	30	10		25	10		
t_{su}	Setup time from input or feedback to clock	20X10, 20X8, 20X4	60	38		50	38		ns
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics (Over Operating Conditions)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −2mA	2.4	2.8		V
			Com	I_{OH} = −3.2mA				
I_{OZL}[2]	Off-state output current	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}[2]				V_O = 2.4V			100	μA
I_{OS}[3]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	20X10	20X8 20X4		120	180	mA
I_{CC}	Supply current	V_{CC} = MAX	20L10			90	165	mA

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics (Over Operating Conditions)

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output 20X8, 20X4, 20L10	$R_1 = 200\Omega$ $R_2 = 390\Omega$		35	60		35	50	ns
t_{CLK}	Clock to output or feedback except 20L10			20	35		20	30	ns
$t_{PXZ/ZX}$	Pin 13 to output disable/enable except 20L10			20	45		20	35	ns
t_{PZX}	Input to output enable except 20X10			35	55		35	45	ns
t_{PXZ}	Input to output disable except 20X10			35	55		35	45	ns
f_{MAX}	Maximum frequency 20X10, 20X8, 20X4		10.5	16		12.5	16		MHz

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1] MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	25	15		ns
		High	15	7		
t_{su}	Setup time from input or feedback to clock	20X10A, 20X8A, 20X4A	30	20		ns
t_h	Hold time		0	−15		ns
T_A	Operating free-air temperature		0	25	75	°C

Electrical Characteristics (Over Operating Conditions)

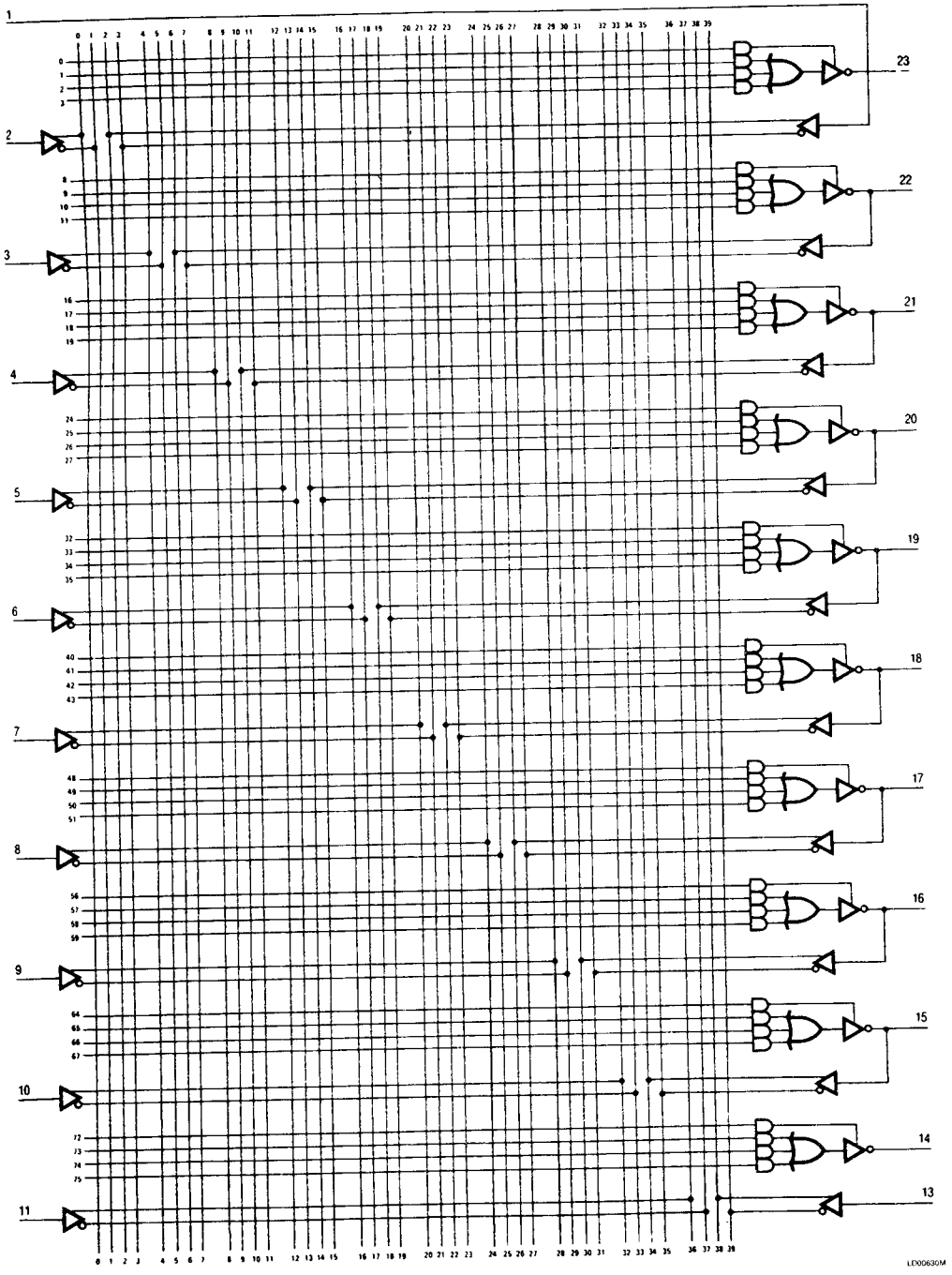
SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 24mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = MAX	20X10A,20X8A,20X4A		140	180	mA
			20L10A		115	165	

Switching Characteristics (Over Operating Conditions)

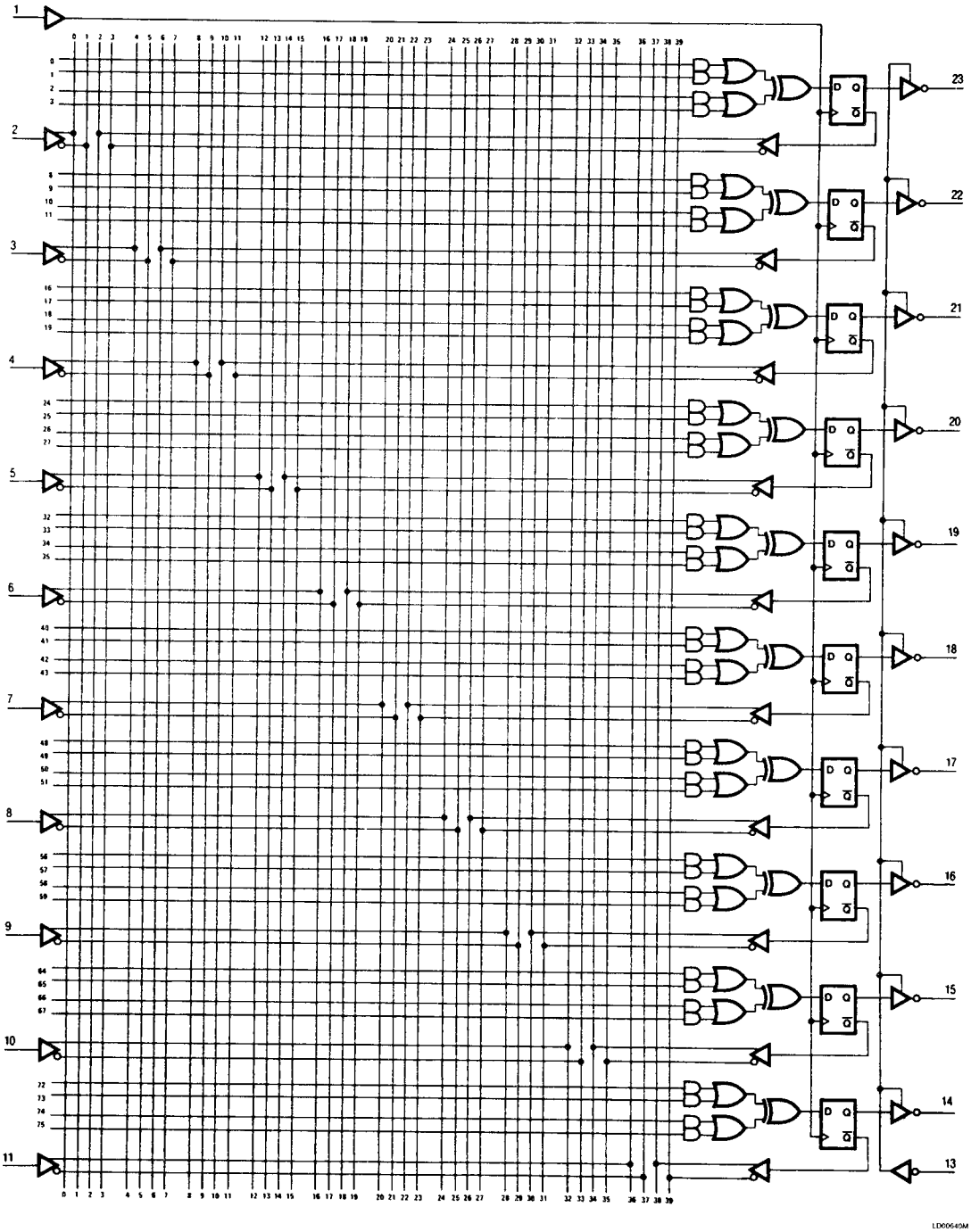
SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output 20L10A, 20X8A, and 20X4A		Commercial R_1 = 200Ω R_2 = 360Ω		23	30	ns
t_{CLK}	Clock to output or feedback				10	15	ns
t_{PZX}	Pin 13 to output enable except 20L10A				11	20	ns
t_{PXZ}	Pin 13 to output disable except 20L10A				10	20	ns
t_{PZX}	Input to output enable	20X8A, 20X4A, and 20L10A			19	30	ns
t_{PXZ}	Input to output disable	20X8A, 20X4A, and 20L10A			15	30	ns
f_{MAX}	Maximum frequency	20X10A, 20X8A, and 20X4A		22.2	32		MHz

1. The PAL24XA Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

20L10

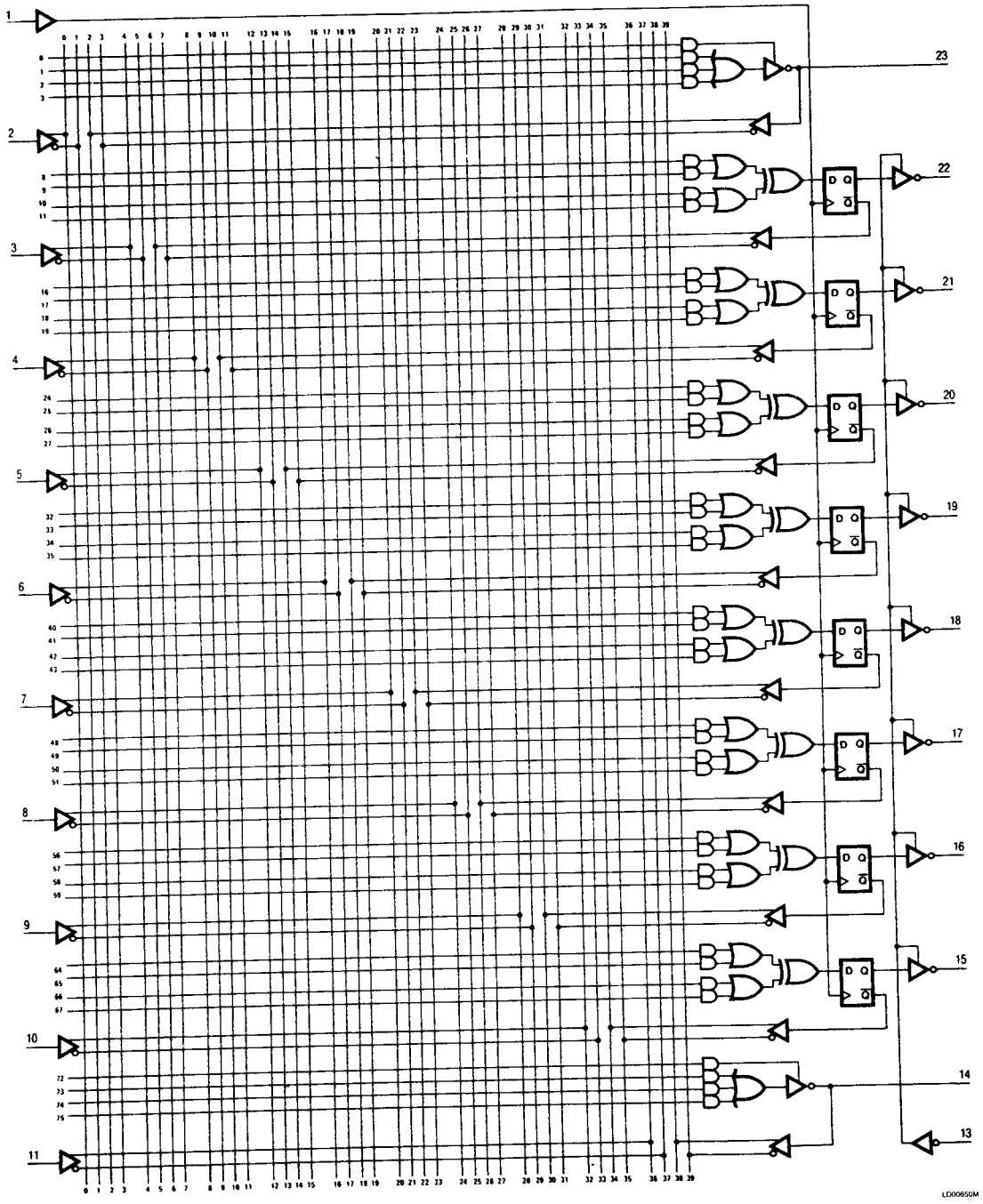


20X10



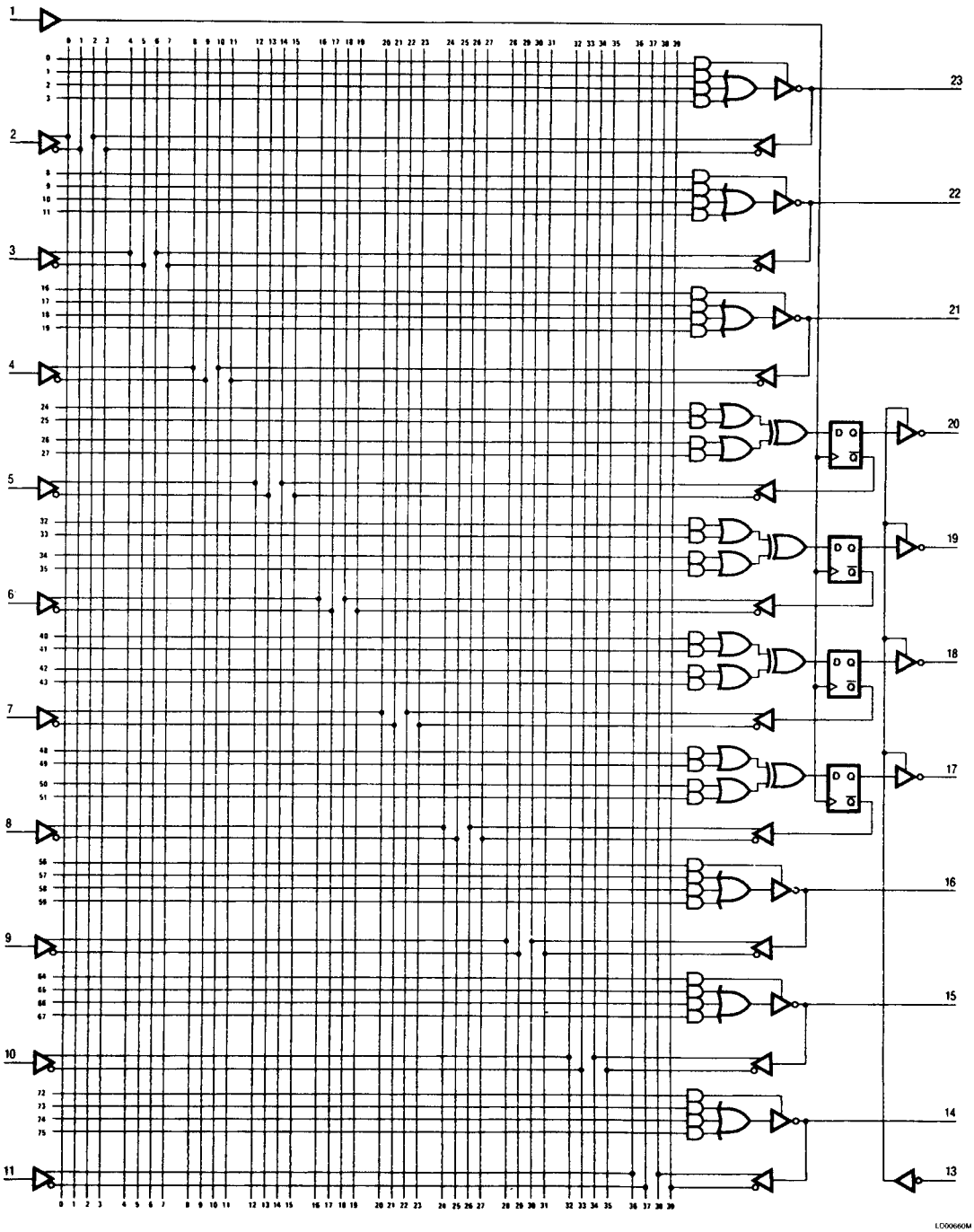
LD00640M

20X8



LD00850M

20X4



Large 24RS Series

	ARRAY INPUTS	OUTPUTS		STANDARD	
		COMBINATORIAL	REGISTERED	t_{PD}* (ns)	I_{CC} (mA)
PAL20S10	20	10	0	35/40	240
PAL20RS10	20	0	10	35	240
PAL20RS8	20	2	8	35/40	240
PAL20RS4	20	6	4	35/40	240

*35ns active low, 40ns active high

Description

The Large 24RS Series offers product term sharing, which allows up to sixteen product terms to be used at a single output.

Enable

The combinatorial outputs are enabled by a product term. The registered outputs are enabled by a common enable pin.

Programmable Polarity

Each flip-flop has individually programmable polarity. The unprogrammed state is active low.

Product Term Sharing

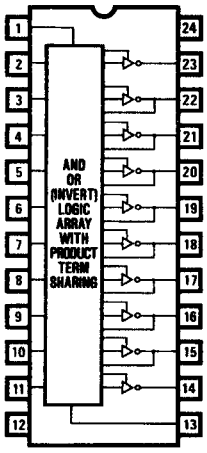
Product term sharing allows each pair of outputs to share its product terms with one output or the other (not both). Each pair has a total of sixteen product terms; thus, one output can use zero to sixteen terms while the other has sixteen to zero. Product terms can only be shared mutually exclusively. If both outputs need the same term, it must be created twice, once for each output.

Preload and Power-up Reset

The 24RS Series offers register preload for device testability. The registers can be preloaded from the outputs by using supervoltages (see waveforms at end of section) in order to simplify functional testing. The 24RS Series also offers Power-up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

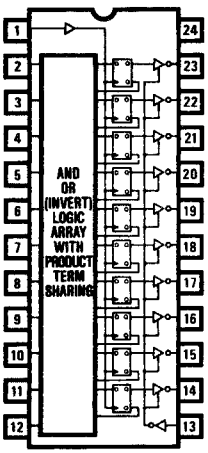
DIP Pinouts

20S10



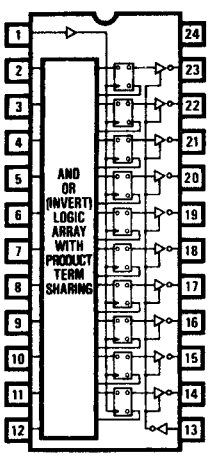
CD00680M

20RS10



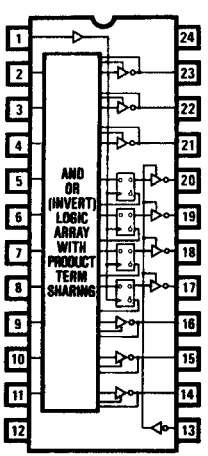
CD00690M

20RS8



CD00160M

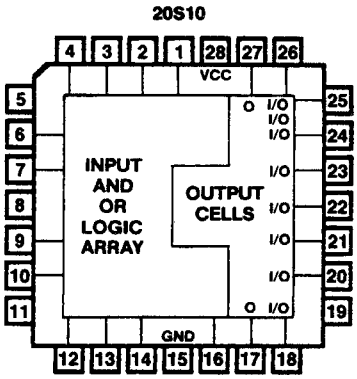
20RS4



CD00700M

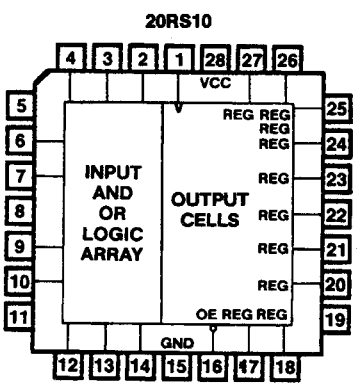
PLCC Pinouts

20S10



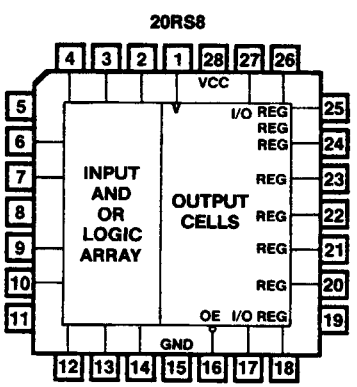
CD00830M

20RS10



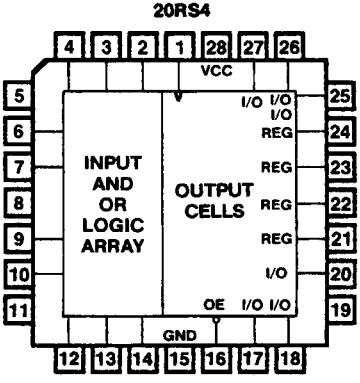
CD00230M

20RS8



CD00840M

20RS4



CD00850M

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	10		15	10		ns
		High	20	10		15	10		
t_{su}	Setup time from input or feedback to clock	20RS10, 20RS8, 20RS4	40	25		35	25		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics (Over Operating Conditions)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 12mA		0.3	0.5	V
			Com	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −2mA	2.4	2.8		V
			Com	I_{OH} = −3.2mA				
I_{OZL}[2]	Off-state output current	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}[2]				V_O = 2.4mA			100	
I_{OS}[3]	Output short-circuit current	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				175	240	mA

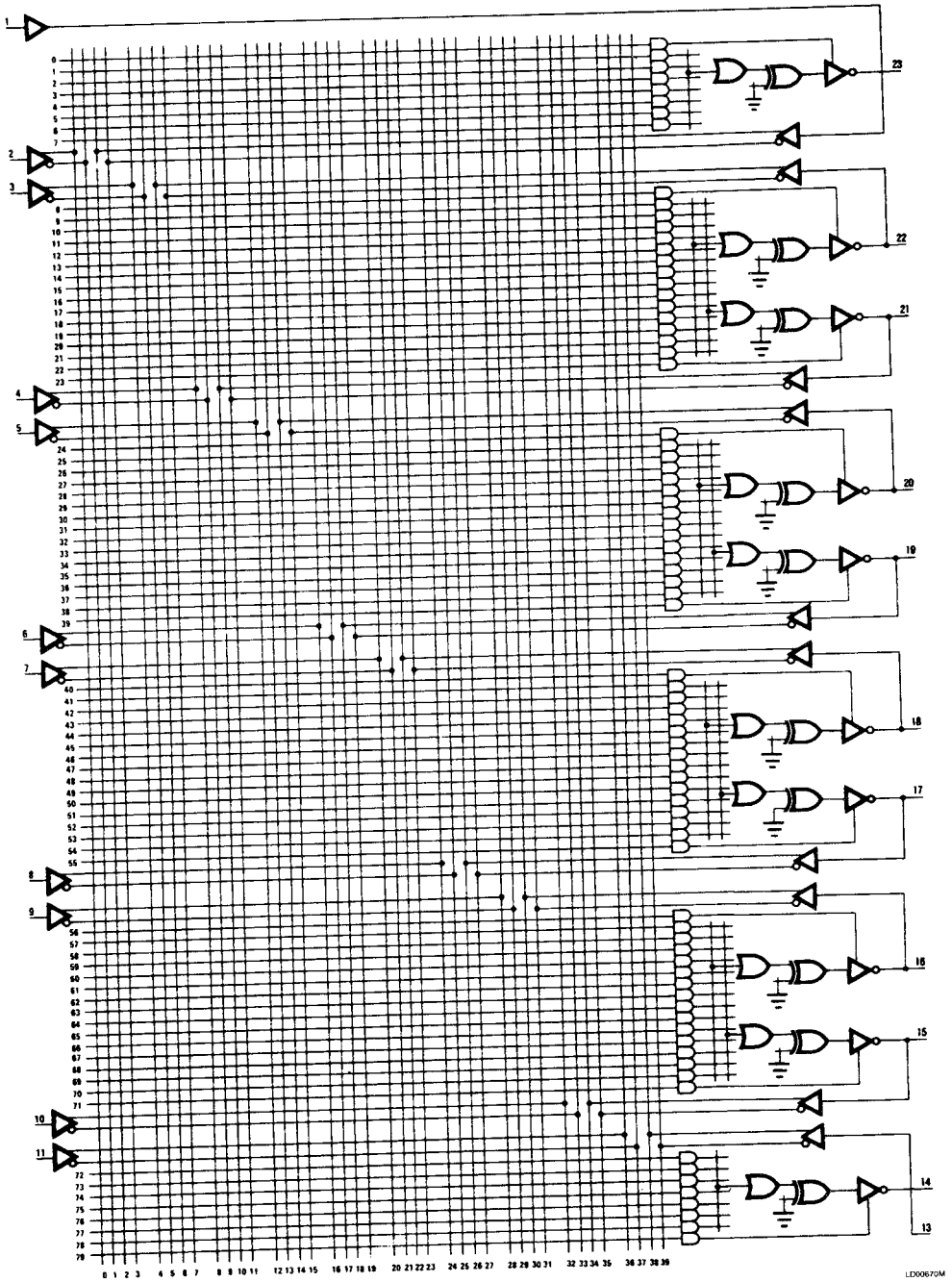
1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics (Over Operating Conditions)

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output 20S10, 20RS8, 20RS4	Polarity fuse intact	Commercial $R_1 = 200\Omega$ $R_2 = 390K\Omega$		25	40		25	35	ns
		Polarity fuse blown			30	45		30	40	
t_{CLK}	Clock to output or feedback				12	20		12	17	ns
t_{PZX}	Pin 13 to output enable except 20S10				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable except 20S10				11	25		11	20	ns
t_{PZX}	Input to output enable	20S10, 20RS8, 20RS4			25	35		25	35	ns
t_{PZX}	Input to output disable	20S10, 20RS8, 20RP4	Military $R_1 = 390\Omega$ $R_2 = 750\Omega$		13	30		13	25	ns
f_{MAX}	Maximum frequency	20RS10, 20RS8, 20RS4		18	28		20	28		MHz

2

20S10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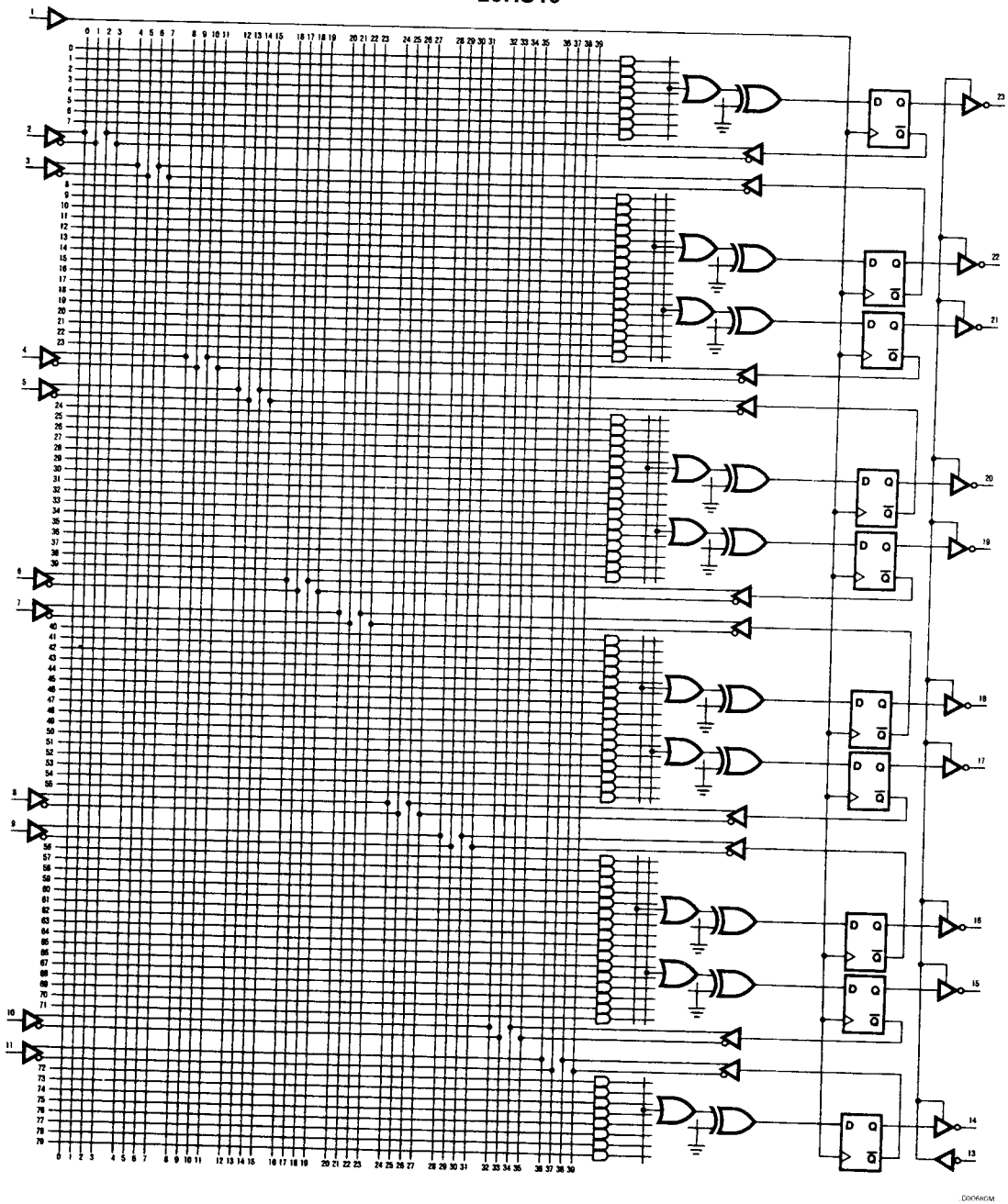
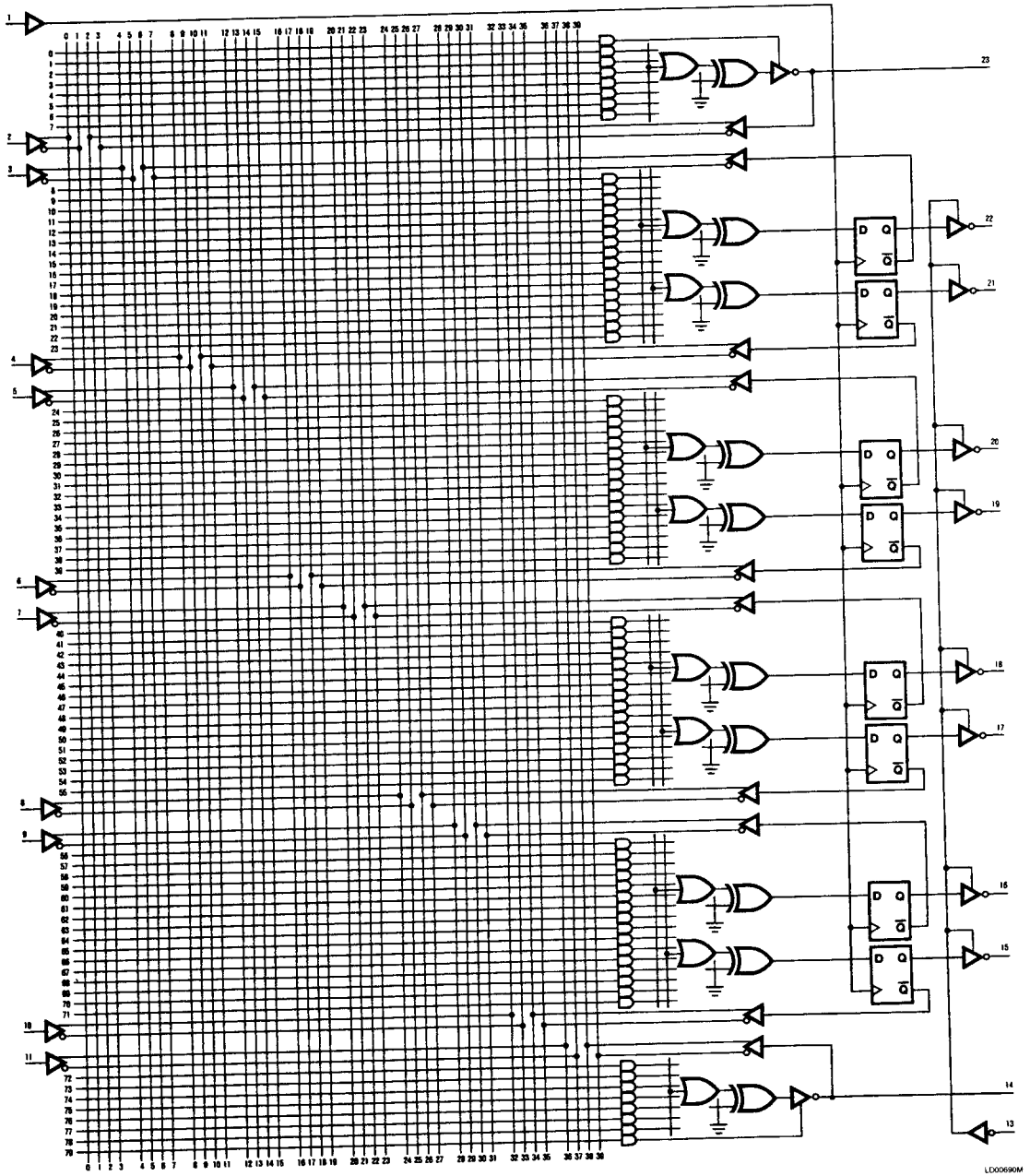
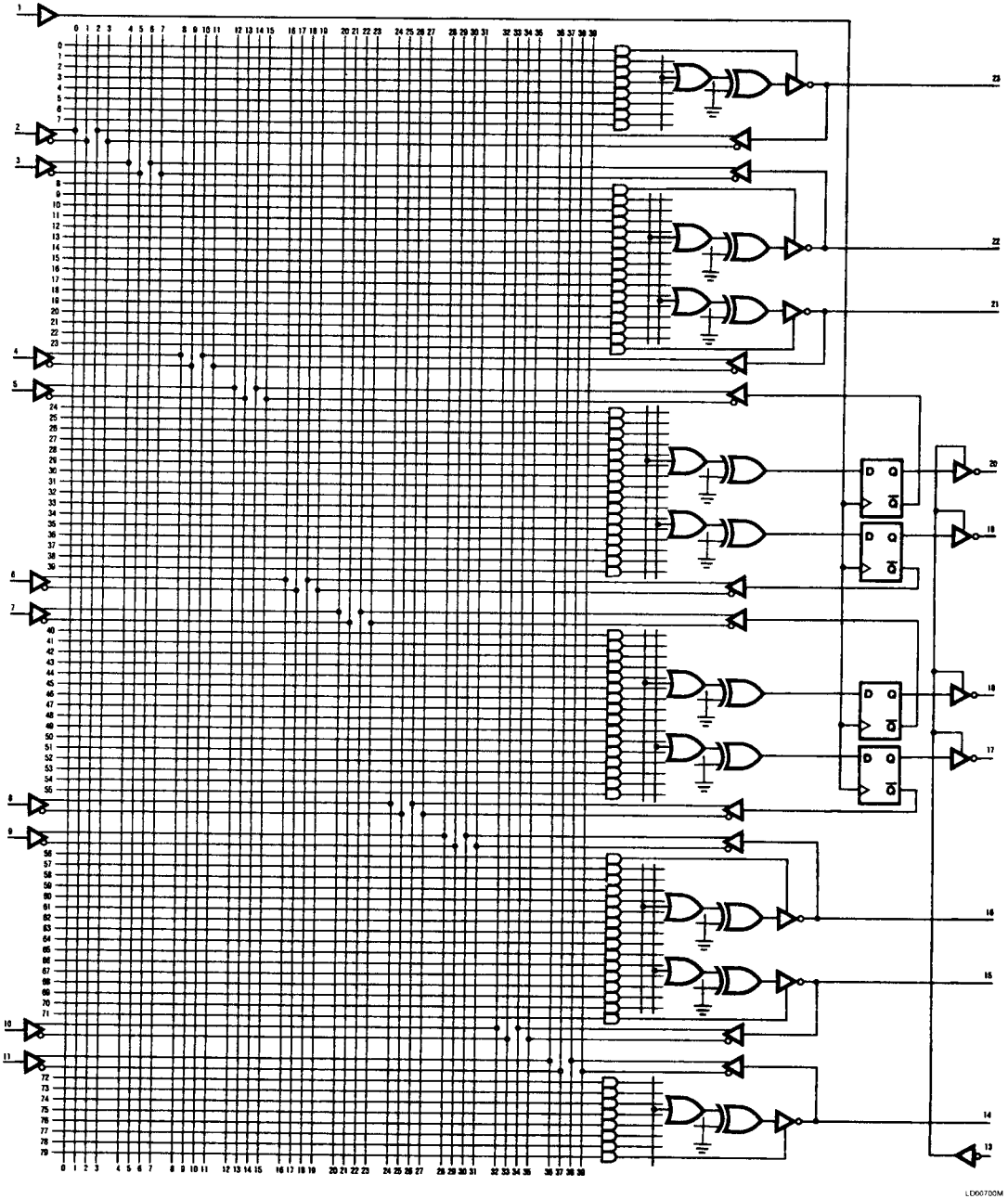
20RS10



20RS8



20RS4



LD00700M

Large 24RA (PAL20RA10)

Description

The PAL20RA10 is a 24-pin registered asynchronous PAL device. This versatile device features programmable clock, enable, set, and reset, all of which can operate asynchronously to other flip-flops in the same device. It also has individual flop-flop bypass, allowing this one device to provide any combination of registered and combinatorial outputs.

Programmable Clock

The clock input to each flip-flop comes from the programmable array, allowing the flip-flops to be clocked independently if desired.

Programmable Set and Reset

Each flip-flop has a product line for asynchronous set and one product for asynchronous reset. If the chosen product line is high, the flip-flop will set (become a logic HIGH), or reset (become a logic LOW). The sense of the output pin is inverted if the output is active low.

Programmable Polarity

Each flip-flop has individually programmable polarity. The unprogrammed state is active low.

Programmable Flip-flop Bypass

If both the set and reset product lines are high, the flip-flop is bypassed and the output becomes combinatorial. Thus each output can be configured to be registered or combinatorial.

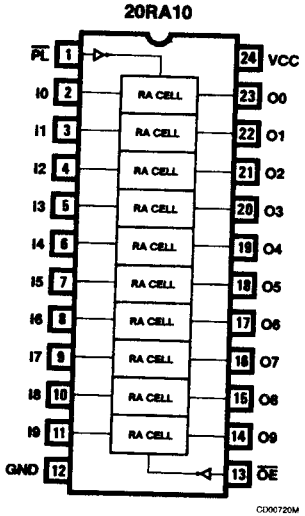
Programmable and Hard-Wired Three-State Outputs

The PAL20RA10 provides a product term dedicated to output control. There is also an output control pin (pin 13). The output is enabled if both the output control pin is low and the output control product term is high. If the output control pin is high all outputs will be disabled. If an output control product term is low, then that output will be disabled.

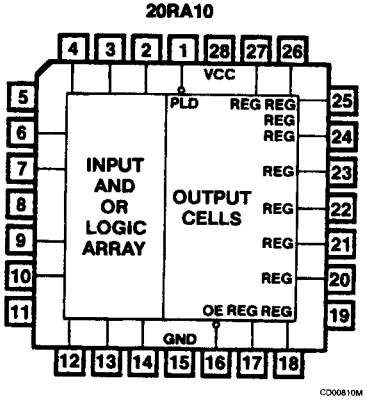
Register Preload and Power-up Reset

Each device also offers register preload for device testability. The registers can be preloaded from the outputs by using TTL level signals in order to simplify functional testing. This series also offers Power-up Reset, whereby the registers power up to a logic LOW, setting the active-low outputs to a logic HIGH.

DIP Pinout



PLCC Pinout



Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	13		20	13		ns
		High	25	13		20	13		
t_{wp}	Preload pulse width		45	15		35	15		ns
t_{su}	Setup time for input or feedback to clock		25	10		20	10		ns
t_{sup}	Preload setup time		30	5		25	5		ns
t_h	Hold time	Polarity fuse intact	10	−2		10	−2		ns
		Polarity fuse blown	0	−6		0	−6		
t_{hp}	Preload hold time		30	5		25	5		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics (Over Operating Conditions)

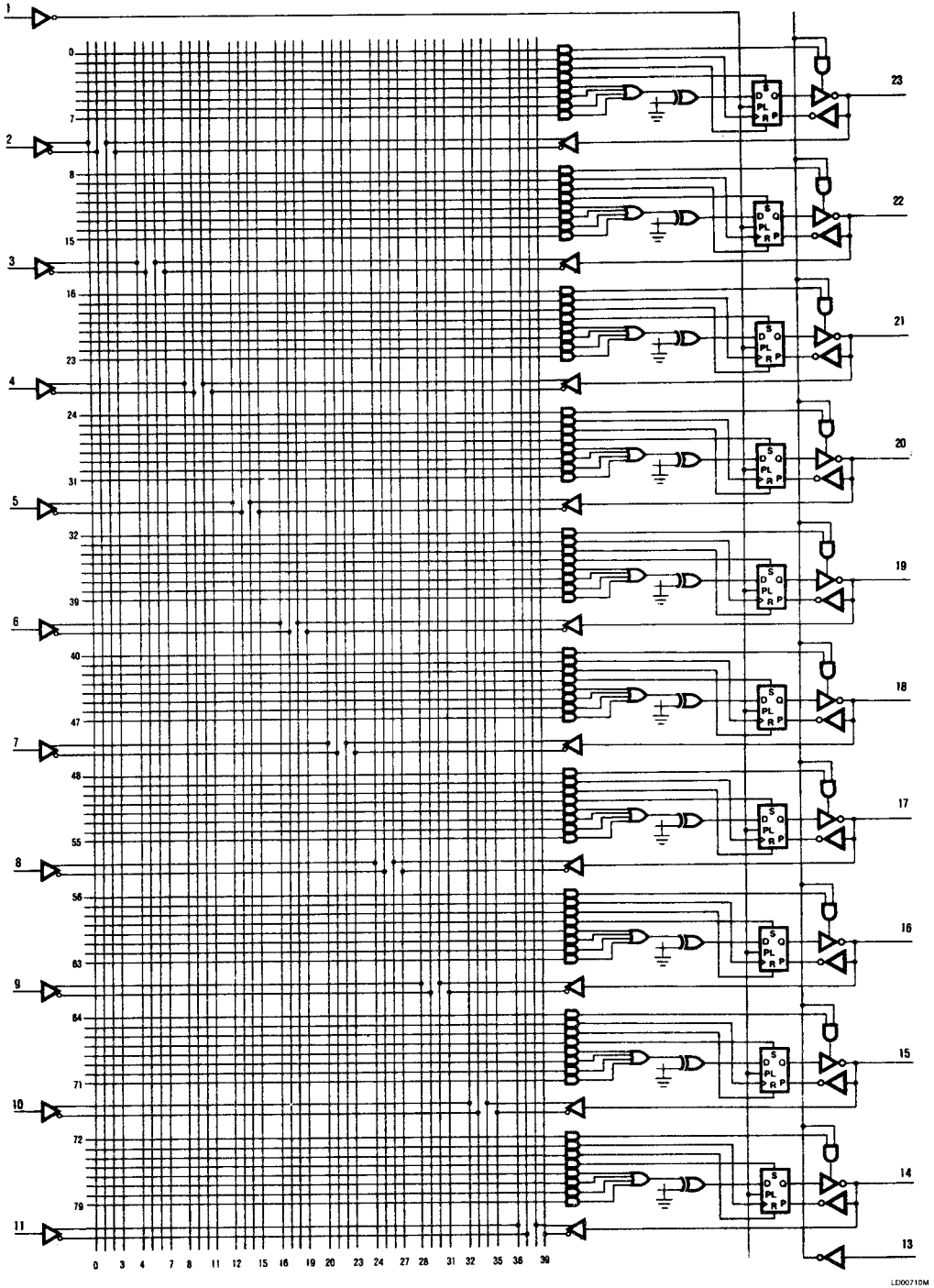
SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage					0.8	V
V_{IH}[1]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH}: Mil-2mA Com-3.2mA	2.4	2.8		V
I_{OZ}[2]	Off-state output current	V_{CC} = MAX	V_O = 2.4 V/V_O = 0.4V	−100		100	μA
I_{OS}[3]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			155	200	mA

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics (Over Operating Conditions)

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	Polarity fuse intact	$R_1 = 560\Omega$ $R_2 = 1.1K\Omega$		20	35		20	30	ns
		Polarity fuse blown			25	40		25	35	
t_{CLK}	Clock to output or feedback			10	17	35	10	17	30	ns
t_S	Input to asynchronous set				22	40		22	35	ns
t_R	Input to asynchronous reset				27	45		27	40	ns
t_{PZX}	Pin 13 to output enable				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable				10	25		10	20	ns
t_{PZX}	Input to output enable				18	35		18	30	ns
t_{PXZ}	Input to output disable				15	35		15	30	ns
f_{MAX}	Maximum frequency			16	35		20	35		MHz

20RA10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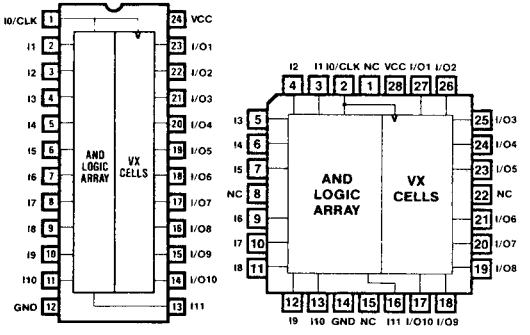
Features/Benefits

- Dual independent feedback paths allow buried state registers or input registers
- Programmable flip-flops allow J-K, S-R, T or D types for the most efficient use of product terms
- 10 input/output macrocells for flexibility
- Programmable registered or combinatorial outputs
- Programmable output polarity
- Global register asynchronous preset/synchronous reset or synchronous preset/asynchronous reset
- Automatic register preset on power up
- Preloadable output registers for testability
- Varied product term distribution
  –Up to 16 product terms per output
- High speed
  –25ns "A" version
  –30ns standard version
- Space-saving 24-pin 300-mil SKINNYDIP® package or 28-pin chip carrier
- Pin-compatible functional superset of 22V10

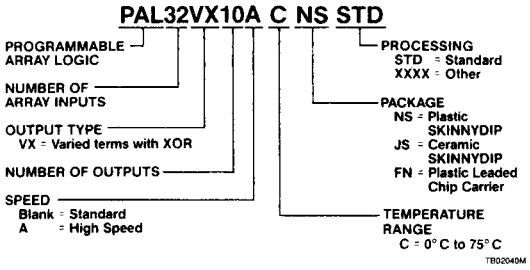
Pin Configurations



SKINNYDIP Package **Plastic Leaded Chip Carrier**

CD01660M

Ordering Information



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General Description

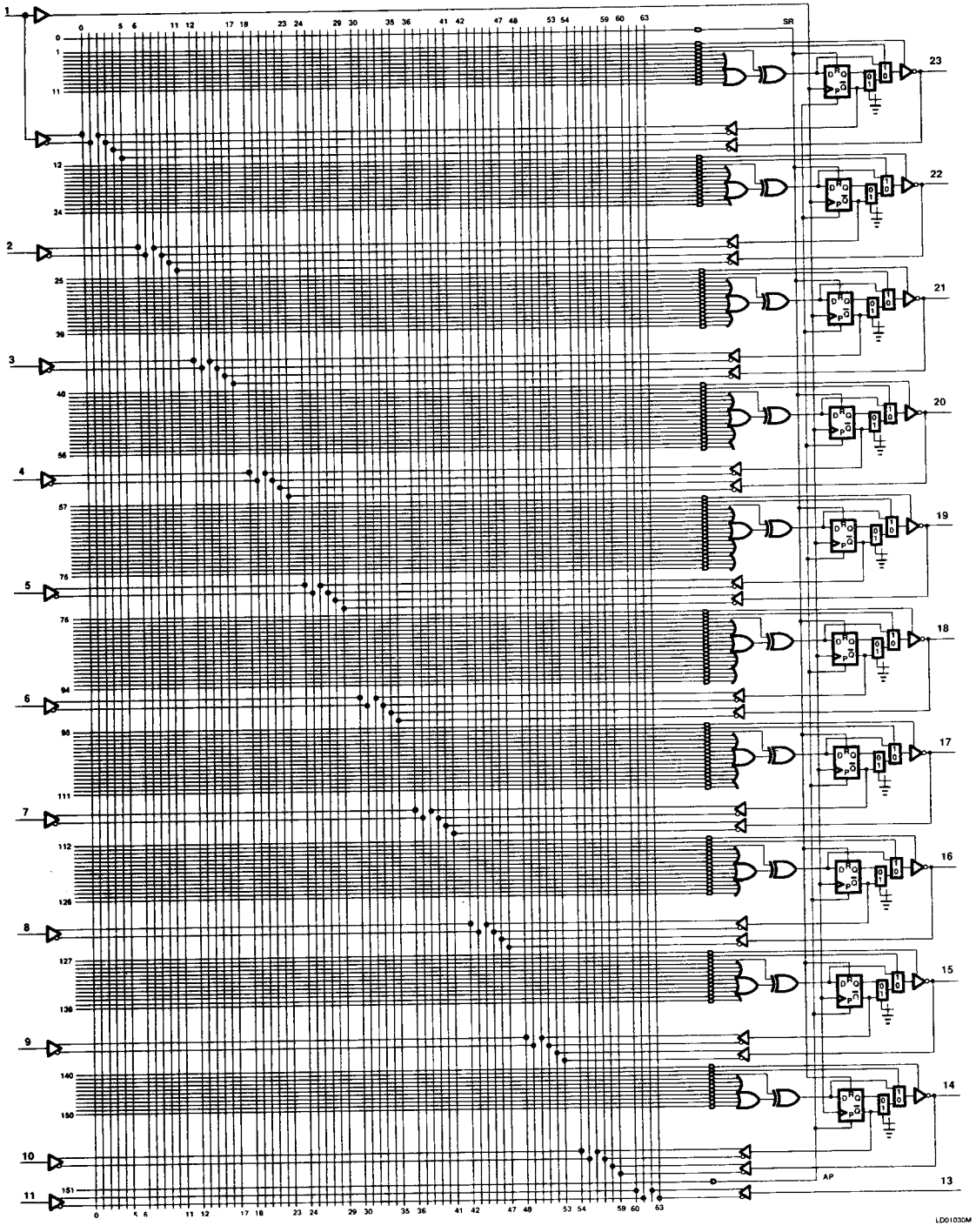
The PAL32VX10 is a high-density Programmable Array Logic (PAL®) device which implements a sum-of-products transfer function via a user-programmable AND logic array and a fixed OR logic array. Featured are ten highly flexible input/output macrocells which are user-configurable for combinatorial or registered operation. Each flip-flop can be programmed to be either a J-K, S-R, T, or D-type for optimal design of state machines and other synchronous logic. In addition, a unique dual feedback architecture allows I/O capability for each macrocell in both combinatorial and registered configurations. This can be achieved even when register feedback is present, and allows implementation of buried flip-flops while preserving the external macrocell input. Supplied in space-saving 300-mil-wide dual in-line packages or 28-pin chip carriers, the PAL32VX10 offers a powerful, space saving alternative to SSI/MSI logic devices, while providing the advantage of instant prototyping. Security fuses defeat readout after programming and make proprietary designs difficult to copy.

The PAL32VX10 is fabricated using Monolithic Memories' advanced oxide-isolated bipolar process for high speed and low power. TiW fuse links provide high reliability and programming yields. Special on-chip test circuits allow full AC, DC, and functional testing before programming. Preloadable output registers facilitate functional testing.

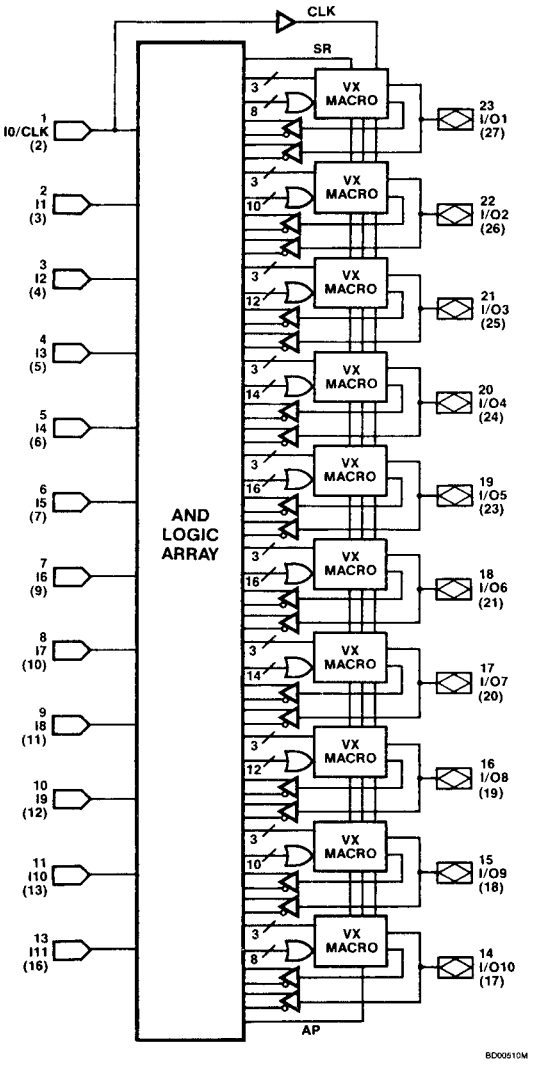
The PAL32VX10 can be programmed on standard PAL device programmers, fitted with appropriate programming modules and configuration software. Design development is supported by Monolithic Memories' PALASM® 2 software as well as by other programmable logic CAD tools available from third party vendors. Approved development tools are listed on page 10.

2

Logic Diagram



Block Diagram



Note: PLCC pin numbers are indicated in parentheses.
PLCC pins 1, 8, 15, and 22 are not connected.

Description of Architecture

The PAL32VX10 has twelve dedicated input lines and ten programmable I/O macrocells. Pin 1 serves either as an array input or as a clock for all flip-flops. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. The fuse matrix implements a programmable AND logic array, which drives a fixed OR logic array.

The high level of flexibility built into each macrocell, shown in Figure 1, allows the PAL32VX10 to implement over thirty different architecture options. Each macrocell can be individually programmed to implement a variety of combinatorial or registered logic functions.

Dual Output Feedback

Dual feedback paths associated with each macrocell provide independent feedback paths directly into the array from both the flip-flop output and the output pin. Unlike other devices which have a single feedback path, the PAL32VX10 allows each output to have full I/O capability when configured as either a combinatorial output or a registered output, even if register feedback to the array is used. Thus registers can be loaded from their outputs.

If a macrocell is configured as a dedicated input, by disabling the three-state output buffer, the dual feedback architecture allows use of the associated register as an input register or as a "buried" state register, avoiding waste of the flip-flop, as shown in Figure 2.

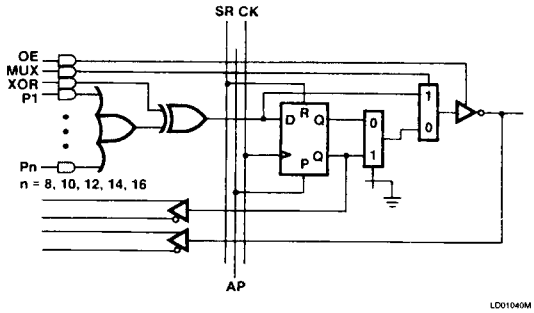


Figure 1. PAL32VX10 Macrocell

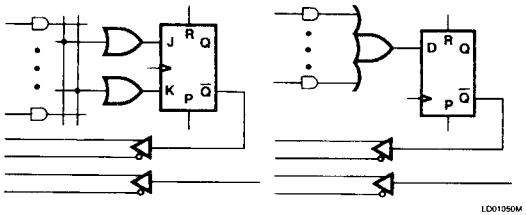


Figure 2. Buried Flip-Flops with Dedicated Inputs

Programmable Flip-Flops

Each output macrocell contains a unique programmable flip-flop consisting of a basic D-type flip-flop driven by an XOR gate. This allows the user to choose the optimal flip-flop for the design, since either J-K, S-R, or T-type flip-flops can be synthesized from such a structure without wasting product terms.

As indicated in the macrocell logic diagram, one input of the XOR gate is connected to a single product term, while the second input is connected to the output of the OR logic array. The XOR gate output feeds the input of the D flip-flop. The way in which the XOR gate is used to synthesize the different flip-flop types is described in detail below.

D Flip-Flop. The D flip-flop option is implemented directly. In this configuration, the XOR gate on the input of the flip-flop can be used to program the logic polarity of the transfer function.

J-K Flip-Flop. The J-K flip-flop option can be easily synthesized with a more sophisticated manipulation of the XOR gate inputs and the D flip-flop output.

The transfer function of a J-K flip-flop can be mapped in the Karnaugh Map of Figure 3, where Q + represents the next state of the flip-flop:

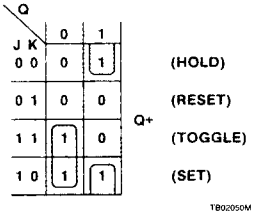


Figure 3. J-K Flip-Flop Transfer Function

Dropping the (+) for simplicity, the equivalent Boolean expression for Q + is:

$$Q: = \overline{K}*Q + J*\overline{Q}$$

In general, J and K can be sum-of-product expressions which are provided in the PAL architecture only in active-high form. Thus, a direct implementation of $\overline{K}$ expressions must invoke a DeMorgan transformation, which can use excessive product terms. This can be avoided by rewriting the equation for Q without inversions on the J or K inputs.

The XOR gate can be used to construct a logically equivalent expression without any inversions on the J or K inputs. The rewritten Boolean expression is:

$$Q: = Q: + :(J*\overline{Q} + K*Q)$$

To check that these expressions are logically equivalent, change the XOR to its equivalent sum of products form (remember A: +: B = A*$\overline{B}$ + $\overline{A}$*B) and reduce (using DeMorgan's theorem):

$Q: = Q*(J*\overline{Q} + K*Q)$ $\quad +\overline{Q}*(J*\overline{Q} + K*Q)$
$Q: = Q*((\overline{J} + Q)*(\overline{K} + \overline{Q}))$ $\quad +\overline{Q}*J*\overline{Q} + \overline{Q}*K*Q$
$Q: = Q*(J*\overline{K} + \overline{J}*\overline{Q} + Q*\overline{K} + Q*\overline{Q}) + J*\overline{Q}$
$Q: = \overline{J}*\overline{K}*Q + \overline{K}*Q + J*\overline{Q}$

which simplifies to $Q: = \overline{K}*Q + J*\overline{Q}$.

Since J and K are, in general, sums of products, J and K in either expression can be substituted with (J1 + J2 + ... + Jm) and (K1 + K2 + ... + Kn – m), where n is the total number of product terms associated with a given output macrocell. Thus, the total n-product term resource is shared between the J and K control inputs (Figure 4). Note that all J terms will contain $\overline{Q}$ and all K terms will contain Q.

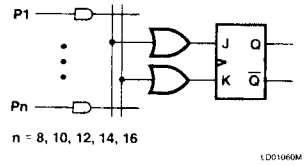


Figure 4. J-K Flip-Flop Logic Equivalent; J and K Can Also be Active-Low

The above discussions have assumed that it was most convenient to "group ones" in the Karnaugh Map. Sometimes it takes fewer product terms to "group zeros", i.e., implement the inversion of the desired function. The equations shown in Table 1 are equivalent and can be interchanged to optimize product term utilization. This can be readily proved through logic reductions similar to that above.

J and K active high	$Q: = Q: + :(J*\overline{Q} + J*Q)$
J active high, K active low	$Q: = J*\overline{Q} + \overline{K}*Q$
J active low, K active high	$\overline{Q}: = \overline{J}*\overline{Q} + K*Q$
J and K active low	$Q: = \overline{Q}: + :(\overline{J}*\overline{Q} + \overline{K}*Q)$

Note: J = sum of products J1 + J2 + ... + Jm
K = sum of products K1 + K2 + ... + Kn – m
n = total number of available product terms for a given macrocell (8 to 16)

Table 1. J-K Flip-Flop Transfer Functions

S-R Flip-Flop. The S-R flip-flop has a truth table identical to that of the J-K flip-flop, with the exception that the J = K = 1 (toggle) condition is not allowed. The S-R flip-flop implementation is identical to that of the J-K flip-flop, with J-K replaced by S-R, and the S = R = 1 condition avoided.

T Flip-Flop. A T (toggle) flip-flop either holds its state or toggles, depending on the logic state of the T input. The T flip-flop is a subset of the J-K flip-flop and can be considered equivalent to a J-K type with J = K. The general transfer function and its active-low T equivalent are both given in Table 2.

$Q: = Q: + :T$
$Q: = \overline{Q}: + :\overline{T}$

Note: T = sum of products T1 + T2 + T3 + ... + Tn

Table 2. T Flip-Flop Transfer Functions

Summary

The PAL32VX10 can synthesize J-K, S-R, T, and D flip-flops, whichever is most convenient for the application, without sacrificing product terms. Additionally, the synthesized equations can use the active-high or active-low forms of the inputs, allowing the designer to minimize product term requirements.

Flip-Flop Bypass

Any output in the PAL32VX10 can be configured to be combinatorial by bypassing the output flip-flop. This is done by setting the output multiplexer to the appropriate state. The multiplexer is controlled by a product term which can be set unconditionally for a permanent combinatorial (all fuses opened, product term high) or registered (all fuses intact, product term low) output configuration, or can be programmed to bypass the output flip-flop "on the fly," allowing signals to be routed directly to output pins under user-specified conditions.

Varied Product Term Distribution

An increased number of product terms has been provided in the PAL32VX10 over previous generation PAL devices. These terms are distributed among the ten macrocells in a varied manner, ranging from eight to sixteen terms per output. The five output pairs have 8, 10, 12, 14, or 16 product terms available for the OR gate within each macrocell. In addition, each macrocell has one XOR product term and two architecture control product terms.

Programmable I/O

Each macrocell has a three-state output buffer with programmable three-state control. Control is implemented by a single product term, allowing specification of enable/disable functions controlled by any device input or output. Each macrocell can be configured as a dedicated input by disabling the buffer drive capability. When this is done, the associated register can still be used as an input register or buried state register, due to the independent register feedback path.

Programmable Preset and Reset

The ten macrocell flip-flops share common programmable preset and reset control for easy system initialization. The Q outputs of the register will go to the logic low state following a low-to-high transition on pin 1 (I0/CLK) when the synchronous reset (SR) product term is asserted. The register will be forced to the logic high state independent of the clock when the asynchronous preset (AP) product term is asserted.

Programmable Polarity

The polarity of each macrocell output can be set active high or active low.

Combinatorial Outputs. The XOR gate provides polarity control for combinatorial outputs, with the single product term to the XOR gate controlling the invert/not invert function. With all fuses intact, there is no inversion through the XOR gate, creating an active low output. Opening all fuses forces the product term high, inverting data and creating an active high output.

Registered Outputs. Output polarity for registered outputs can be determined in two ways. For D-type registered outputs, polarity can be set by the XOR gate, as is the case with combinatorial outputs. Using this method to set polarity, preset and reset will not be affected.

Polarity, as observed from the output pin, can also be determined by the flip-flop output multiplexer. Note that this does not affect the polarity of the register feedback signal, but does affect preset and reset. By changing the flip-flop output multiplexer, the preset and reset functions are exchanged, relative to the controlling product terms.

With the multiplexer fuse intact, the Q output is routed to the output pin, configuring an active low output. With the multiplexer fuse opened, $\overline{Q}$ is routed to the output pin, and synchronous reset becomes synchronous preset. Similarly, asynchronous reset becomes asynchronous preset.

Polarity options for J-K, S-R, and T flip-flops have been discussed in the section on programmable flip-flops.

Power-Up Preset

All flip-flops power up to a logic high for predictable system initialization. Outputs of the PAL32VX10 will be high or low depending on the state of the register output multiplexers.

Register Preload

The register on the PAL32VX10 can be preloaded to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading in illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL32VX10 design can be secured by programming the security fuses. Once programmed, these fuses defeat readback of the internal fuse pattern by a device programmer, making proprietary designs very difficult to copy.

Quality and Testability

The PAL32VX10 offers a very high level of built-in quality. Special on-chip test circuitry provides a means of verifying performance of all AC and DC parameters prior to programming. In addition, these built-in test paths verify complete functionality of each device to provide the highest post-programming functional yields in the industry.

Programmable Flip-Flops

Each output macrocell contains a unique programmable flip-flop consisting of a basic D-type flip-flop driven by an XOR gate. This allows the user to choose the optimal flip-flop for the design, since either J-K, S-R, or T-type flip-flops can be synthesized from such a structure without wasting product terms.

As indicated in the macrocell logic diagram, one input of the XOR gate is connected to a single product term, while the second input is connected to the output of the OR logic array. The XOR gate output feeds the input of the D flip-flop. The way in which the XOR gate is used to synthesize the different flip-flop types is described in detail below.

D Flip-Flop. The D flip-flop option is implemented directly. In this configuration, the XOR gate on the input of the flip-flop can be used to program the logic polarity of the transfer function.

J-K Flip-Flop. The J-K flip-flop option can be easily synthesized with a more sophisticated manipulation of the XOR gate inputs and the D flip-flop output.

The transfer function of a J-K flip-flop can be mapped in the Karnaugh Map of Figure 3, where Q + represents the next state of the flip-flop:

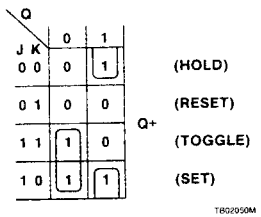


Figure 3. J-K Flip-Flop Transfer Function

Dropping the (+) for simplicity, the equivalent Boolean expression for Q + is:

$$Q: = \overline{K}*Q + J*\overline{Q}$$

In general, J and K can be sum-of-product expressions which are provided in the PAL architecture only in active-high form. Thus, a direct implementation of $\overline{K}$ expressions must invoke a DeMorgan transformation, which can use excessive product terms. This can be avoided by rewriting the equation for Q without inversions on the J or K inputs.

The XOR gate can be used to construct a logically equivalent expression without any inversions on the J or K inputs. The rewritten Boolean expression is:

$$Q: = Q: + :(J*\overline{Q} + K*Q)$$

To check that these expressions are logically equivalent, change the XOR to its equivalent sum of products form (remember A: +: B = A*$\overline{B}$ + $\overline{A}$*B) and reduce (using DeMorgan's theorem):

$Q: = Q*(J*\overline{Q} + K*Q) + \overline{Q}*(J*\overline{Q} + K*Q)$
$Q: = Q*((\overline{J} + Q)*(\overline{K} + \overline{Q})) + \overline{Q}*J*\overline{Q} + \overline{Q}*K*Q$
$Q: = Q*(J*\overline{K} + \overline{J}*\overline{Q} + Q*\overline{K} + Q*\overline{Q}) + J*\overline{Q}$
$Q: = \overline{J}*\overline{K}*Q + \overline{K}*Q + J*\overline{Q}$

which simplifies to $Q: = \overline{K}*Q + J*\overline{Q}$.

Since J and K are, in general, sums of products, J and K in either expression can be substituted with (J1 + J2 + ... + Jm) and (K1 + K2 + ... + Kn – m), where n is the total number of product terms associated with a given output macrocell. Thus, the total n-product term resource is shared between the J and K control inputs (Figure 4). Note that all J terms will contain $\overline{Q}$ and all K terms will contain Q.

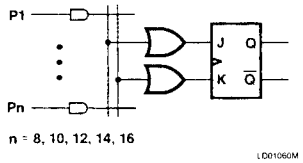


Figure 4. J-K Flip-Flop Logic Equivalent; J and K Can Also be Active-Low

The above discussions have assumed that it was most convenient to "group ones" in the Karnaugh Map. Sometimes it takes fewer product terms to "group zeros", i.e., implement the inversion of the desired function. The equations shown in Table 1 are equivalent and can be interchanged to optimize product term utilization. This can be readily proved through logic reductions similar to that above.

J and K active high	$Q: = Q: + :(J*\overline{Q} + J*Q)$
J active high, K active low	$Q: = J*\overline{Q} + \overline{K}*Q$
J active low, K active high	$\overline{Q}: = \overline{J}*\overline{Q} + K*Q$
J and K active low	$Q: = \overline{Q}: + :(\overline{J}*\overline{Q} + \overline{K}*Q)$

Note: J = sum of products J1 + J2 + ... + Jm
K = sum of products K1 + K2 + ... + Kn – m
n = total number of available product terms for a given macrocell (8 to 16)

Table 1. J-K Flip-Flop Transfer Functions

S-R Flip-Flop. The S-R flip-flop has a truth table identical to that of the J-K flip-flop, with the exception that the J = K = 1 (toggle) condition is not allowed. The S-R flip-flop implementation is identical to that of the J-K flip-flop, with J-K replaced by S-R, and the S = R = 1 condition avoided.

T Flip-Flop. A T (toggle) flip-flop either holds its state or toggles, depending on the logic state of the T input. The T flip-flop is a subset of the J-K flip-flop and can be considered equivalent to a J-K type with J = K. The general transfer function and its active-low T equivalent are both given in Table 2.

$Q: = Q: + :T$
$Q: = \overline{Q}: + :\overline{T}$

Note: T = sum of products T1 + T2 + T3 + ... + Tn

Table 2. T Flip-Flop Transfer Functions

Summary

The PAL32VX10 can synthesize J-K, S-R, T, and D flip-flops, whichever is most convenient for the application, without sacrificing product terms. Additionally, the synthesized equations can use the active-high or active-low forms of the inputs, allowing the designer to minimize product term requirements.

Flip-Flop Bypass

Any output in the PAL32VX10 can be configured to be combinatorial by bypassing the output flip-flop. This is done by setting the output multiplexer to the appropriate state. The multiplexer is controlled by a product term which can be set unconditionally for a permanent combinatorial (all fuses opened, product term high) or registered (all fuses intact, product term low) output configuration, or can be programmed to bypass the output flip-flop "on the fly," allowing signals to be routed directly to output pins under user-specified conditions.

Varied Product Term Distribution

An increased number of product terms has been provided in the PAL32VX10 over previous generation PAL devices. These terms are distributed among the ten macrocells in a varied manner, ranging from eight to sixteen terms per output. The five output pairs have 8, 10, 12, 14, or 16 product terms available for the OR gate within each macrocell. In addition, each macrocell has one XOR product term and two architecture control product terms.

Programmable I/O

Each macrocell has a three-state output buffer with programmable three-state control. Control is implemented by a single product term, allowing specification of enable/disable functions controlled by any device input or output. Each macrocell can be configured as a dedicated input by disabling the buffer drive capability. When this is done, the associated register can still be used as an input register or buried state register, due to the independent register feedback path.

Programmable Preset and Reset

The ten macrocell flip-flops share common programmable preset and reset control for easy system initialization. The Q outputs of the register will go to the logic low state following a low-to-high transition on pin 1 (I0/CLK) when the synchronous reset (SR) product term is asserted. The register will be forced to the logic high state independent of the clock when the asynchronous preset (AP) product term is asserted.

Programmable Polarity

The polarity of each macrocell output can be set active high or active low.

Combinatorial Outputs. The XOR gate provides polarity control for combinatorial outputs, with the single product term to the XOR gate controlling the invert/not invert function. With all fuses intact, there is no inversion through the XOR gate, creating an active low output. Opening all fuses forces the product term high, inverting data and creating an active high output.

Registered Outputs. Output polarity for registered outputs can be determined in two ways. For D-type registered outputs, polarity can be set by the XOR gate, as is the case with combinatorial outputs. Using this method to set polarity, preset and reset will not be affected.

Polarity, as observed from the output pin, can also be determined by the flip-flop output multiplexer. Note that this does not affect the polarity of the register feedback signal, but does affect preset and reset. By changing the flip-flop output multiplexer, the preset and reset functions are exchanged, relative to the controlling product terms.

With the multiplexer fuse intact, the Q output is routed to the output pin, configuring an active low output. With the multiplexer fuse opened, $\overline{Q}$ is routed to the output pin, and synchronous reset becomes synchronous preset. Similarly, asynchronous reset becomes asynchronous preset.

Polarity options for J-K, S-R, and T flip-flops have been discussed in the section on programmable flip-flops.

Power-Up Preset

All flip-flops power up to a logic high for predictable system initialization. Outputs of the PAL32VX10 will be high or low depending on the state of the register output multiplexers.

Register Preload

The register on the PAL32VX10 can be preloaded to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading in illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL32VX10 design can be secured by programming the security fuses. Once programmed, these fuses defeat readback of the internal fuse pattern by a device programmer, making proprietary designs very difficult to copy.

Quality and Testability

The PAL32VX10 offers a very high level of built-in quality. Special on-chip test circuitry provides a means of verifying performance of all AC and DC parameters prior to programming. In addition, these built-in test paths verify complete functionality of each device to provide the highest post-programming functional yields in the industry.

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5V to 7V	−0.5V to 12V
Input voltage	−1.5V to 5.5V	−1.0V to 22V
Off-state output voltage	5.5V	12V
Storage temperature		−65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1]						UNIT
			STD			A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
t_w	Width of clock	Low	20	10		18	10		ns
		High	20	10		18	10		
t_{su}	Setup time from input or feedback to clock	Product terms P_1-P_n, SR	30	20		25	20		ns
		Product term XOR	35	25		30	25		
t_h	Hold time		0	−10		0	−10		ns
t_{aw}	Asynchronous preset width		−30	20		25	20		ns
t_{ar}	Asynchronous preset recovery time		−30	20		25	20		ns
t_{sr}	Asynchronous reset recovery time		−30	20		25	20		ns
T_A	Operating case temperature		0	25	75	0	25	75	°C

Electrical Characteristics Over Operating Conditions

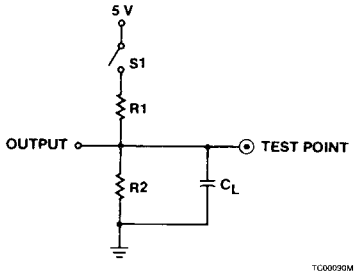
SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			200	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16mA		0.35	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3.2mA	2.4	3.4		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX			140	180	mA
C_{IN}	Input capacitance	V_{IN} = 2.0V at f = 1MHz			6		pF
C_{OUT}	Output capacitance	V_{OUT} = 2.0V at f = 1MHz			11		

1. The PAL32VX10/A is designed to operate over the full military operating conditions. For availability and specifications contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

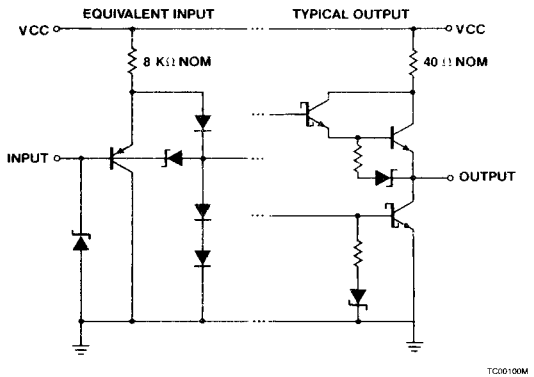
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION	STD			A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input or feedback to output	Product terms P_1-P_n	R_1 = 200Ω, R_2 = 390Ω		15	30		15	25	ns
		Product term XOR			25	35		20	30	
t_{CLK}	Clock to output or feedback				10	15		10	15	ns
t_{PZX}	Input to output enable				20	30		20	25	ns
t_{PXZ}	Input to output disable				20	30		20	25	ns
t_{AP}	Asynchronous preset to output				20	30		20	25	ns
t_{CR}	Input or feedback to registered output from combinatorial configuration				75	90		75	90	ns
t_{RC}	Input or feedback to combinatorial output from registered configuration				75	90		75	90	ns
f_{MAX}	Maximum frequency	Feedback ($1/t_{P1}$)	Product terms P_1-P_0	22.5	35		25	35		MHz
			Product term XOR	20	30		22.2	30		
		No feedback ($1/t_{P2}$)		25	40		27.7	40		

Switching Test Load

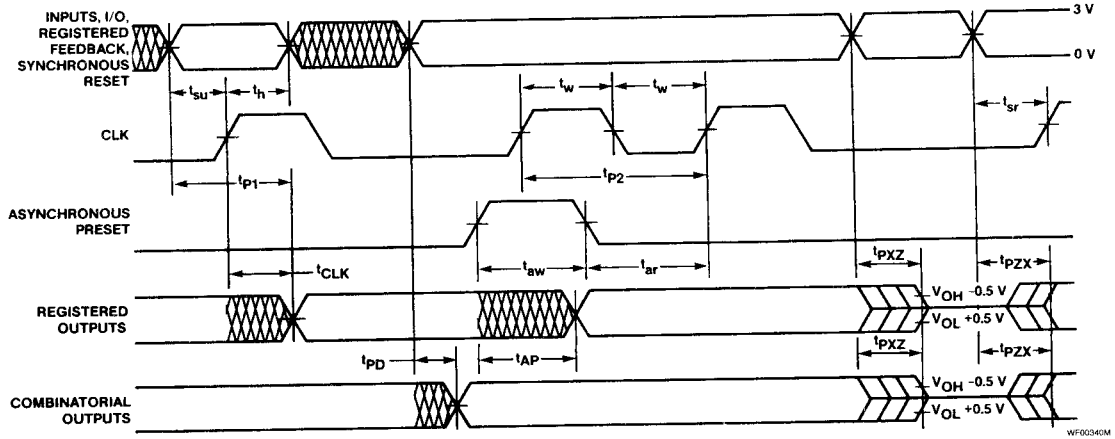


Schematic of Inputs and Outputs



Notes:
1. t_{PD} is tested with switch S_1 closed. C_L = 50pF and measured at 1.5V output level.
2. t_{PZX} is measured at the 1.5V output level with C_L = 50pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5V output level.

Switching Waveforms

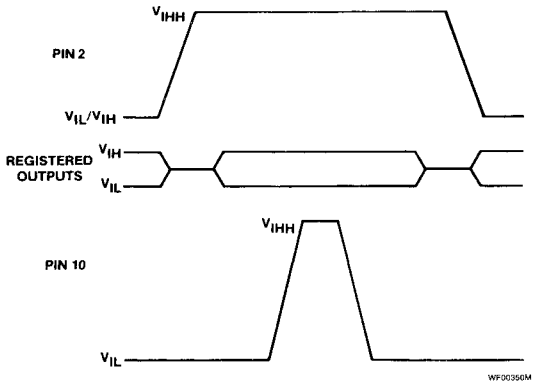


Output Register Preload

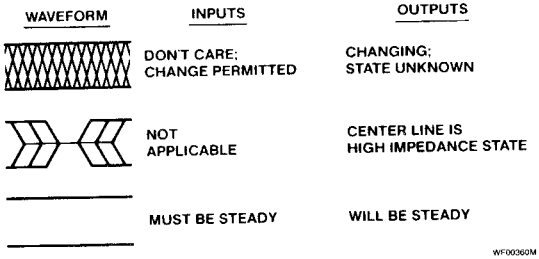
The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is:

1. Raise V_{CC} to 4.5V.
2. Disable output registers by setting pin 2 to V_{IHH}(12V).
3. Apply V_{IL}/V_{IH} to all registered output pins. Leave combinatorial outputs floating.
4. Pulse pin 10 to V_{IHH}, then back to 0V.
5. Remove V_{IL}/V_{IH} from all output registers.
6. Remove high voltage from pin 2.
7. Enable registered outputs per programmed pattern.
8. Verify for V_{OL}/V_{OH} at all registered output pins.

Note: V_{IHH} = 11.0 (MIN), 11.5 (TYP) and 12.0 (MAX).



Key to Timing Diagrams



f_{MAX} Parameters

The parameter fMAX is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, fMAX is specified to address two major classes of synchronous designs.

The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is employed (Figure 1). Under these conditions, the frequency of operation is limited by the greater of the data setup time (tsu) or the minimum clock period (tw high + tw low, or tP2). This parameter is designated fMAX (no feedback).

For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins or flip-flop outputs via the internal feedback paths (Figure 2). Under these conditions, fMAX is defined as the reciprocal of (tsu + tCLK), or tP1, and is designated fMAX (feedback).

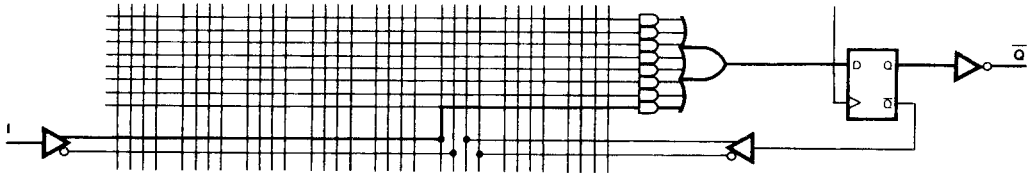


Figure 1. Data Path Register Configuration Without Feedback, Q: = I

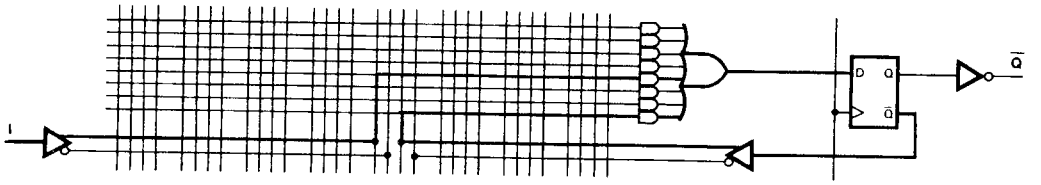


Figure 2. State Machine Configuration With Feedback, Q: = I + $\overline{Q}$

Use of XOR Product Term

The speed of the PAL32VX10 is specified according to the use of the Exclusive-OR (XOR) product term in the macrocell. Note that the macrocell data input is a function of the two-input XOR gate, whose inputs are the OR of the product terms P1-Pn and the single additional XOR product term (Figure 3).

The specification for the path through the single XOR product term is 5ns slower than through the P1-Pn product terms and the OR gate. As a result, if the single XOR product term is changing, the macrocell data input will not be available until 5ns later than if only the P1-Pn product terms were changing.

This difference between paths affects tPD, tsu, and fMAX (feedback). As a result, these three parameters are specified both for only the P1-Pn product terms changing ("Product terms P1-Pn") and with the single XOR product term changing ("Product term XOR") (Figure 4).

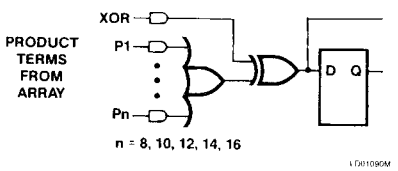


Figure 3.

SPECIFICATION		EXPLANATION
t_{PD}, t_{su}, f_{MAX} (feedback)	Product terms P1-Pn	If only the P1-Pn product terms are changing (XOR term is not changing)
	Product term XOR	If XOR term is changing

Figure 4.

MANUFACTURER	PROGRAMMER CONFIGURATION
Data I/O Corp. 10525 Willows Rd. NE, PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	System 29A, 29B LogicPak™ 303A Adapter 303A-011A/B-V01 Family/Pinout Code: 22-77
Digelec Inc. 1602 Lawrence Ave., Suite 113 Ocean, NJ 07712 (201) 493-2420	Contact manufacturer
Digital Media 11770 East Warner Ave., Suite 225 Fountain Valley, CA 92708 (714) 751-1373	Contact manufacturer
Japan Macnics Corp. 2999 Monterey/Salinas Hwy. Monterey, CA 93940 (408) 373-3607	Contact manufacturer
Kontron Electronics Inc. 1230 Charleston Rd. Mountain View, CA 94039-7230 (415) 965-7020	System EPP-80 Module UPM-B rev. 1.48 or later
Microprоss Parc d'activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq (20) 47.90.40	Contact manufacturer
Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale, CA 94089 (408) 745-1991	Contact manufacturer
Storey Systems 3201 N. Hwy 67, Suite H Mesquite, TX 75150 (214) 270-4135	Contact manufacturer
Structured Design 988 Bryant Way Sunnyvale, CA 94087 (408) 988-0725	Contact manufacturer
Valley Data Sciences Charleston Business Park 2426 Charleston Rd. Mountain View, CA 94043 (415) 968-2900	Contact manufacturer
Varix Corp. 1210 E. Campbell Rd., Suite 100 Richardson, TX 75081 (214) 437-0777	Contact manufacturer
MANUFACTURER	**SOFTWARE DEVELOPMENT SYSTEM**
Monolithic Memories, Inc. IdeaLogic® Exchange M/S 09-25 2175 Mission College Blvd. Santa Clara, CA 95054-1592 (800) 247-6527 ext. 6105	PALASM® 2 Software rev. 2.21 and later
Data I/O Corp. 10525 Willows Rd. NE, PO Box 97046 Redmond, WA 90873-9746 (800) 247-5700	ABEL™ Software — Contact manufacturer
Personal CAD Systems Assisted Technology Division 1290 Parkmoor Ave. San Jose, CA 95126 (408) 971-1300	CUPL™ Software — Contact manufacturer

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LogicPak and ABEL are trademarks of Data I/O Corporation.
CUPL is a trademark of Personal CAD Systems.

Features/Benefits

- User-programmable synchronous state machine
- 25MHz maximum frequency for compatibility with 12.5MHz processors
- 14 inputs (8 external), 8 outputs, 128 states
- PAL® array optimizes product terms and states
- Internal feedback adds versatility and control
- Optimized for four-way branching
- User-selectable asynchronous preset or asynchronous enable function
- Power-up preset for start-up in known state
- Diagnostics-On-Chip™ shadow register eases chip and board-level testing
- PROSE™ device software makes it easy to "write your sequencer in PROSE"
- Programmed on standard logic programmers
- Security fuse prevents pattern duplication
- Space-saving 24-pin 300-mil SKINNYDIP® and 28-pin PLCC and LCC packages

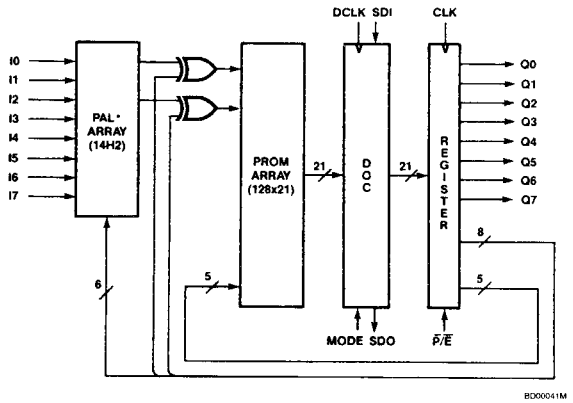
Description

The PMS14R21 programmable sequencer is the first member of the PROSE (PROgrammable SEquencer) family. The PMS14R21 is a high-speed, 14-input, 8-output state machine. It consists of a 128x21 PROM array preceded by a 14H2 PAL array. The PAL array is efficient for a large number of input conditions, while the PROM array is optimal for a large number of product terms and states. The combination allows a very efficient state machine with a large number of inputs and state bits. The PAL array, with eight product terms per output, operates on the eight conditional and six state inputs to select two control bits to the PROM. Two Exclusive-OR gates between the two arrays help to minimize product terms and redundant states. Five lines feed back from the PROM to form the primary address for the next state. The PROM stores up to 128 states of eight outputs and thirteen feedback control signals.

Applications

- High speed sequential logic
- Peripheral controller
- Cache control sequencer
- Signal processing sequencer
- Industrial control

Block Diagram

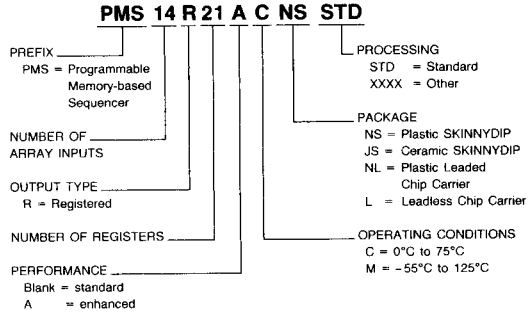


Definition of Signals

I0-I7	Primary inputs to the PAL array
Q0-Q7	Outputs from the register
$\overline{P}/\overline{E}$	Programmable asynchronous preset ($\overline{P}$) or asynchronous enable ($\overline{E}$)
CLK	Clock for output register
DCLK	Clock for diagnostic register
MODE	Selects diagnostic functions
SDI	Serial data input to shadow register
SDO	Serial data output from shadow register

PROSE™ and Diagnostics-On-Chip™ are trademarks of Monolithic Memories, Inc.

PROSE Part Numbering System



Diagnostics-On-Chip Feature

The PMS14R21 is the newest member of the Diagnostics-On-Chip family. These devices incorporate a serial shadow register on-chip which facilitates board-level testing. The shadow register has a Serial Data Input (SDI), Serial Data Output (SDO) and its own clock (DCLK). The MODE control configures the shadow register either in parallel with the output register or in serial shift mode (see function table). Other devices with this feature are listed below.

Diagnostics Family Members

PART NUMBER	DESCRIPTION
53/63DA441	1K x 4 PROM (async. enables)
53/63DA442	1K x 4 PROM (async/sync. enables)
53/63DA841	2K x 4 PROM
53/63D1641	4K x 4 PROM (async. enable)
53/63DA1643	4K x 4 PROM (async. initialization)
54/74S818	8-bit register

Software Support

PROSE device software from Monolithic Memories provides full support for the PMS14R21. Based on PALASM®2 syntax, the software automatically converts a state machine description directly into the PAL and PROM array fuse maps, for downloading to a programmer. The syntax supports both Mealy and Moore state machine models, and makes optimal use of the features of the PROSE device. Simulation support is also provided, both for design checking and for generation of test vectors for device testing. Additional support is available from third-party software vendors, including the ABEL™ package from Data I/O.

Programming

Both the PAL and PROM arrays are programmed on standard logic programmers using the JEDEC programming format. The TiW fuses program from the low to the high state. Programming also sets the architectural fuse which selects between asynchronous preset or asynchronous output enable; the unprogrammed state is preset. If asynchronous preset is selected, asserting the pin low will set all outputs and feedback bits high.

Power-up Preset

Power-up preset is provided for system start-up in a known state. It has the same effect as preset; all output register bits go high.

Diagnostic Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	$Q_{20} - Q_0$	$S_{20} - S_0$	SDO	
L	X	↑	*	$Q_n \leftarrow$ PROM	HOLD	S_{20}	Load output register from PROM array
L	X	*	↑	HOLD	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow$ SDI	S_{20}	Shift shadow register data
L	X	↑	↑	$Q_n \leftarrow$ PROM	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow$ SDI	S_{20}	Load output register from PROM array while shifting shadow register data
H	X	↑	*	$Q_n \leftarrow S_n$	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	$S_n \leftarrow Q_n$	SDI	Load shadow register from output bus and feedback
H	H	*	↑	HOLD	HOLD	SDI	† No operation

* Clock must be steady or falling.
† Reserved operation for 54/74S818 8-Bit Diagnostic Register.

Features/Benefits

- 20 logic inputs: 12 external, 8 feedback
- 8 outputs with programmable polarity
- ECL technology for ultra-high speed — max t_{PD} = 6ns
- 32 product terms with term sharing
- 10KH ECL compatible
- Fully AC tested
- Input pull-down resistors
- Voltage compensated
- Space-saving 24-pin SKINNYDIP® and 28-pin PLCC packages
- Programmable using standard TTL programmers with adapter
- Greater than 99% programming yield
- Security fuse prevents unauthorized copying

Description

The PAL10H20P8 is a 10KH family compatible ECL PAL device having twelve dedicated inputs and eight outputs with feedback. A programmable AND array and a fixed OR array make possible the implementation of a wide variety of logic functions with far fewer packages than with SSI devices. The logic is implemented by opening metal fuse connections within the AND array. Designs can be specified by using any of a variety of software packages which accept the design and assemble a file that can be downloaded into a device programmer. Fuses are programmed using any of the qualified PAL device programmers.

The outputs are equipped with programmable polarity. They can drive a 50Ω termination (to V_{CC} – 2.0V). Product term sharing is provided to allow greater flexibility in assigning product terms to outputs.

The input pins have 50kΩ internal pull-down resistors, which allow unused inputs to be left open. Open inputs will assume a logic low state.

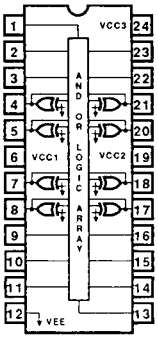
Features

Each output has a programmable polarity fuse, allowing for more efficient representation of many logic functions. Each output is active high with polarity fuse intact, and active low with the polarity fuse blown.

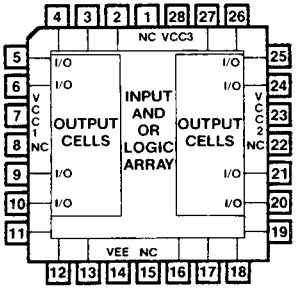
The programmable AND array contains a total of thirty-two product terms. Product terms are arranged in groups of eight. The terms in each group can be shared mutually exclusively between two adjacent output cells. If a particular product term is needed for two outputs, then two identical product terms are generated: one for each output.

A security fuse is provided to help protect the fuse pattern from unauthorized copying. Once the security fuse has been programmed, it is no longer possible to verify the contents of the fuse array electrically. The security fuse has no effect on functionality.

DIP Pinout



PLCC Pinout



CD00880M

Absolute Maximum Ratings

These ratings specify the conditions above which the device may be permanently damaged. AC and DC specifications are not necessarily guaranteed over this range.

Supply voltage V_{EE} ($V_{CC1} = V_{CC2} = V_{CC3} = 0V$) ..... −8.0V to 0V
Input voltage V_I ($V_{CC1} = V_{CC2} = V_{CC3} = 0V$) ..... 0V to V_{EE}
Output current, I_{OUT}
Continuous 35mA
Surge 100mA
Storage temperature range, T_{stg} ..... −65°C to 150°C

Operating Conditions

SYMBOL	PARAMETER	COMMERCIAL			UNIT
		MIN	TYP	MAX	
V_{EE}	Supply voltage (V_{CC} = 0V)	−5.46	−5.2	−4.94	V
T_A	Operating free-air temperature	0		75	°C

Electrical Characteristics V_{EE} = −5.2V ± 5% (See note 1)

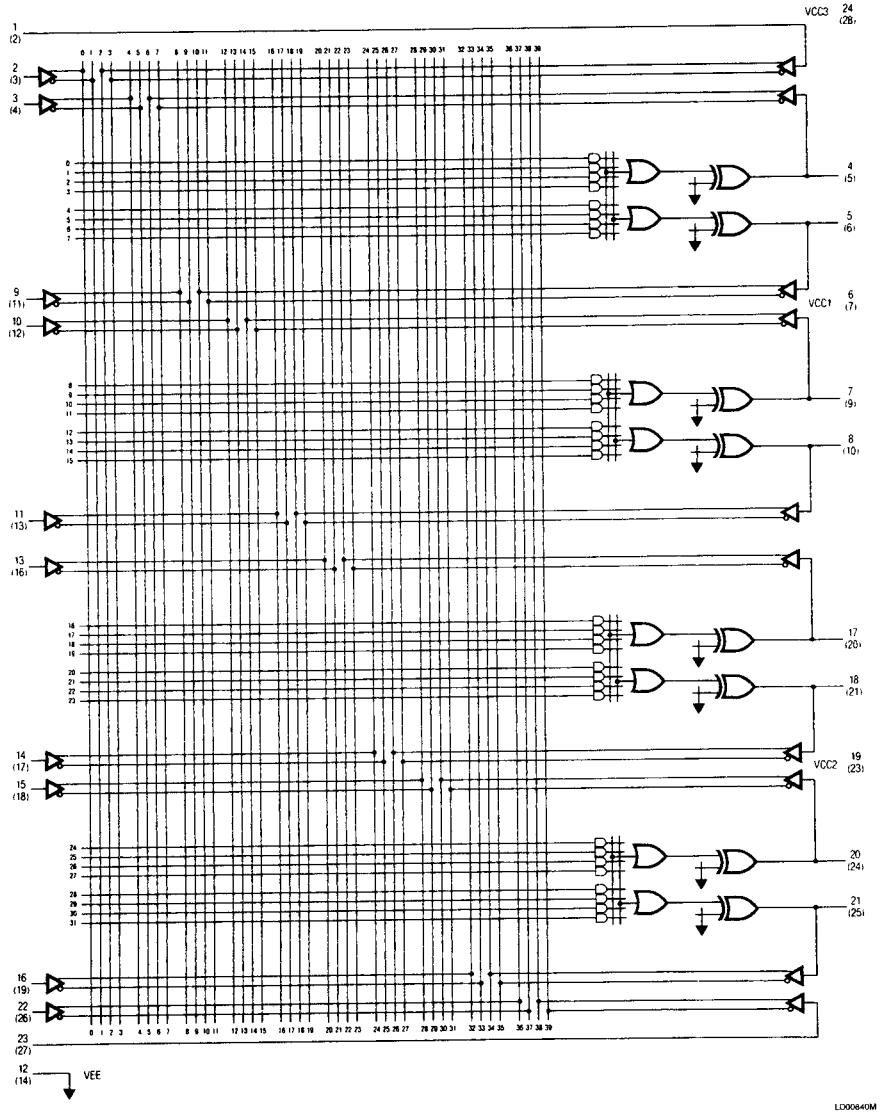
SYMBOL	PARAMETER	TEST CONDITIONS	0°C		25°C		75°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
I_{EE}	Power supply current	Inputs $V_{IN} = V_{IH}$ Max	–	210	–	210	–	210	mA
I_{inH}	Input current high	V_{IH} Min < V_{in} < V_{IH} Max	–	425	–	265	–	265	μA
I_{inL}	Input current low	V_{IL} Min < V_{in} < V_{IL} Max	0.5	–	0.5	–	0.3	–	μA
V_{OH}	High output voltage	(See Note 2)	−1.02	−0.84	−0.98	−0.81	−0.92	−0.735	V_{dc}
V_{OL}	Low output voltage	(See Note 2)	−1.95	−1.63	−1.95	−1.63	−1.95	−1.60	V_{dc}
V_{IH}	High input voltage	(See Note 2)	−1.17	−0.84	−1.13	−0.81	−1.07	−0.735	V_{dc}
V_{IL}	Low input voltage	(See Note 2)	−1.95	−1.48	−1.95	−1.48	−1.95	−1.45	V_{dc}

Switching Characteristics V_{EE} = −5.2V ± 5% (See note 2)

SYMBOL	PARAMETER	0°C		25°C		75°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PD}	Propagation delay	2.0	6.0	2.0	6.0	2.0	6.0	ns
t_R	Rise time (20%-80%)	0.7	2.2	0.7	2.0	0.7	2.2	ns
t_F	Fall time (80%-20%)	0.7	2.2	0.7	2.0	0.7	2.2	ns

Note: 1. Each ECL 10KH series circuit has been designed to meet the specifications shown in test table after thermal equilibrium has been established. The circuit is in test socket or mounted on a printed board and transverse air flow greater than 500 linear fpm is maintained.
2. Outputs are terminated through a 50Ω resistor to V_{CC} − 2.0V. Discrete carbon resistors should be used for terminations. Multiple-resistor packs and metal film discrete resistors are inductive and should be avoided. The single-ended nature of the outputs demands strict adherence to ground and termination plane design techniques.
3. If pin 13 (PLCC pin 16) is not used, it should be left open or terminated to V_{TT} (= V_{CC} − 2.0V). It should not be terminated to V_{EE}.

Logic Diagram



MegaPAL Devices

	ARRAY INPUTS	REGISTERED OUTPUTS	t_{PD} (ns)	I_{CC} (mA)
PAL32R16	32	16	40	280
PAL64R32	64	32	50	640

Description

The MegaPAL Devices offer very high density programmable logic.

Programmable Polarity

Each flip-flop has individually programmable polarity. The unprogrammed state is active low.

Product Term Sharing

Product term sharing allows each pair of outputs to share its product terms with one output or the other (not both). Each pair has a total of sixteen product terms; thus, one output can use zero to sixteen terms while the other has sixteen to zero. Product terms can only be shared mutually exclusively. If both outputs need the same term, it must be created twice, once for each output.

Register Bypass

Registers in either device can be bypassed in banks of eight, creating a set of combinatorial outputs.

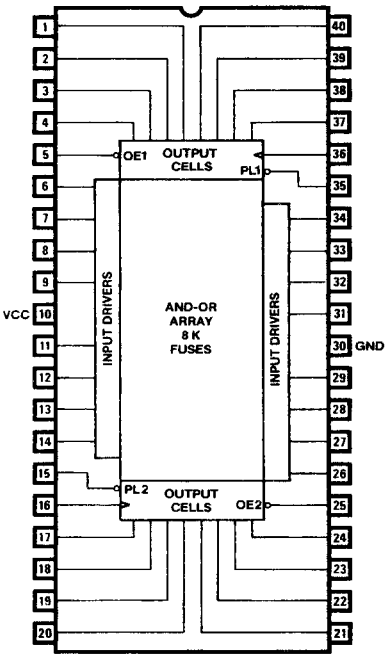
Reset

The PAL64R32 also features asynchronous reset (previously called preset). The reset function sets a bank of eight registers to a logic LOW, setting the output HIGH if active low.

Register Preload and Power-up Reset

Both devices also offer register preload for device testability. The registers can be preloaded from the outputs by using TTL level signals in order to simplify functional testing. This series also offers Power-up Reset, whereby the registers power up to a logic LOW, setting active-low outputs to a logic HIGH.

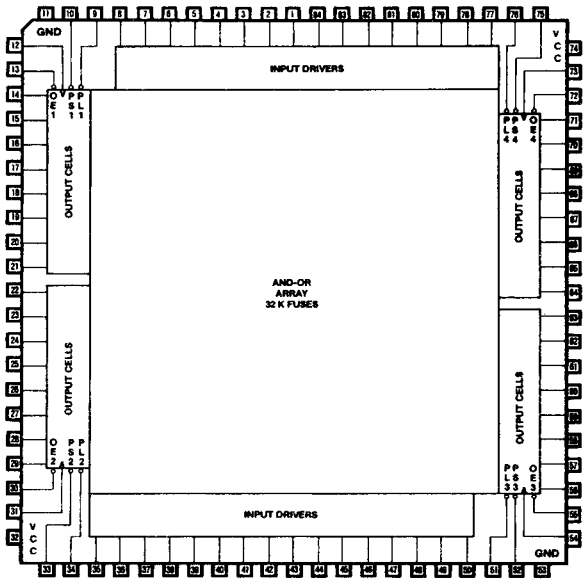
32R16



DIP

CD00250M

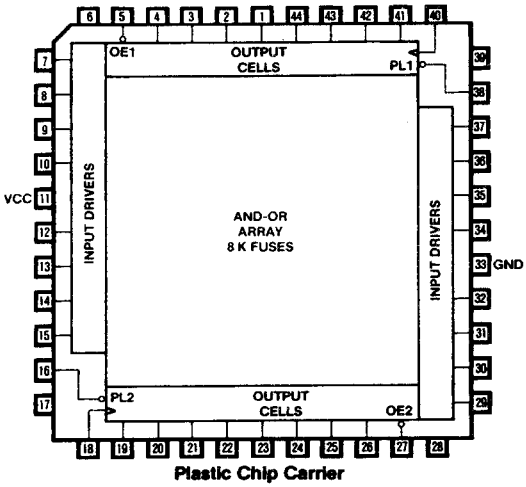
64R32



Plastic Chip Carrier

CD00260M

32R16



Plastic Chip Carrier

CD00270M

Testing Conditions

SYMBOL	PARAMETER	COMMERCIAL			UNIT
		MIN	TYP	MAX	
t_{wp}	Preload pulse width	35			ns
t_{sup}	Preload setup time	50			ns
t_{hp}	Preload hold time	5			ns
t_{PRW}	Preset pulse width	25			ns
t_{PRR}	Preset recovery time	35			ns

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25			20			ns
		High	25			20			
t_{wp}	Preload pulse width		45			35			ns
t_{su}	Setup time for input to clock	Polarity fuse intact	50			40			ns
		Polarity fuse blown	50			40			
t_{sup}	Preload setup time		30			25			ns
t_h	Hold time		0	−10		0	−10		ns
t_{hp}	Preload hold time		10			5			ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics (Over Operating Conditions)

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage						0.8	V
V_{IH}[1]	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}[2]	Low-level input current	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[2]	High-level input current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Mil	I_{OL} = 8mA		0.3	0.5	V
			Com	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	Mil	I_{OH} = −2mA	2.4	2.8		V
			Com	I_{OH} = −3.2mA				
I_{OZL}[2]	Off-state output current	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}[2]				V_O = 2.4V			100	μA
I_{OS}[3]	Output short-circuit current	V_{CC} = MAX		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				200	280	mA

Switching Characteristics (Over Operating Conditions)

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input to output	Polarity fuse intact	R_1 = 560Ω R_2 = 1.1KΩ			50			40	ns
		Polarity fuse blown				55			45	
t_{CLK}	Clock to output or feedback					30			25	ns
t_{PZX}	Output enable					25			20	ns
t_{PXZ}	Output disable					25			20	ns
f_{MAX}	Maximum frequency			14			16			MHz

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL[1]			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
t_w	Width of clock	Low	20			ns
		High	20			
t_{su}	Setup time from input to clock	Polarity fuse intact	40			ns
		Polarity fuse blown	40			
t_h	Hold time		0	−10		ns
T_A	Operating free-air temperature		0		75	°C
T_C	Operating case temperature					°C

2

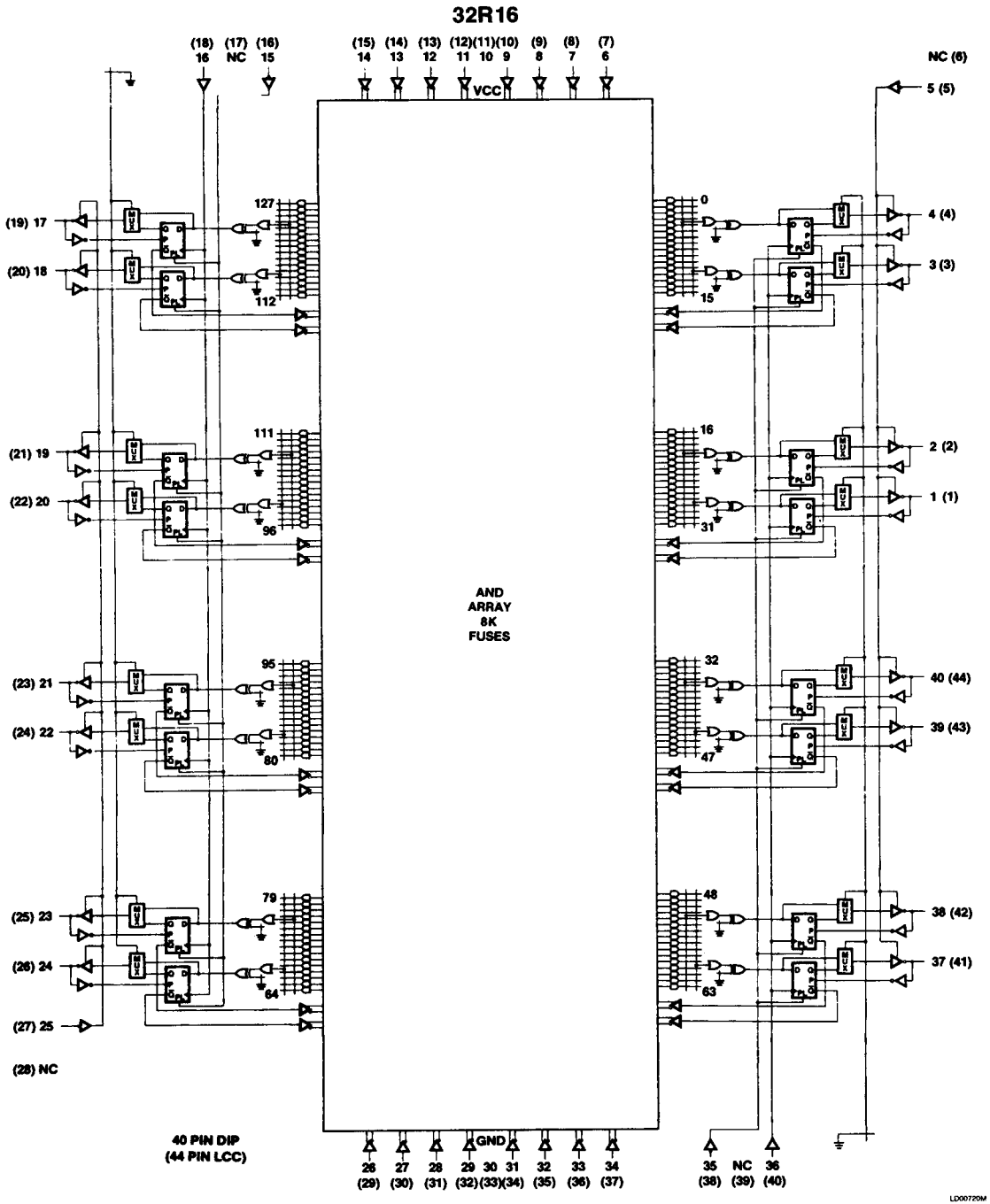
Electrical Characteristics (Over Operating Conditions)

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL			UNIT
				MIN	TYP	MAX	
V_{IL}[2]	Low-level input voltage					0.8	V
V_{IH}[2]	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA		−0.8	−1.5	V
I_{IL}[3]	Low-level input current	V_{CC} = MAX	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}[3]	High-level input current	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 8mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −0.4mA	2.4	2.8		V
I_{OZL}[3]	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−100	μA
I_{OZH}[3]			V_O = 2.4V			100	μA
I_{OS}[4]	Output short-circuit current	V_{CC} = 5V	V_O = 0V	−10	−40	−60	mA
I_{CC}	Supply current	V_{CC} = MAX			400	640	mA

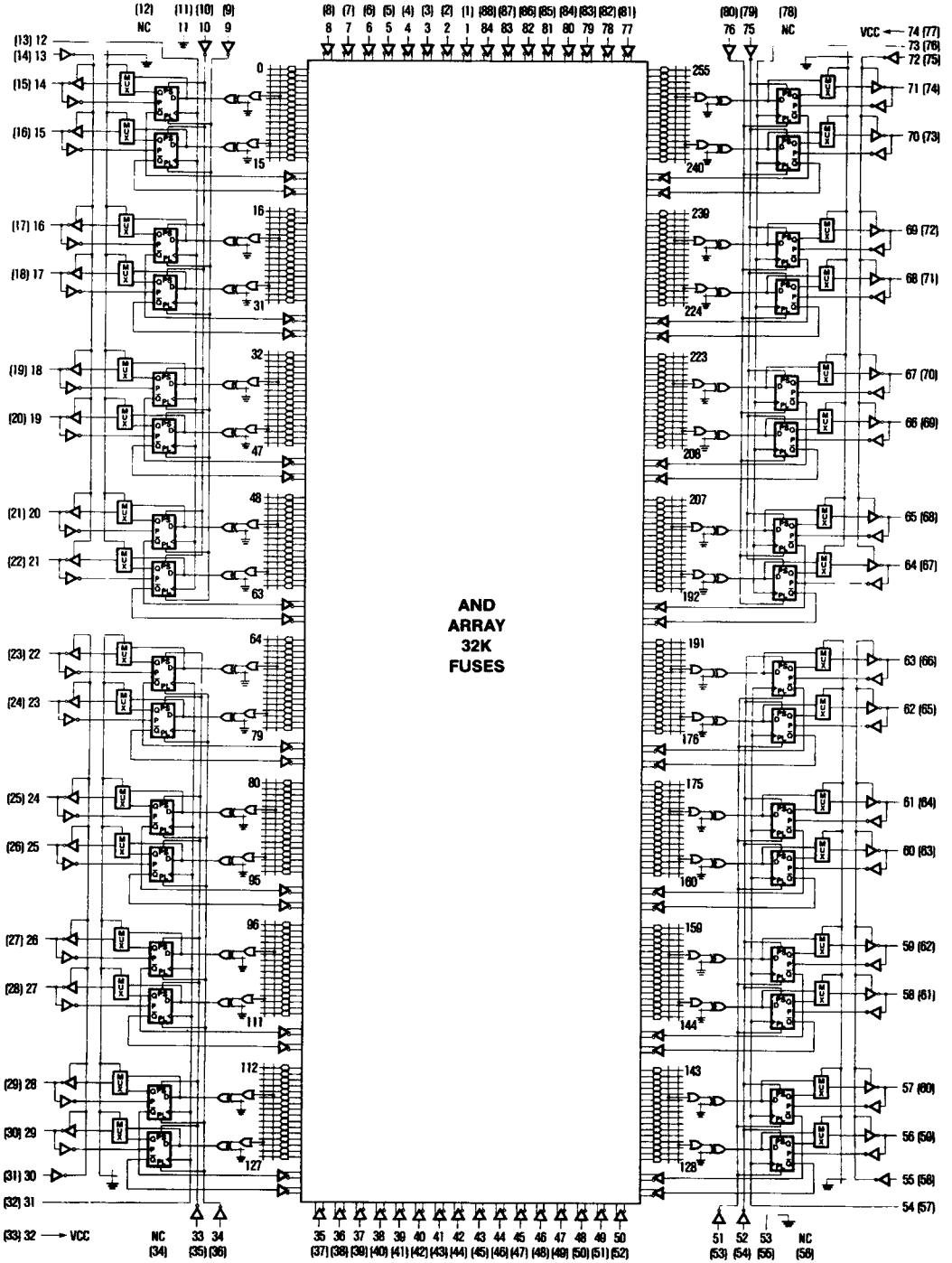
Switching Characteristics (Over Operating Conditions)

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL			UNIT
				MIN	TYP	MAX	
t_{PD}	Input to output	Polarity fuse intact	R_1 = 560Ω R_2 = 1.1KΩ			50	ns
		Polarity fuse blown				55	
t_{CLK}	Clock to output or feedback					22	ns
t_{PZX}	Output enable					30	ns
t_{PXZ}	Output disable					30	ns
t_{PRH}	Preset to output					35	ns
f_{MAX}	Maximum frequency			16	20		MHz

1. The PAL64R32 Series is designed to operate over the full military operating conditions. For availability and specifications, contact Monolithic Memories.
2. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.


32R16
(18) 16
(17) NC
(16) 15
(15) 14
(14) 13
(13) 12
(12) 11
(11) 10
(10) 9
(9) 8
(8) 7
(7) 6
VCC
NC (6)
5 (5)
(19) 17
(20) 18
(21) 19
(22) 20
(23) 21
(24) 22
(25) 23
(26) 24
(27) 25
(28) NC
127
112
111
96
95
80
79
64
0
15
16
31
32
47
48
63
4 (4)
3 (3)
2 (2)
1 (1)
40 (44)
39 (43)
38 (42)
37 (41)
AND
ARRAY
8K
FUSES
40 PIN DIP
(44 PIN LCC)
GND
26 (29)
27 (30)
28 (31)
29 (32)
30 (33)
31 (34)
32 (35)
33 (36)
34 (37)
35 (38)
NC (39)
36 (40)
LD00720M

64R32


AND
ARRAY
32K
FUSES
(12) NC
(11) 11
(10) 10
(9) 9
(8) 8
(7) 7
(6) 6
(5) 5
(4) 4
(3) 3
(2) 2
(1) 1
(88) 84
(87) 83
(86) 82
(85) 81
(84) 80
(83) 79
(82) 78
(81) 77
(80) 76
(79) 75
(78) NC
VCC
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96
111
112
127
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176
191
192
207
206
223
224
239
240
255
LD00730M

f_{MAX} Parameters

The parameter f_{MAX} is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, f_{MAX} for the B-speed devices is specified to address two major classes of synchronous designs.

The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is employed (Figure 1). Under these conditions, the frequency of operation is limited by the greater of the data setup time (t_{su}) or the minimum clock period (t_w high + t_w low). This parameter is designated f_{MAX} (no feedback).

For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins of flip-flop outputs via the internal feedback paths (Figure 2). Under these conditions, f_{MAX} is defined as the reciprocal of (t_{su} + t_{CLK}) and is designated f_{MAX} (feedback).

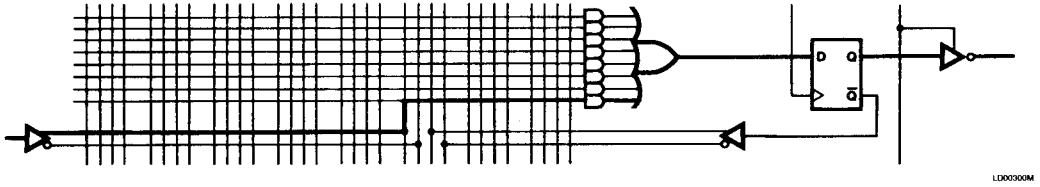


Figure 1. No Feedback

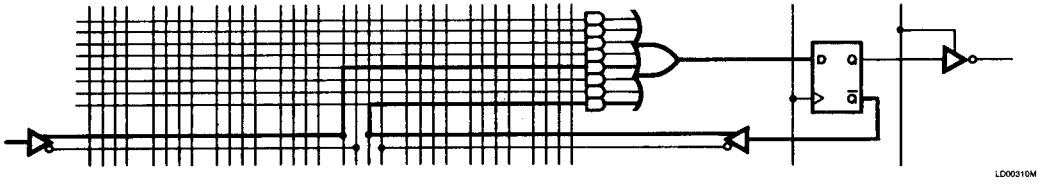


Figure 2. Feedback

Output Register PRELOAD

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for PRELOAD is as follows:

Series 20PA

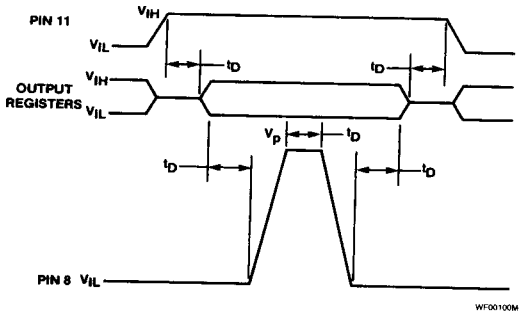
1. Raise V_{CC} to 4.5V.
2. Disable output registers by setting pin 11 to V_{IH}.
3. Apply V_{IL}/V_{IH} to all registered output pins.
4. Pulse pin 8 to V_p, then back to 0V.
5. Remove V_{IL}/V_{IH} from all output registers.
6. Lower pin 11 to V_{IL} to enable the output registers.
7. Verify for V_{OL}/V_{OH} at all registered output pins.

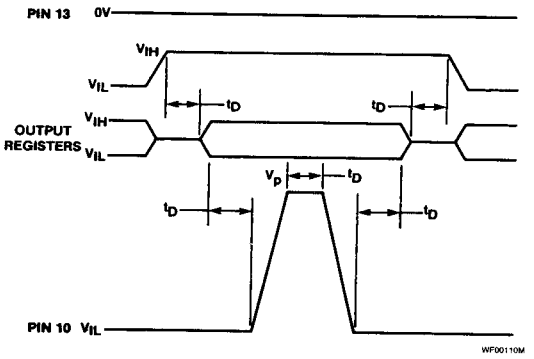
Series 24RS/24XA

1. Raise V_{CC} to 4.5V.
2. Disable output registers by setting pin 13 to V_{IH}.
3. Apply V_{IL}/V_{IH} to all registered output pins.
4. Pulse pin 10 to V_p, then back to 0V.
5. Remove V_{IL}/V_{IH} from all output registers.
6. Lower pin 13 to V_{IL} to enable the output registers.
7. Verify for V_{OL}/V_{OH} at all registered output pins.

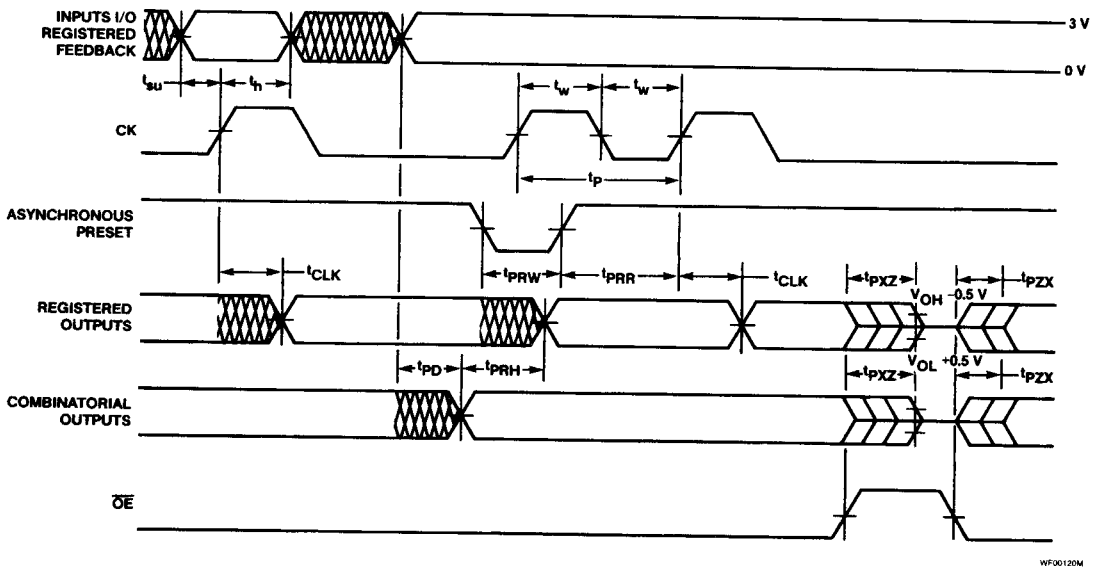
Power-Up RESET

All devices with this PRELOAD feature also have power-up RESET. All registers power up to a logic high for predictable system initialization.





Switching Waveforms



Notes: 1. Input pulse amplitude 0V to 3.0V.
2. Input access measured at the 1.5V level.

f_{MAX} Parameters

The parameter f_{MAX} is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, f_{MAX} for the B-speed devices is specified to address two major classes of synchronous designs.

The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is employed (Figure 1). Under these conditions, the frequency of operation is limited by the greater of the data setup time (t_{su}) or the minimum clock period (t_w high + t_w low). This parameter is designated f_{MAX} (no feedback).

For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins of flip-flop outputs via the internal feedback paths (Figure 2). Under these conditions, f_{MAX} is defined as the reciprocal of (t_{su} + t_{CLK}) and is designated f_{MAX} (feedback).

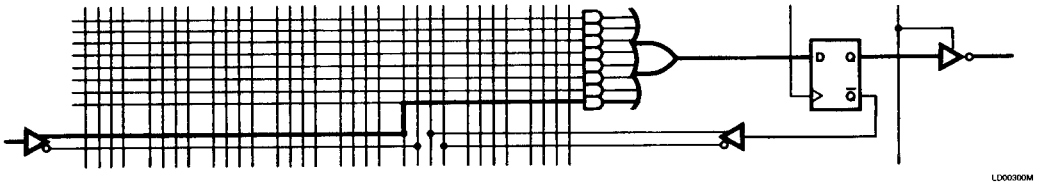


Figure 1. No Feedback

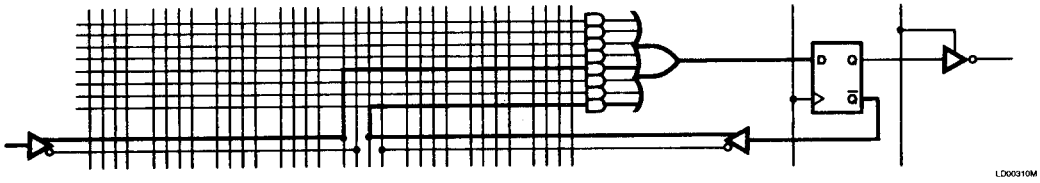


Figure 2. Feedback

Output Register PRELOAD

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for PRELOAD is as follows:

Series 20PA

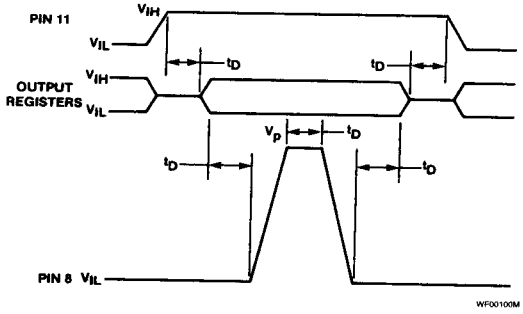
1. Raise V_{CC} to 4.5V.
2. Disable output registers by setting pin 11 to V_{IH}.
3. Apply V_{IL}/V_{IH} to all registered output pins.
4. Pulse pin 8 to V_p, then back to 0V.
5. Remove V_{IL}/V_{IH} from all output registers.
6. Lower pin 11 to V_{IL} to enable the output registers.
7. Verify for V_{OL}/V_{OH} at all registered output pins.

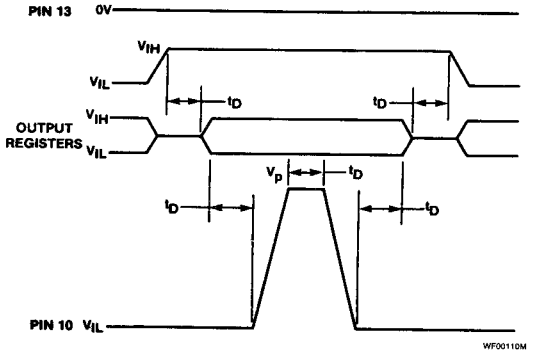
Series 24RS/24XA

1. Raise V_{CC} to 4.5V.
2. Disable output registers by setting pin 13 to V_{IH}.
3. Apply V_{IL}/V_{IH} to all registered output pins.
4. Pulse pin 10 to V_p, then back to 0V.
5. Remove V_{IL}/V_{IH} from all output registers.
6. Lower pin 13 to V_{IL} to enable the output registers.
7. Verify for V_{OL}/V_{OH} at all registered output pins.

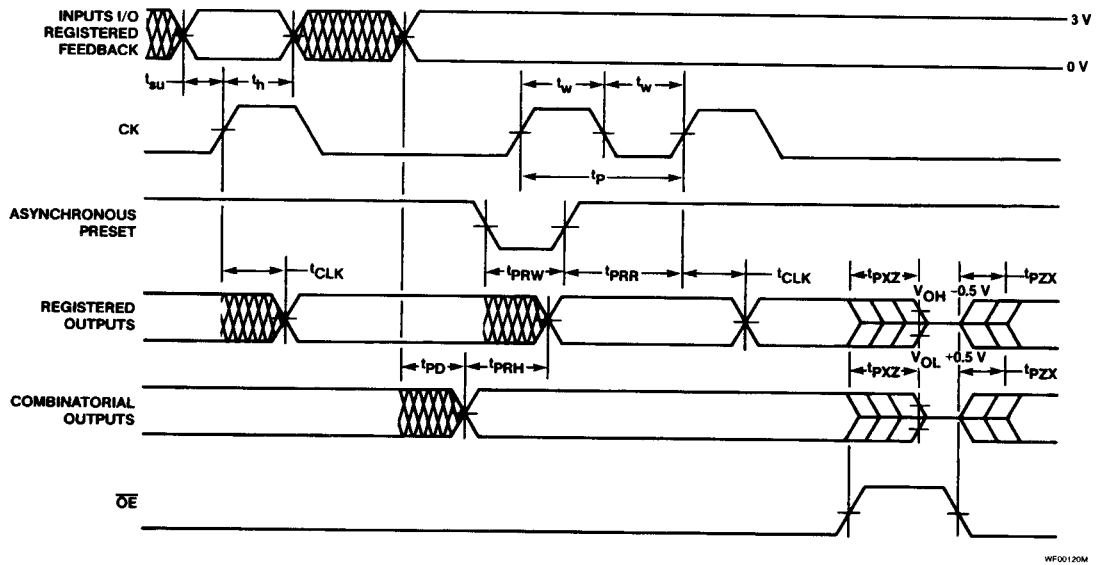
Power-Up RESET

All devices with this PRELOAD feature also have power-up RESET. All registers power up to a logic high for predictable system initialization.





Switching Waveforms

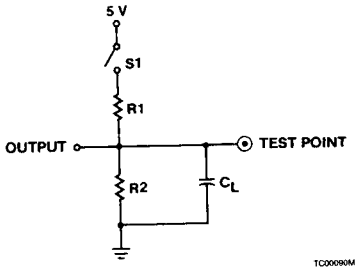


Notes: 1. Input pulse amplitude 0V to 3.0V.
2. Input access measured at the 1.5V level.

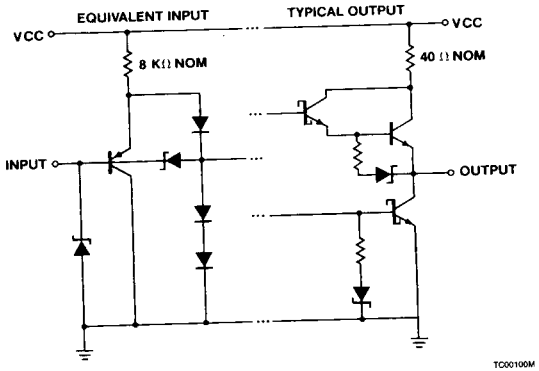
Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5V to 7V	−0.5V to 12V
Input voltage	−1.5V to 5.5V	−1.0V to 22V
Off-state output voltage	5.5V	12V
Storage temperature		−65°C to +150°C

Switching Test Load



Schematic of Inputs and Outputs



Notes:
1. t_{PD} is tested with switch S_1 closed, C_L = 50pF and measured at 1.5V output level.
2. t_{PZX} is measured at the 1.5V output level with C_L = 50pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5V output level.