Signetics

PLS163
Field-Programmable Address Decoder (12 × 9)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 24**

DESCRIPTION

The PLS163 is a bipolar, Field-Programmable Address Decoder. The device consists of nine AND/NAND gates which share 12 common inputs. The type of gate is selected by programming the output as active-High (H) or active-Low (L). Each of the 12 inputs $I_0 - I_{11}$ can be programmed to provide the True (H), Complement (L), or Don't Care (—) state to each of the nine AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

The device is field programmable, which means that custom patterns are immediately available.

The PLS163 includes chip-enable control for output strobing and inhibit. It features 3-State outputs for ease of expansion of input variables and application in bus-organized systems.

Order codes are listed in the Ordering Information Table.

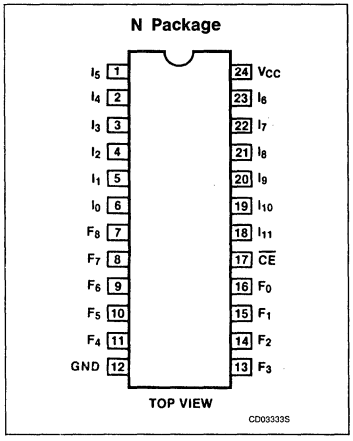
FEATURES

- **Field-Programmable (Ni-Cr link)**
- **12 input variables**
- **9 output functions**
- **Chip Enable input**
- **I/O propagation delay: 30ns (max.)**
- **Power dissipation: 600mW (typ.)**
- **Input loading: −100μA (max.)**
- **3-State outputs**
- **Output disable function: Hi-Z**
- **Fully TTL compatible**

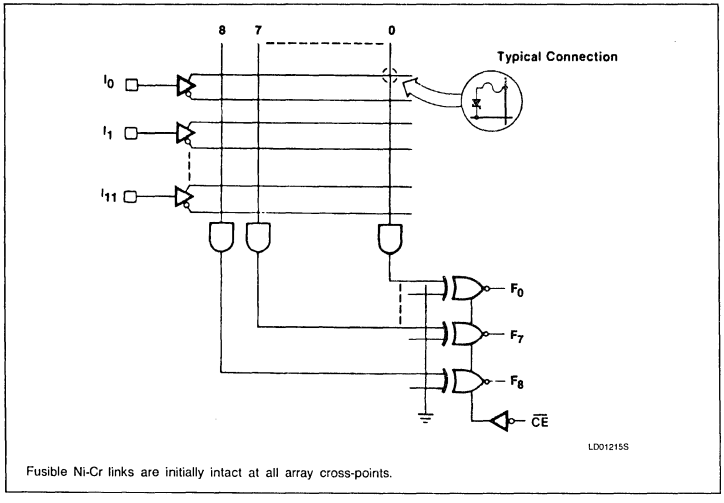
APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



Fusible Ni-Cr links are initially intact at all array cross-points.

LOGIC FUNCTION

TYPICAL OUTPUT FUNCTIONS:

ACTIVE-HIGH

$X = A \cdot \overline{B} \cdot C \cdot \ldots$

ACTIVE-LOW

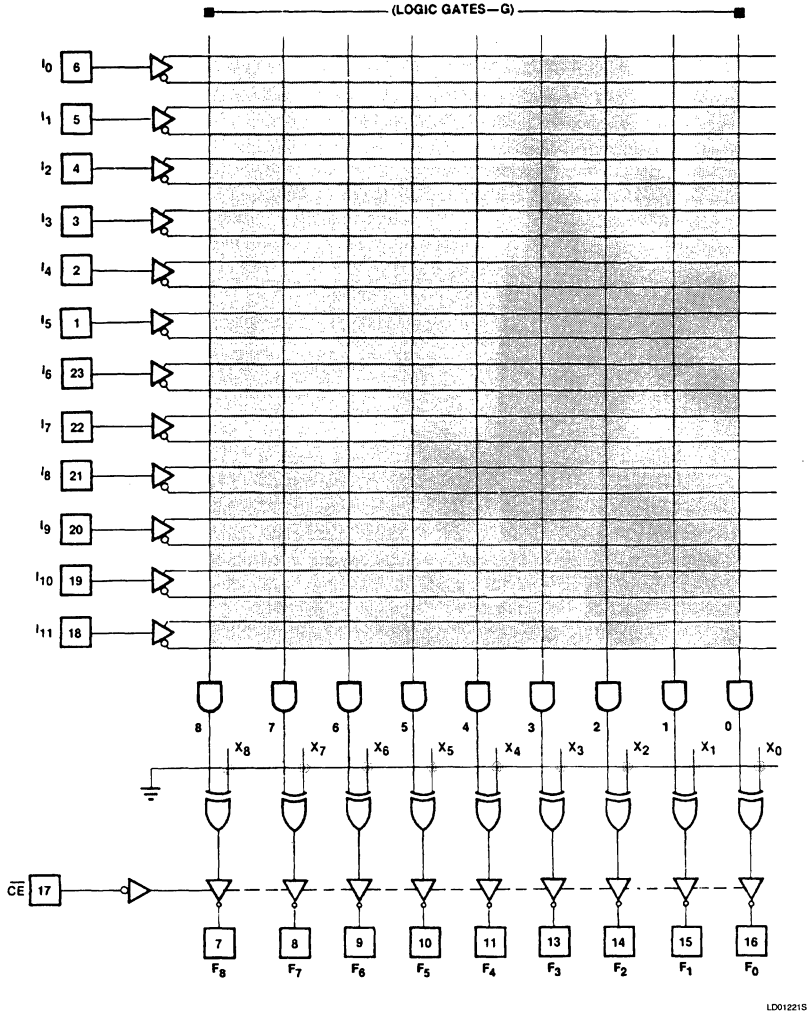
$\overline{X} = A \cdot \overline{B} \cdot C \cdot \ldots$

$X = \overline{A} + B + \overline{C} + \ldots$

NOTES:
1. For each of the 9 outputs, either function X (active-High) or $\overline{X}$ (active-Low) is available, but not both. The desired output polarity is programmed via the Ex-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and output pins (F).

Field-Programmable Address Decoder (12 × 9) PLS163

FPAD LOGIC DIAGRAM



NOTES:
1. All gate inputs with a blown link float to a logic "1".
2. ◌ Programmable connection.

Field-Programmable Address Decoder (12 × 9) PLS163

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Plastic DIP 300mil-wide	PLS163N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C,\ 4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[2]	Max	
Input voltage						
V_{IH}	High[1]	V_{CC} = Max	2.0			V
V_{IL}	Low[1]	V_{CC} = Min			0.8	V
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	V
Output voltage						
V_{OH}	High[1,5]	V_{CC} = Min, I_{OH} = −2mA	2.4			V
V_{OL}	Low[1,4]	I_{OL} = 15mA		0.35	0.5	V
Input current						
I_{IH}	High	V_{CC} = Max, V_{IN} = 5.5V		< 1	40	μA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	μA
Output current						
$I_{O\ (OFF)}$	Hi-Z state[6]	V_{CC} = Max, V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	μA
I_{OS}	Short circuit[3,7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	155	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5.0V, V_{IN} = 2.0V		8		pF
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15		pF

Notes on following page.

Field-Programmable Address Decoder (12 × 9) PLS163

AC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

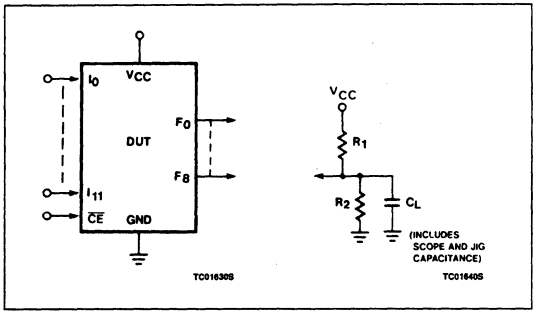
SYMBOL	PARAMETER	TO	FROM	TEST CONDITION	LIMITS			UNIT
					Min	Typ[2]	Max	
t_{PD}	Propagation delay	Output	Input	$C_L = 30pF$		20	30	ns
t_{CE}	Chip enable	Output	Chip enable	$C_L = 30pF$		20	30	ns
t_{CD}	Chip disable	Output	Chip enable	$C_L = 5pF$		20	30	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. Test each pin one at a time.
4. Measure with a programmed logic condition for which the output under test is at low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the outputs open.

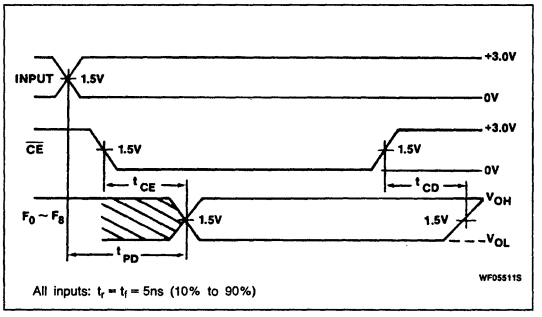
4

Field-Programmable Address Decoder (12 × 9) PLS163

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



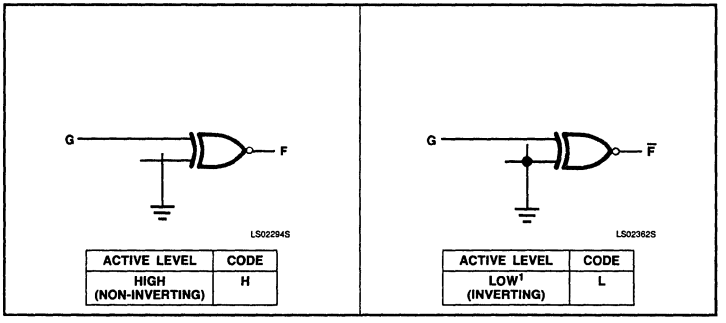
LOGIC PROGRAMMING

PLS163 logic designs can be generated using Signetics' AMAZE PLD design software or one of several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry is accepted.

PLS163 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

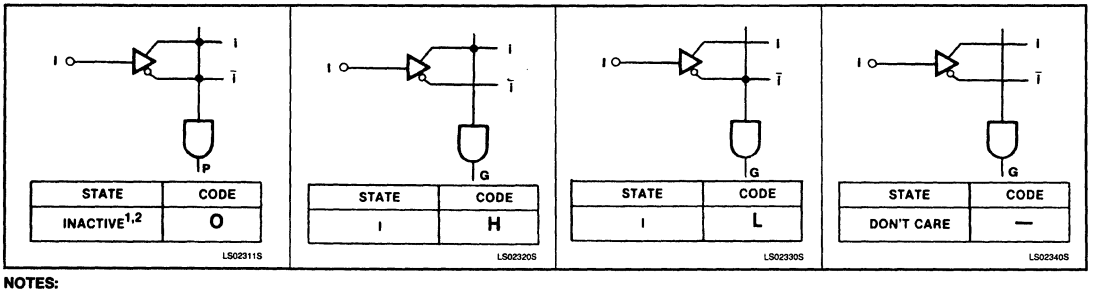
OUTPUT POLARITY – (F)



ACTIVE LEVEL	CODE
HIGH (NON-INVERTING)	H

ACTIVE LEVEL	CODE
LOW[1] (INVERTING)	L

"AND" ARRAY – (I)



STATE	CODE
INACTIVE[1,2]	O

STATE	CODE
I	H

STATE	CODE
I	L

STATE	CODE
DON'T CARE	—

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate G_n will be unconditionally inhibited if both the True and Complement fuses of any input (I) are left intact.

VIRGIN DEVICE

The PLS163 is shipped in an unprogrammed state, in which:

1. All P_n terms are disabled. (Inactive).
2. All P_n terms are active on all outputs.
3. All outputs are active-Low.

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FPAD PROGRAM TABLE

CUSTOMER NAME _____	THIS PORTION TO BE COMPLETED BY SIGNETICS
PURCHASE ORDER # _____	CF (XXXX) _____
SIGNETICS DEVICE # _____	CUSTOMER SYMBOLIZED PART # _____
TOTAL NUMBER OF PARTS _____	DATE RECEIVED _____
PROGRAM TABLE # _____	COMMENTS _____

F_0 (16) _____ = _____

F_1 (15) _____ = _____

F_2 (14) _____ = _____

F_3 (13) _____ = _____

F_4 (11) _____ = _____

F_5 (10) _____ = _____

F_6 (9) _____ = _____

F_7 (8) _____ = _____

F_8 (7) _____ = _____

GATE POLARITY		INPUT I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0
F_0													
F_1													
F_2													
F_3													
F_4													
F_5													
F_6													
F_7													
F_8													
PIN NO.		18	19	20	21	22	23	1	2	3	4	5	6
VARIABLE NAME													

NOTES
1. The FPAD is shipped with all links intact. Thus a background of entries corresponding to states of virgin links exists in the table, shown BLANK for clarity.
2. Unused I bits are normally programmed Don't Care (—).
3. Unused Gates can be left blank.

PROGRAM TABLE ENTRIES

AND (I)		CONTROL (POL.)	
INACTIVE	0	HIGH	H
I	H	LOW	L
$\overline{I}$	L		
Don't Care	—		

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