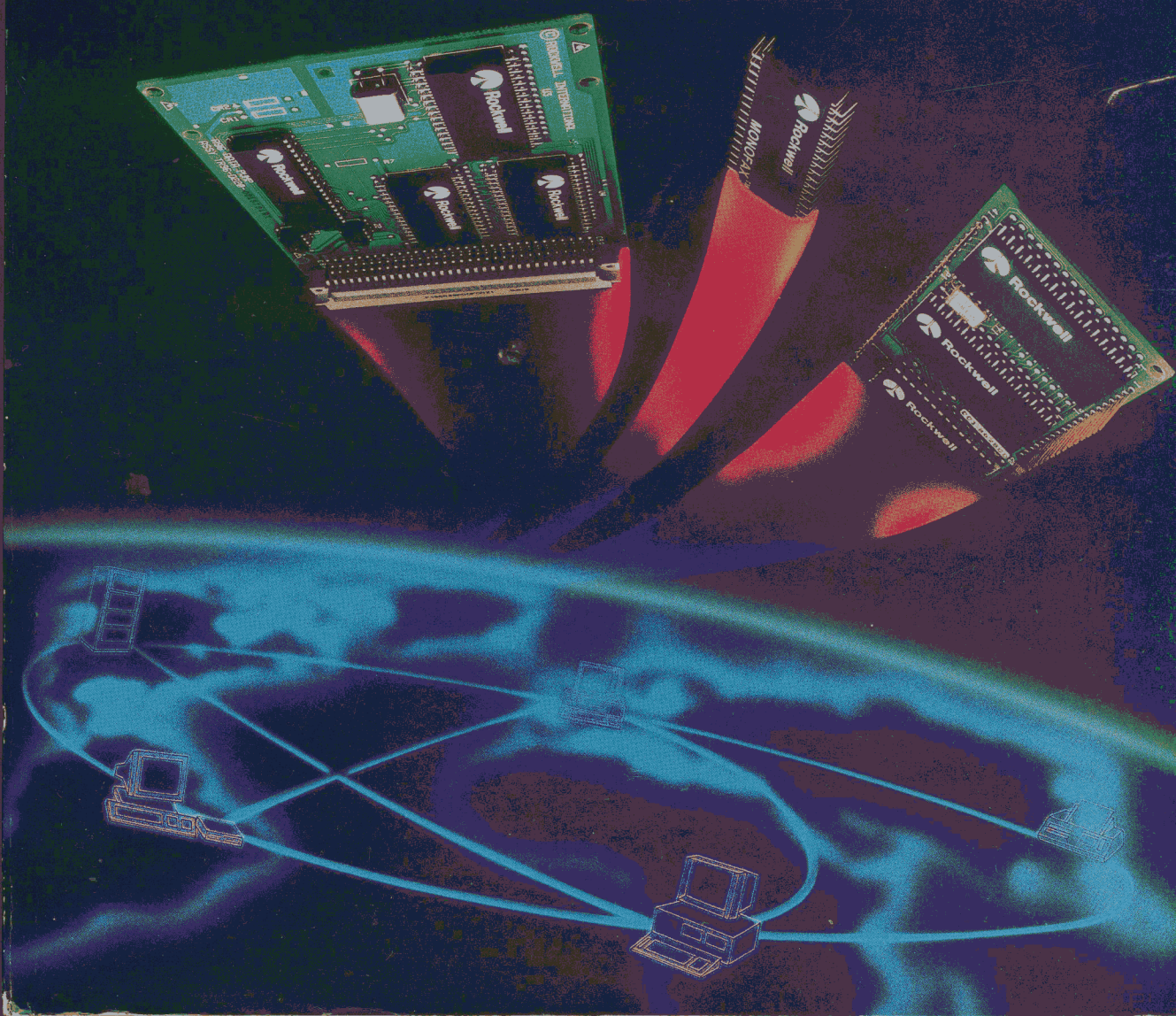
Order No. 1

Rockwell International

Semiconductor Products Division

# MODEM PRODUCTS DATA BOOK



# MODEM PRODUCTS DATA BOOK

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Order No. 1
February, 1987

Rockwell

# R2424
# 2400 bps Full-Duplex Modem

## INTRODUCTION

The Rockwell R2424 is a high performance full-duplex 2400 bps modem. Using state-of-the-art VLSI and signal processing technology, the R2424 provides enhanced performance and reliability. The modem is assembled as a small module with a DIN connector (R2424M and R2424DC) or a new, smaller module (seven square inches) with a dual-in-line pin (DIP) interface.

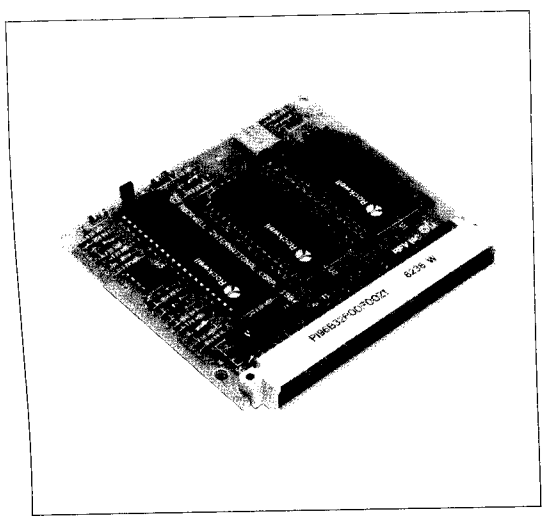
Being CCITT V.22 bis, V.22 A, B compatible, as well as Bell 212A and 103 compatible, the R2424 fits most applications for full-duplex 2400 and 1200 bps fallback (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network, and over point-to-point leased lines.

The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other communications product.

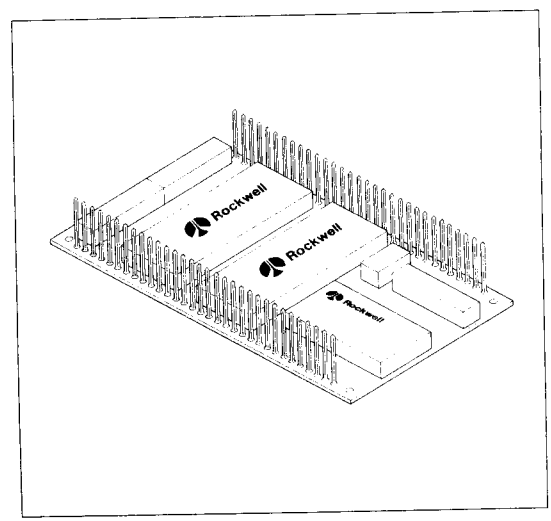
The R2424/DM, with its small form factor and DIP connection, can be automatically installed and soldered onto a host module. Its small size is ideal for internal "1/2-card" PC modem applications. Moreover, the R2424/DM is pin and firmware compatible with the R1212/DM and pin compatible with Rockwell's next generation of medium speed modems, the RC2424 and RC1212.

## FEATURES

- CCITT V.22 bis, V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 2400 bps, 1200 bps, 600 bps ±0.01%
- Asynchronous: 2400 bps, 1200 bps, 600 bps +1%, −2.5%, 0–300 bps
  - — Character Length 8, 9, 10, or 11 bits
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL Compatible
- 2-wire Full-Duplex Operation
- Adaptive and Fixed Compromize Equalization
- Test Configurations:
  - — Local Analog Loopback
  - — Remote Digital Loopback
  - — Self Test
- Auto/Manual Answer
- Auto/Manual Dial—DTMF Tone or Pulse Dial
- Power Consumption: 2.3 Watts Typical
- Power Requirements: +5 Vdc, ±12 Vdc
- Three Module Configurations:
  - — R2424DC (Direct Connect): DIN connector module with FCC approved DAA Part 68 Interface
  - — R2424M: DIN connector module without DAA
  - — R2424/DM: DIP connection module without DAA
- Two Functional Versions
  - — R2424/US All data rates specified except 600 bps
  - — R2424/INT All data rates specified except 0–300 bps



R2424M Modem




R2424/DM Modem

## TECHNICAL SPECIFICATIONS

### TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

The transmitter and signaling frequencies supported in the R2424 are listed in Table 1.

**Table 1. Transmitter Carrier and Signaling Frequencies Specifications**

| Mode | Frequency (Hz ±0.01%) |
|---|---|
| V.22 bis low channel, Originate Mode | 1200 |
| V.22 low channel, Originate Mode | 1200 |
| V.22 bis high channel, Answer Mode | 2400 |
| V.22 high channel, Answer Mode | 2400 |
| Bell 212A high channel Answer Mode | 2400 |
| Bell 212A low channel Originate Mode | 1200 |
| Bell 103/113 Originating Mark | 1270 |
| Bell 103/113 Originating Space | 1070 |
| Bell 103/113 Answer Mark | 2225 |
| Bell 103/113 Answer Space | 2025 |

### TONE GENERATION

The specifications for tone generation are as follows:

1. **Answer Tones:** The R2424 generates echo disabling tones for both the CCITT and Bell configurations, as follows:
   a. CCITT: 2100 Hz ±15 Hz.
   b. Bell: 2225 Hz ±10 Hz.
2. **Guard Tones:** If GTS (see Interface Memory Definitions) is low, an 1800 Hz guard tone frequency is selected; if GTS is high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommendation, the level of transmitted power for the 1800 Hz guard tone is 6 ±1 dB below the level of the data power in the main channel. The total power transmitted to the line is the same whether or not a guard tone is enabled. If a 553.846 Hz guard is used, its transmitted power is 3 ±1 dB below the level of the main channel power, and again the overall power transmitted to the line will remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97 dB and 1.76 dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.
3. **DTMF Tones:** The R2424 generates dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits (see Interface Memory Definitions)must be set to a 1. When in this mode, the specific DTMF tones generated are decided by loading the dial digit register with the appropriate digit as shown in Table 2.

**Table 2. Dial Digits/Tone Pairs**

| Hex | Dial Digits | Tone Pairs | |
|---|---|---|---|
| 00 | 0 | 941 | 1336 |
| 01 | 1 | 697 | 1209 |
| 02 | 2 | 697 | 1336 |
| 03 | 3 | 697 | 1477 |
| 04 | 4 | 770 | 1209 |
| 05 | 5 | 770 | 1336 |
| 06 | 6 | 770 | 1477 |
| 07 | 7 | 852 | 1209 |
| 08 | 8 | 852 | 1336 |
| 09 | 9 | 852 | 1477 |
| 0A | ★ | 941 | 1209 |
| 0B | Spare (B) | 697 | 1633 |
| 0C | Spare (C) | 770 | 1633 |
| 0D | Spare (D) | 852 | 1633 |
| 0E | # | 941 | 1477 |
| 0F | Spare (F) | 941 | 1633 |
| 10 | 1300 Hz Calling Tone | | |

### TONE DETECTION

The R2424 detects tones in the 340 ±5 Hz to 640 ±5 Hz band.
Detection Level: −10 dBm to −43 dBm
Response Time: 17 ±2 ms

### SIGNALING AND DATA RATES

The signaling and data rates for the R2424 are defined in Table 3.

**Table 3. Signaling and Data Rates**

| Operating Mode | Signaling Rate (Baud) | Data Rate |
|---|---|---|
| V.22 bis: | 600 | Synchronous/Asynchronous, 2400 bps ±0.01% |
| V.22 bis: | 600 | Synchronous/Asynchronous, 1200 bps ±0.01% |
| V.22: | | |
| (Alternative A) | | |
| Mode i | 600 | 1200 bps ±0.01% Synchronous |
| Mode iii | 600 | 600 bps ±0.01% Synchronous |
| (Alternative B) | | |
| Mode i | 600 | 1200 bps ±0.01% Synchronous |
| Mode iii | 600 | 600 bps ±0.01% Synchronous |
| Mode ii | | 1200 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character |
| Mode iv | | 600 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character |
| Bell 212A; | 600 | 1200 bps ±0.01%, Synchronous/Asynchronous |
| | 0 to 300 | 0 to 300 bps Asynchronous |

### DATA ENCODING

The specifications for data encoding are as follows:

1. *2400 bps (V.22 bis).* The transmitted data is divided into groups of four consecutive bits (quad bits) forming a 16-point signal structure.
2. *1200 bps (V.22 and Bell 212A).* The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
3. *600 bps (V.22).* Each bit is encoded as a phase change relative to the phase preceding signal elements.

### EQUALIZERS

The R2424 provides equalization functions that improve performance when operating over low quality lines.

**Automatic Adaptive Equalizer**—An automatic adaptive equalizer is provided in the receiver circuit for V.22 bis, V.22 and Bell 212A configurations.

**Fixed Compromise Equalizer**—A fixed compromise equalizer is provided in the transmitter.

### TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ±150 microseconds over the frequency range 900 to 1500 Hz (low channel) and 2100 to 2700 Hz (high channel).

### SCRAMBLER/DESCRAMBLER

The R2424 incorporates a self-synchronizing scrambler-/descrambler. In accordance with the CCITT V.22 bis, V.22 and the Bell 212A recommendations.

### RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R2424 can adapt to received frequency errors of up to ±7 Hz with less than a 0.2 dBm degradation in BER performance.

### RECEIVE LEVEL

The receiver circuit of the R2424 satisfies all specified performance requirements for the received line signals from −10 dBm to −48 dBm. The received line signal is measured at the receiver analog input RXA.

### TRANSMIT LEVEL

The R2424M output control circuitry contains a variable gain buffer which reduces the modem output level. The R2424M can be strapped via the host interface memory to accomplish this.

### PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R2424M transmit level is +6 dBm to allow a Data Access Arrangement (DAA) to be used. The DAA then determines the permissive or programmable configuration.

The R2424DC transmit level is strapped in the permissive mode so that the maximum output level is −10 dBm ±1.0 dBm.

### AUTOMATIC RECONFIGURATION

The R2424 is capable of automatically configuring itself to the compatibility of a remote modem. The R2424 can be in either the answer or originate mode for this to occur. The R2424 adaptation compatibilities are limited to V.22 bis, V.22 A/B (1200 bps), Bell 212, and Bell 103. If the R2424 is to originate in a specific configuration, the MODE bits (see Interface Memory Definitions)must be set.

## MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

## HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, DAA signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The column titled "Type" refers to designations found in the Hardware Circuits Interface Characteristics (Tables 5 and 6). The six groups of hardware circuits are described in the following paragraphs.

## POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives pin 13C to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 13C, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 13C low for at least 3 $\mu$s. When an external low input is applied to pin 13C, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 13C is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The R2424 POR sequence leaves the modem configured as follows:

- 2400 bps
- Asynchronous
- 10-bit Character Length
- Constant Carrier
- Serial Mode
- Answer Mode
- Auto Answer Disabled
- RAM Access Code = 00

This configuration is suitable for performing high speed data transfer over the public switched telephone network using the serial data port. Individual features are discussed in subsequent paragraphs.

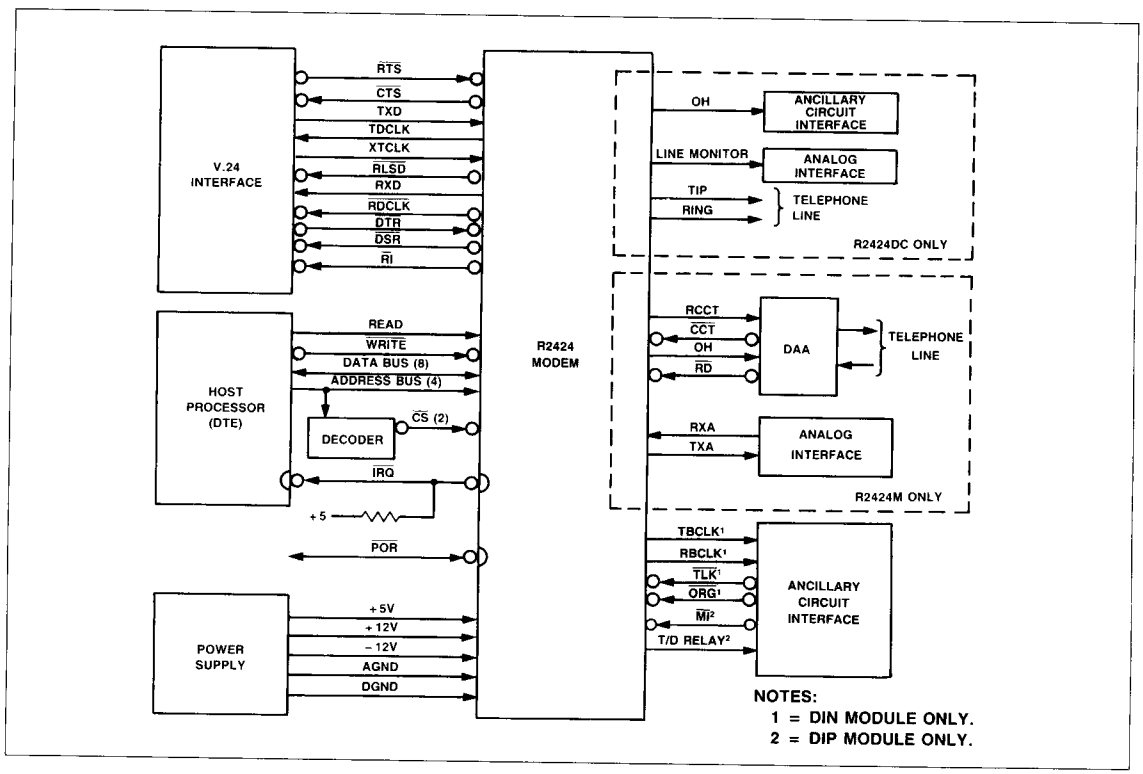



**Figure 1. R2424 Modem Functional Interconnect Diagram**

## Table 4. Hardware Circuits

| Name | Type | DIN Pin No. | DIP Pin No. | Description |
|---|---|---|---|---|
| **A. OVERHEAD SIGNALS** | | | | |
| Ground (A) | AGND | 31C, 32C | 21, 26, 39 | Analog Ground Return |
| Ground (D) | DGND | 3C, 8C, 5A, 10A | 20, 40, 51, 60 | Digital Ground Return |
| +5 volts | PWR | 19C, 23C, 26C, 30C | 1, 19, 61 | +5 volt supply |
| +12 volts | PWR | 15A | 22 | +12 volt supply |
| −12 volts | PWR | 12A | 25 | −12 volt supply |
| $\overline{POR}$ | I/OB | 13C | 13 | Power-on-Reset |
| **B. MICROPROCESSOR INTERFACE SIGNALS** | | | | |
| D7 | I/OA | 1C | 52 | Data Bus (8-Lines) |
| D6 | I/OA | 1A | 53 | |
| D5 | I/OA | 2C | 54 | |
| D4 | I/OA | 2A | 55 | |
| D3 | I/OA | 3A | 56 | |
| D2 | I/OA | 4C | 57 | |
| D1 | I/OA | 4A | 58 | |
| D0 | I/OA | 5C | 59 | |
| RS3 | IA | 6C | 45 | Register Select (4-Lines) |
| RS2 | IA | 6A | 44 | |
| RS1 | IA | 7C | 43 | |
| RS0 | IA | 7A | 42 | |
| $\overline{CS0}$ | IA | 10C | 48 | Chip Select Receiver (Baud Rate Device) |
| $\overline{CS1}$ | IA | 9C | 41 | Chip Select Transmitter (Sample Rate Device) |
| $\overline{READ}$ | IA | 12C | 47 | Read Enable |
| $\overline{WRITE}$ | IA | 11A | 49 | Write Enable |
| $\overline{IRQ}$ | OB | 11C | 50 | Interrupt Request |

| Name | Type | DIN Pin No. | DIP Pin No. | Description |
|---|---|---|---|---|
| **C. V.24 INTERFACE SIGNALS** | | | | |
| XTCLK | IB | 22A | 3 | External Transmit Clock |
| TDCLK | OC | 23A | 7 | Transmit Data Clock |
| $\overline{RDCLK}$ | OC | 21A | 8 | Receive Data Clock |
| $\overline{RTS}$ | IB | 25A | 4 | Request-to-Send |
| $\overline{CTS}$ | OC | 25C | 5 | Clear-to-Send |
| TXD | IB | 24C | 6 | Transmit Data |
| $\overline{RXD}$ | OC | 22C | 9 | Receive Data |
| $\overline{RLSD}$ | OC | 24A | 10 | Received Line Signal Detector |
| $\overline{DTR}$ | IB | 21C | 12 | Data Terminal Ready |
| $\overline{DSR}$ | OC | 20A | 11 | Data Set Ready |
| $\overline{RI}$ | OC | 18A | 2 | Ring Indicator |
| **D. ANALOG SIGNALS** | | | | |
| RXA (M) | IB | 32A | 23 | Receive Analog Input |
| TXA (M) | OC | 31A | 24 | Transmit Analog Output |
| TIP/RING (DC) | AE | RJ11 Jacks | — | Phone Line Interface |
| LINE MONITOR (DC) | AD | 30A | — | Analog Line Monitor |
| **E. DAA INTERFACE SIGNALS** | | | | |
| $\overline{RD}$ (M) | IB | 27A | 35 | Ring Detect |
| RCCT (M) | OC | 28A | — | Request Coupler Cut Through |
| $\overline{CCT}$ (M) | IB | 29C | — | Coupler Cut Through |
| OH | OC | 29A | 36 | Off-Hook Relay Status |
| T/D Relay | OC | — | 37 | Talk/Data Relay |
| $\overline{MI}$ | IC | — | 38 | Manual Input |
| **F. ANCILLARY INTERFACE SIGNALS** | | | | |
| TBCLK | OC | 27C | — | Transmit Baud Clock |
| RBCLK | OC | 26A | — | Receive Baud Clock |
| $\overline{TLK}$ | IC | 28C | — | Talk (TLK = Data) |
| $\overline{ORG}$ | IB | 16C | — | Originate (ORG = Answer) |

(M) R2424M Only, (DC) R2424DC Only, — = not applicable

## Table 5. Digital Interface Characteristics

| Symbol | Parameter | Units | Input/Ouput Type IA | IB | IC | OA | OB | OC | I/O A | I/OB |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input Voltage, High | V | 2.0 min. | 2.0 min. | 2.0 min. | | | | 2.0 min. | 5.25 max. |
| $V_{IL}$ | Input Voltage, Low | V | 0.8 max. | 0.8 max. | 0.8 max. | | | | 0.8 max. | 2.0 min. |
| $V_{OH}$ | Output Voltage, High | V | | | | 2.4 min.[1] | | | 2.4 min.[2] | 0.8 max. |
| $V_{OL}$ | Output Voltage, Low | V | | | | 0.4 max.[2] | 0.4 max.[2] | 0.4 max.[2] | 0.4 max.[2] | 2.4 min.[3] |
| $I_{IN}$ | Input Current, Leakage | μA | ±2.5 max. | | | | | | ±2.5 max.[4] | 0.4 max.[5] |
| $I_{OH}$ | Output Current, High | mA | | | | −0.1 max. | | | | |
| $I_{OL}$ | Output Current, Low | mA | | | | 1.6 max. | 1.6 max. | 1.6 max. | | |
| $I_L$ | Output Current, Leakage | μA | | | | | ±10 max. | | | |
| $I_{PU}$ | Pull-up Current (Short Circuit) | μA | | −240 max. −10 min. | −240 max. −10 min. | | | −240 max. −10 min. | | −260 max. −100 min. |
| $C_L$ | Capacitive Load | pF | 5 | 5 | 20 | | | | 10 | 40 |
| $C_D$ | Capacitive Drive | pF | | | | 100 | 100 | 100 | 100 | 100 |
| | Circuit Type | | TTL | TTL w/Pull-up | TTL w/Pull-up | TTL | Open-Drain | Open-Drain w/Pull-up | 3 State Transceiver | Open-Drain w/Pull-up |

**Notes:** 1. I load = −100 μA 2. I load = 1.6 mA 3. I load = −40 μA 4. $V_{IN}$ = 0.4 to 2.4 Vdc, $V_{CC}$ = 5.25 Vdc 5. I load = 0.36 mA

**Table 6. Analog Interface Characteristics**

| Name | Type | Characteristics |
|---|---|---|
| TXA | AA | The transmitter output impedance is 604Ω ±1% with an output level of +6 dBm. To obtain a 0 dBm output, a 600Ω load to ground is needed. |
| RXA | AB | The receiver input impedance is 23.7 KΩ ±1%. The receive level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled). |
| LINE MONITOR | AD | The line monitor output impedance is 15 KΩ ±5%. |
| TIP/RING | AE | The impedance of TIP with respect to RING is 600 Ω. |

## V.24 INTERFACE

Eleven hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, +5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

### Data Terminal Ready ($\overline{DTR}$)

$\overline{DTR}$ prepares the modem to be connected to the communications channel, and maintains the connection established by the DTE (manual answering) or internal (automatic answering) means. $\overline{DTR}$ OFF places the modem in the disconnect state.

### Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) ON indicates that the modem is in the data transfer state. $\overline{DSR}$ OFF is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except $\overline{RI}$. $\overline{DSR}$ will switch to the OFF state when in test state. The ON condition of $\overline{DSR}$ indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem has generated an answer tone or detected answer tone.
4. After ring indicate ($\overline{RI}$) goes ON, $\overline{DSR}$ waits at least two seconds before turning ON to allow the telephone company equipment to be engaged.

$\overline{DSR}$ will go OFF 50 ms after $\overline{DTR}$ goes OFF, or 50 ms plus a maximum of 4 seconds when the SSD bit is enabled.

### Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. In constant carrier mode, $\overline{RTS}$ can be wired to $\overline{DTR}$. In controlled carrier operation, independent operation of $\overline{RTS}$ turns the carrier ON and OFF. The responses to $\overline{RTS}$ are shown in Table 7 (assume the modem is in data mode).

**Table 7. $\overline{RTS}$ Responses**

| Leased or Dial Line[1] | $\overline{RTS}$ OFF | $\overline{RTS}$ ON |
|---|---|---|
| Controlled Carrier | $\overline{CTS}$ OFF<br>Carrier OFF | Carrier ON<br>210 to 275 ms Scrambled 1s Transmitted<br>$\overline{CTS}$ ON |
| Constant Carrier | $\overline{CTS}$ OFF<br>Carrier ON<br>Scrambled 1s Transmitted | $\overline{CTS}$ ON<br>Carrier ON<br>Data Transmitted |

**Note:**
1. After handshake is complete.

### Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON or OFF condition of $\overline{RTS}$ are shown in Table 8.

**Table 8. $\overline{CTS}$ Response Times**

| $\overline{CTS}$ Transition | Constant Carrier | Controlled Carrier |
|---|---|---|
| OFF to ON | <2 ms | 210 to 275 ms |
| ON to OFF | <20 ms* | <20 ms* |

**Note:** *Programmable

### Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency*. Selected data rate of 2400 Hz, 1200 Hz or 600 Hz (±0.01%).
2. *Duty Cycle*. 50 ±1%.

TDCLK is provided to the user in both asynchronous and synchronous communications. TDCLK is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing (TDCLK is not valid in FSK). TDCLK is necessary for synchronous communication. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

### External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

### Receive Data Clock ($\overline{\text{RDCLK}}$)

The modem provides a Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±.035% (relative) frequency error in the associated transmit timing source.

$\overline{\text{RDCLK}}$ is provided to the user in both asynchronous and synchronous communications. $\overline{\text{RDCLK}}$ is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing ($\overline{\text{RDCLK}}$ is not valid in FSK). $\overline{\text{RDCLK}}$ is necessary for synchronous communication.

### Received Line Signal Detector ($\overline{\text{RLSD}}$)

The $\overline{\text{RLSD}}$ thresholds for both high and low channels are:

$\overline{\text{RLSD}}$ ON $\geq$ −43 dBm
$\overline{\text{RLSD}}$ OFF $\leq$ −48 dBm

$\overline{\text{RLSD}}$ will not respond to guard tones or answer tones.

When $\overline{\text{RLSD}}$ is active, it indicates to the terminal equipment that valid data is available on RXD.

### Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

### Received Data (RXD)

The modem presents received data to the local DTE on this output.

### Ring Indicator ($\overline{\text{RI}}$)

The modem provides a Ring Indicator ($\overline{\text{RI}}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the ON segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The high condition of the $\overline{\text{RI}}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received. The operation of $\overline{\text{RI}}$ is not disabled by an OFF condition on $\overline{\text{DTR}}$.

$\overline{\text{RI}}$ will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across TIP and RING), with the response times given in Table 13.

This OFF-to-ON (ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent ON (OFF) transition of $\overline{\text{RI}}$.

**Table 9. $\overline{\text{RI}}$ Response Time**

| $\overline{\text{RI}}$ Transition | Response Time |
|---|---|
| OFF-to-ON* | 110 ±50 ms (50% duty cycle) |
| ON-to-OFF | 450 ±50 ms |
| **Note:** *The OFF-to-ON time is duty cycle dependent: 890 ms (15%) ≥ time ≥ 50 ms (100%) | |

## MICROPROCESSOR INTERFACE

Seventeen hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

### Chip Select ($\overline{CS0}$ and $\overline{CS1}$) and Register Selects (RS0-RS1)

The signal processor to be accessed is selected by grounding one of two unique chip select lines, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit ($2^3$) is RS3 while the least significant address bit ($2^0$) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit ($2^7$) is D7 while the least significant data bit ($2^0$) is D0.

### Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ line high or the $\overline{WRITE}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

### Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to + 5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

## DAA INTERFACE

The R2424M provides a Data Access Arrangement (DAA) interface that is directly hardware and software compatible with the RDAA. Manual/automatic originate and answer are then controlled via the appropriate R2424M hardware ancillary circuits or software control bits. The modem provides the only interface with the microprocessor (MPU) bus, i.e., no RDAA interface signals must be directly controlled from the MPU bus.

### Ring Detect ($\overline{RD}$)

$\overline{RD}$ indicates to the modem by an ON (low) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the $\overline{RD}$ input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40 Vrms, 15 to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on $\overline{RI}$.

### Request Coupler Cut Through (RCCT)

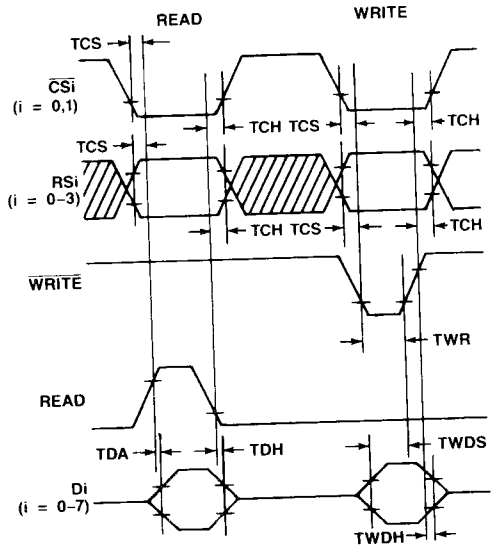
RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When RCCT goes OFF (low), the cut-through buffers are disabled and $\overline{CCT}$ should go OFF (high). RCCT should be OFF during dialing but ON for tone address signaling.

### Coupler Cut Through ($\overline{CCT}$)

An ON (low) signal to the $\overline{CCT}$ lead indicates to the modem that the data transmission path through the DAA is connected. This input can always be grounded if the two second billing delay squelch is desired. If $\overline{CCT}$ is user controlled, the billing delay squelch can only be 2 seconds or greater.

### Off-Hook Relay Status (OH)

The modem provides an OH output which indicates the state of the OH relay. A high condition on OH implies the OH relay is closed and the modem is connected to the telephone line (off-hook). A low condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.




| Characteristic | Symbol | Min | Max | Units |
|---|---|---|---|---|
| $\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$ | TCS | 30 | — | ns |
| Data access time after Read | TDA | — | 140 | ns |
| Data hold time after Read | TDH | 10 | 50 | ns |
| $\overline{CSi}$, RSi hold time after Read or $\overline{Write}$ | TCH | 10 | — | ns |
| Write data setup time | TWDS | 75 | — | ns |
| Write data hold time | TWDH | 10 | — | ns |
| Write strobe pulse width | TWR | 75 | — | ns |

**Figure 2. Microprocessor Interface Timing Diagram**

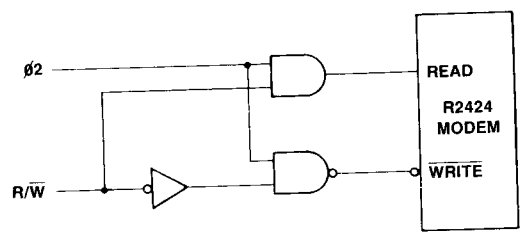



**Figure 3. R/$\overline{W}$ to READ $\overline{WRITE}$ Conversion Logic**

### ANALOG SIGNALS (R2424M)

Two connections are devoted to analog audio signals: TXA and RXA.

### Transmit Analog (TXA)

The TXA output is suitable for driving a data access arrangement for connection to either leased lines or the public switched telephone network. The transmitter output impedance is 604 ohms ±1% with an output level of +6 dBm ±1 dBm. To obtain a 0 dBm output, a 600 ohm load to ground is needed.

### Receive Analog (RXA)

RXA is an input to the receiver from a data access arrangement. The input impedance is 23.7K ohms ±1%. The received level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled).

### ANALOG SIGNALS (R2424DC)

Three analog signals are output by the R2424DC: LINE MONITOR, TIP and RING.

### Analog Line Monitor (LINE MONITOR)

The LINE MONITOR output is suitable for a speaker interface. It provides an output for all dialing signals, call progress signals, and the carrier signals. The output impedance is 15K ohms ±1%. The signals which appear on LINE MONITOR are approximately the same level as the signals would appear on the network (assuming a 1 dB loss attributed to the audio transformer).

### Phone Line Interface (TIP and RING)

TIP and RING are the DAA analog outputs to the public switched telephone network. These outputs use two RJ11 jacks in parallel as the interface to the network (see Table 10 and Figure 4). The R2424DC, which contains the DAA TIP and RING interface, has been FCC Part 68 approved. The user need not apply for further Part 68 approval. The impedance of TIP with respect to RING is 600 ohms.

**Table 10. R2424DC Network Interface**

| Connector Type | Pin Number | Name | Function |
|---|---|---|---|
| RJ11 Jack | 3 | RING | One Side of TELCO Line |
| | 4 | TIP | One Side of TELCO Line |

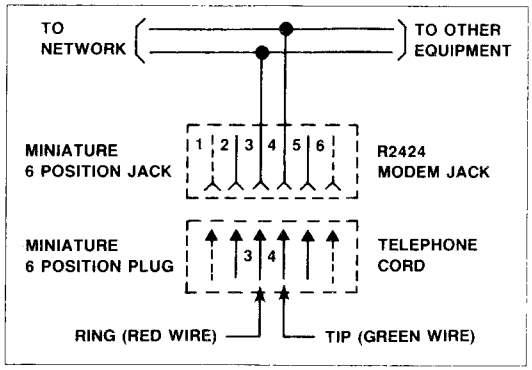



**Figure 4. RJ11 Telephone Jack**

## ANCILLARY CIRCUITS

### Transmit Baud Clock (TBCLK) and Received Baud Clock (RBCLK)

TBCLK and RBCLK are provided to the user at the baud rate (600 Hz).

### Talk ($\overline{TLK}$) (DIN Module Only)

$\overline{TLK}$ is an input which manually places the modem on-hook (relay open, $\overline{TLK}$ = 0) or off-hook (relay closed, $\overline{TLK}$ = 1). The on-hook condition is referred to as TALK mode and the off-hook condition is referred to as DATA mode. $\overline{TLK}$ is used with $\overline{ORG}$ to manually originate or answer a call. $\overline{TLK}$ should be 0 at power-on or reset to prevent the modem from inadvertently entering the data mode.

### Originate ($\overline{ORG}$)

$\overline{ORG}$ is an input which manually places the modem in the originate mode ($\overline{ORG}$ = 0) or the answer mode ($\overline{ORG}$ = 1). To manually originate a call, $\overline{ORG}$ = 0 and $\overline{TLK}$ = 0. Dial the number using the telephone. When the other modem answers and sends answer tone switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook.

To manually answer a call $\overline{ORG}$ = 1 and $\overline{TLK}$ = 0. When the phone rings switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook.

### Off-Hook Relay Status (OH)

The modem provides an OH output which indicates the state of the OH relay. A high condition on OH implies the OH relay is closed and the modem is connected to the telephone line (off-hook). A low condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

### T/D Relay. (DIP Module Only)

The T/D Relay signal may be used as a second relay control when the parallel control mode of operation is selected (BUS bits 0 and 1 = 1). If the serial control mode is selected (BUS bits 0 and 1 = 0) the T/D relay follows the status of the OH output signal which is controlled by the $\overline{MI}$ signal. In the parallel control mode the OH output signal is controlled by the status of the DATA bit, while independent control of the T/D relay is provided by the $\overline{MI}$ signal. During pulse dialing the OH signal reflects the pulse signals being dialed. It is therefore possible to use the T/D Relay signal to control the off-hook relay and use the OH signal to perform pulse dialing on a separate, independent relay.

### Manual Input ($\overline{MI}$) (DIP Module Only)

$\overline{MI}$ is an input which manually places the modem on-hook (relay open, $\overline{MI}$ = 0) or off-hook (relay closed, $\overline{MI}$ = 1). The on-hook condition is referred to as TALK mode and the off-hook condition is referred to as DATA mode. $\overline{MI}$ is used with $\overline{ORG}$ to manually originate or answer a call. $\overline{MI}$ should be 0 at power-on or reset to prevent the modem from inadvertently entering the data mode.

## SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load-/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on two special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into two areas. These areas are partitioned into receiver and transmitter devices.

### INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 32 addressable registers in the modem receiver (CS0) and transmitter (CS1) interface memory are shown in Figures 5 and 6, respectively. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Figures 7 and 8 show the registers according to the overall function they perform in the receiver and transmitter, respectively. Figures 9 through 12 show the power on configurations of the interface memory bits for the R2424/US and the R2424/INT versions.

Table 11 defines the individual bits in the interface memory. In the Table 11 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| F | RAM Access R | | | | | | | |
| E | IRQ | ENSI | NEWS | — | NEWC | — | — | — |
| D | BUS | CRQ | — | — | — | LCD | RSD | — |
| C | — | — | — | CHAR | | — | — | — |
| B | — | — | — | — | — | — | — | AL |
| A | ERDL | RDL | DL | ST | MODE | | | |
| 9 | — | — | SPEED | | — | — | — | — |
| 8 | TONE | ATD | — | — | — | — | TM | RLSD |
| 7 | — | — | — | — | — | — | — | — |
| 6 | — | — | — | — | — | — | — | — |
| 5 | RAM Data YRM (YRAMRM) | | | | | | | |
| 4 | RAM Data YRL (YRAMRL) | | | | | | | |
| 3 | RAM Data XRM (XRAMRM) | | | | | | | |
| 2 | RAM Data XRL (XRAMRL) | | | | | | | |
| 1 | — | — | — | — | — | — | — | — |
| 0 | — | — | — | — | — | — | — | — |

Note
(—) Indicates reserved for modem use only.

Figure 5. Receiver ($\overline{CS0}$) Interface Memory Map

| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| F | RAM Access T | | | | | | | |
| E | IRQ | ENSI | NEWS | — | NEWC | DDEI | — | DDRE |
| D | BUS | CRQ | DATA | AAE | DTR | — | — | SSD |
| C | DSRA | TXCLK | | CHAR | | — | — | DLSF[1] |
| B | TX LEVEL | | | GTE | GTS | 3DB | DTMF | AL |
| A | ERDL | RDL | DL | ST | MODE | | | |
| 9 | NAT[1] | RTRN | ORG | LL | RTS | CC | EF | NTS |
| 8 | DLO | CTS | DSR | RI | — | — | — | — |
| 7 | — | — | — | — | — | — | — | — |
| 6 | — | — | — | — | — | — | — | — |
| 5 | RAM Data YTM (YRAMTM) | | | | | | | |
| 4 | RAM Data YTL (YRAMTL) | | | | | | | |
| 3 | RAM Data XTM (XRAMTM) | | | | | | | |
| 2 | RAM Data XTL (XRAMTL) | | | | | | | |
| 1 | — | — | — | — | — | — | — | — |
| 0 | Dial Digit Register | | | | | | | |

Notes
1. Not valid before R5310-22
(—) Indicates reserved for modem use only.

Figure 6. Transmitter ($\overline{CS1}$) Interface Memory Map

| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| F | DIAGNOSTIC CONTROL | | | | | | | |
| E | HANDSHAKE | | | | | | | |
| D | CONFIGURATION | | | | | | | |
| C | CONFIGURATION | | | | | | | |
| B | CONFIGURATION | | | | | | | |
| A | CONFIGURATION | | | | | | | |
| 9 | STATUS | | | | | | | |
| 8 | STATUS | | | | | | | |
| 7 | RESERVED | | | | | | | |
| 6 | RESERVED | | | | | | | |
| 5 | DIAGNOSTIC | | | | | | | |
| 4 | DIAGNOSTIC | | | | | | | |
| 3 | DIAGNOSTIC | | | | | | | |
| 2 | DIAGNOSTIC | | | | | | | |
| 1 | RESERVED | | | | | | | |
| 0 | RESERVED | | | | | | | |
| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Figure 7. Receiver ($\overline{CS0}$) Interface Memory Functions

| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| F | DIAGNOSTIC CONTROL | | | | | | | |
| E | HANDSHAKE | | | | | | | |
| D | CONFIGURATION | | | | | | | |
| C | CONFIGURATION | | | | | | | |
| B | CONFIGURATION | | | | | | | |
| A | CONFIGURATION | | | | | | | |
| 9 | CONFIGURATION | | | | | | | |
| 8 | STATUS | | | | | | | |
| 7 | RESERVED | | | | | | | |
| 6 | RESERVED | | | | | | | |
| 5 | DIAGNOSTIC | | | | | | | |
| 4 | DIAGNOSTIC | | | | | | | |
| 3 | DIAGNOSTIC | | | | | | | |
| 2 | DIAGNOSTIC | | | | | | | |
| 1 | RESERVED | | | | | | | |
| 0 | DIAL DIGIT REGISTER | | | | | | | |
| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Figure 8. Transmitter ($\overline{CS1}$) Interface Memory Functions

| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| F | RAM Access R 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E | IRQ 0 | ENSI 0 | NEWS 0 | — | NEWC 0 | — | — | — |
| D | BUS 0 | CRQ 0 | — | — | — | LCD 1 | RSD 0 | — |
| C | — | — | — | CHAR 1 | 0 | — | — | — |
| B | — | — | — | — | — | — | — | AL 0 |
| A | ERDL 0 | RDL 0 | DL 0 | ST 0 | 0 | MODE 0 | 0 | 1 |
| 9 | — | — | SPEED 0 | 0 | — | — | — | — |
| 8 | TONE 0 | ATD 0 | — | — | — | — | TM 0 | RLSD 0 |
| 7 | — | — | — | — | — | — | — | — |
| 6 | — | — | — | — | — | — | — | — |
| 5 | RAM Data YRM (Random) | | | | | | | |
| 4 | RAM Data YRL (Random) | | | | | | | |
| 3 | RAM Data XRM (Random) | | | | | | | |
| 2 | RAM Data XRL (Random) | | | | | | | |
| 1 | — | — | — | — | — | — | — | — |
| 0 | — | — | — | — | — | — | — | — |
| Register / Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

(—) Indicates reserved for modem use only.

**Figure 9. R2424/US Receiver ($\overline{CS0}$) Interface Memory Power On Configuration**

| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| F | RAM Access T 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E | IRQ 0 | ENSI 0 | NEWS 0 | — | NEWC 0 | DDEI 0 | — | DDRE 0 |
| D | BUS 0 | CRQ 0 | DATA 0 | AAE 0 | DTR 0 | — | — | SSD 0 |
| C | DSRA 0 | TX CLK 0 | 0 | CHAR 1 | 0 | — | — | DLSF 0 |
| B | TX LEVEL 0 | 0 | 0 | GTE 0 | GTS 0 | 3DB 0 | DTMF 0 | AL 0 |
| A | ERDL 0 | RDL 0 | DL 0 | ST 0 | 1 | MODE 1 | 0 | 1 |
| 9 | NAT 0 | RTRN 0 | ORG 0 | LL 0 | RTS 0 | CC 0 | EF 0 | NTS 0 |
| 8 | DLO 0 | CTS 0 | DSR 0 | RI 0 | — | — | — | — |
| 7 | — | — | — | — | — | — | — | — |
| 6 | — | — | — | — | — | — | — | — |
| 5 | RAM Data YTM (Random) | | | | | | | |
| 4 | RAM Data YTL (Random) | | | | | | | |
| 3 | RAM Data XTM (Random) | | | | | | | |
| 2 | RAM Data XTL (Random) | | | | | | | |
| 1 | — | — | — | — | — | — | — | — |
| 0 | Dial Digit Register (Write-Only Register) | | | | | | | |
| Register / Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

(—) Indicates reserved for modem use only.

**Figure 10. R2424/US Transmitter ($\overline{CS1}$) Interface Memory Power On Configuration**

| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| F | RAM Access R 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E | IRQ 0 | ENSI 0 | NEWS 0 | — | NEWC 0 | — | — | — |
| D | BUS 0 | CRQ 0 | — | — | — | LCD 1 | RSD 0 | — |
| C | — | — | — | CHAR 1 | 0 | — | — | — |
| B | — | — | — | — | — | — | — | AL 0 |
| A | ERDL 0 | RDL 0 | DL 0 | ST 0 | 1 | MODE 1 | 0 | 1 |
| 9 | — | — | SPEED 0 | 0 | — | — | — | — |
| 8 | TONE 0 | ATD 0 | — | — | — | — | TM 0 | RLSD 0 |
| 7 | — | — | — | — | — | — | — | — |
| 6 | — | — | — | — | — | — | — | — |
| 5 | RAM Data YRM (Random) | | | | | | | |
| 4 | RAM Data YRL (Random) | | | | | | | |
| 3 | RAM Data XRM (Random) | | | | | | | |
| 2 | RAM Data XRL (Random) | | | | | | | |
| 1 | — | — | — | — | — | — | — | — |
| 0 | — | — | — | — | — | — | — | — |
| Register / Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

(—) Indicates reserved for modem use only.

**Figure 11. R2424/INT Receiver ($\overline{CS0}$) Interface Memory Power On Configuration**

| Register \ Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| F | RAM Access T 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E | IRQ 0 | ENSI 0 | NEWS 0 | — | NEWC 0 | DDEI 0 | — | DDRE 0 |
| D | BUS 0 | CRQ 0 | DATA 0 | AAE 0 | DTR 0 | — | — | SSD 0 |
| C | DSRA 0 | TX CLK 0 | 0 | CHAR 1 | 0 | — | — | DLSF 0 |
| B | TX LEVEL 0 | 0 | 0 | GTE 0 | GTS 0 | 3DB 0 | DTMF 0 | AL 0 |
| A | ERDL 0 | RDL 0 | DL 0 | ST 0 | 1 | MODE 1 | 0 | 1 |
| 9 | NAT 0 | RTRN 0 | ORG 0 | LL 0 | RTS 0 | CC 0 | EF 0 | NTS 0 |
| 8 | DLO 0 | CTS 0 | DSR 0 | RI 0 | — | — | — | — |
| 7 | — | — | — | — | — | — | — | — |
| 6 | — | — | — | — | — | — | — | — |
| 5 | RAM Data YTM (Random) | | | | | | | |
| 4 | RAM Data YTL (Random) | | | | | | | |
| 3 | RAM Data XTM (Random) | | | | | | | |
| 2 | RAM Data XTL (Random) | | | | | | | |
| 1 | — | — | — | — | — | — | — | — |
| 0 | Dial Digit Register (Write-Only Register) | | | | | | | |
| Register / Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

(—) Indicates reserved for modem use only.

**Figure 12. R2424/INT Transmitter ($\overline{CS1}$) Interface Memory Power On Configuration**

**Table 11. Interface Memory Definitions**

| Mnemonic | Name | Memory Location | Description |
|---|---|---|---|
| AAE | Auto Answer Enable | 1:D:4 | When configuration bit AAE is a 1, the modem will automatically answer when a ringing signal is present on the line. When AAE is set to a 1, the modem will answer after one ring and go into data mode.<br><br>The modem goes off-hook 1 second after the on-to-off transition of the ring. The $\overline{ORG}$ pin or ORG bit need not to be set to the answer polarity. If it is desired to answer after more than one ring, then the user must use the alternative answer method described under the DATA bit. The $\overline{DTR}$ pin or the DTR bit must also be set before the modem will auto answer. Writing a 0 into the AAE bit will cause the modem to go on-hook. This will occur only when the modem auto answers using the AAE bit. |
| AL | Analog Loopback | (0,1):B:0 | When configuration bits AL are a 1, the modem is in local analog loopback (V.54 Loop 3). In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is attenuated 14 ±1 dBm. The modem may be placed into analog loopback in either the idle mode or the data mode. However, in the data mode, setting the AL bits to a 1 will terminate the connection. Analog loopback will only function in the high speed modes (2400, 1200, or 600 bps).<br><br>The DTE may be tested when the modem is in analog loopback. Also, all parts of the modem except the line interface are checked. If no DTE is connected, the modem integrity may be verified by use of the self test function. When entering analog loopback, set AL in the receiver to a 1 before setting AL in the transmitter to a 1.<br><br>When exiting analog loopback, reset AL in the transmitter to a 0 before resetting AL in the receiver to a 0. |
| ATD | Answer Tone Detected | 0:8:6 | When status bit ATD is a 1, it signifies that the modem receiver detected the answer tone. The bit is 1 set 75 ms after the answer tone is first detected, and is cleared to a 0 when the modem goes on-hook. The user may clear ATD manually after CTS is active. |
| BUS | Bus Select | (0,1):D:7 | When configuration bits BUS are a 1, the modem is in the parallel control mode; and when 0, the modem is in the serial control mode. BUS can be in either state to configure the modem.<br><br>*Serial Control Mode*<br><br>The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. The control signals used in serial control mode are $\overline{DTR}$, $\overline{RTS}$, $\overline{TLK}$, and $\overline{ORG}$. Outputs such as $\overline{RLSD}$ and $\overline{DSR}$ are reflected both in the interface memory and the V.24 interface. Once the bus bits have been set to a 0, the state of the DTR, RTS, DATA, and ORG bits are ignored.<br><br>*Parallel Control Mode*<br><br>The modem has the capability of modem control via the microprocessor bus. Data transfer is maintained over the serial V.24 channel. The control bits used in parallel control are DTR, RTS, ORG, and DATA.<br><br>The modem automatically defaults to the serial mode at power-on.<br><br>If the parallel control mode is to be used, it is recommended that the $\overline{TLK}$ pin be tied to ground. A floating $\overline{TLK}$ pin will assume a logic 1 which will immediately put the modem into the data mode before the BUS bits are set.<br><br>In either mode, the modem is configured by the host processor via the microprocessor bus. |

**Table 11. Interface Memory Definitions (Continued)**

| Mnemonic | Name | Memory Location | Description |
|---|---|---|---|
| CC | Controlled Carrier | 1:9:2 | When configuration bit CC is a 1, the modem operates in controlled carrier; when 0, the modem operates in constant carrier.<br>Controlled carrier allows the modem transmitter to be controlled by the $\overline{RTS}$ pin or the RTS bit. Its effect may be seen in the RTS and CTS descriptions. |
| CHAR | Character Length Select | (0,1):C:(3,4) | These character length bits select either 8, 9, 10, or 11 bit characters (includes data, stop, and start bits) as shown below:<br>**Configuration Word** 4 3 — **Configuration**<br>0 0 — 8 bits<br>0 1 — 9 bits<br>1 0 — 10 bits<br>1 1 — 11 bits<br>It is possible to change character length during the data mode. Errors in the data will be expected between the changeover and the resynchronization (which occurs on the next start bit after the change is implemented). |
| CRQ | Call Request | (0,1):D:6 | When configuration bit CRQ in chip 1 (the transmitter) is a 1, it places the transmitter in auto dial mode. The data then placed in the Dial Digit Register is treated as digits to be dialed. The format for the data should be a hex representation of the number to be dialed (if a 9 is to be dialed then an $09_{16}$ should be loaded in DDR). CRQ in chip 1 should be a 1 for the duration of the data mode. If CRQ in chip 1 is changed to a 0, the modem will go on-hook. Also, see DDRE bit.<br>When configuration bit CRQ in chip 0 (the receiver) is a 1, the receiver goes into tone detect mode. Any energy above threshold and in the 345 to 635 Hz bandwidth is reflected by the TONE bit. CRQ in chip 0 must be reset to a 0 (after the last digit was dialed and tone detection completed) before the answer tone is sent by the answering modem (after ringback is detected). CRQ in chip 0 need not be used during auto dialing, but may be used to provide call progress information as part of an intelligent auto dialing routine. An example flowchart is given in Figure 13.<br>FF (hex) should be loaded into the Dial Digit Register after the last digit is dialed and tone detection is completed. This action also puts the modem in data mode and starts a 30 second abort timer. If the handshake has not been completed in 30 seconds the modem will go on-hook. |
| CTS | Clear-to-Send | 1:8:6 | When status bit CTS is a 1, it indicates to the terminal equipment that the modem will transmit any data which are present at TXD.<br>CTS response times from an ON or OFF condition of RTS are shown below:<br>**CTS Transition** — **Constant Carrier** — **Controlled Carrier**<br>OFF to ON — ≤2 ms — 210 to 275 ms<br>ON to OFF — ≤20 ms* — ≤20 ms*<br>*Programmable |
| DATA | Talk/Data | 1:D:5 | When control bit DATA is a 1, the modem is in the data state (off-hook); and when 0, the modem is in the talk state (on-hook). This bit allows the modem to go off-hook after a programmable number of rings by counting the required number of RI bit transitions and then setting the DATA bit (assuming ORG = 0). |
| DDEI | Dial Digit Empty Interrupt | 1:E:2 | When handshake bit DDEI is a 1, an interrupt will occur when the Dial Digit Register (1:0) is empty (DDRE = 1). This is independent of the state of the ENSI bit. The interrupt will set the IRQ bit and also assert the $\overline{IRQ}$ signal. Loading the Dial Digit Register with a new digit will clear the interrupt condition. |

**Table 11. Interface Memory Definitions (Continued)**

| Mnemonic | Name | Memory Location | Description |
|---|---|---|---|
| DDR | Dial Digit Register | 1:0:(0–7) | DDR is used to load the digits to be dialed. Example: If a 4 is to be dialed, an 04 (hex) should be loaded. This action also causes the interrupt to be cleared. The modem automatically accounts for the interdigit delay. Note: DDR is a write-only register. |
| DDRE | Dial Digit Register Empty | 1:E:0 | When handshake bit DDRE is a 1, it indicates that the dial digit register is empty and can be loaded with a new digit to be dialed. If the DDEI bit is set, the IRQ bit will be set when the DDRE bit is set. Also, the $\overline{IRQ}$ signal will be generated.<br><br>After the DDR is loaded, DDRE goes to a 0 and the interrupts are automatically cleared. |
| DL | Digital Loopback (Manual) | (0,1):A:5 | When configuration bits DL are set to a 1, the modem is manually placed in digital loopback. DL should only be set during the data mode. The DSR and CTS bits will be reset to a 0. The local modem can then be tested from the remote modem end by looping a remotely generated test pattern. At the remote modem, all interface circuits behave normally as in the data mode.<br><br>At the conclusion of the test, DL must be reset to a 0. The local modem will then return to the normal data mode with control reverting to the DTEs, DTR.<br><br>DL does not function in 300 bps. |
| DLO | Dial Line Occupied | 1:8:7 | When status bit DLO is a 1, it indicates that the modem is in the auto dial state, i.e., CRQ in the transmitter is a 1 and the modem is off-hook and ready to dial. |
| DLSF | Disable Low Speed Fallback | 1:C:0 | When configuration bit DLSF is a 1, the modem will not automatically fallback to the 300 bps operating mode if it is configured for another data rate. This bit is valid in originate mode only. |
| DSR | Data Set Ready | 1:8:5 | The ON condition of the status bit DSR indicates that the modem is in the data transfer state. The OFF condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits — except RI. DSR will switch to the OFF state when in test state. The ON condition of DSR indicates the following:<br><br>The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.<br><br>The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.<br><br>The modem has generated an answer tone or detected answer tone.<br><br>After ring indicate goes ON, DSR waits at least two seconds before turning ON to allow the telephone company equipment to be engaged.<br><br>DSR will go OFF 50 msec after DTR goes OFF, or 50 msec plus a maximum of 4 sec when the SSD bit is enabled. |
| DSRA | Data Set Ready in Analog Loopback | 1:C:7 | When configuration bit DSRA is a 1, it causes DSR to be ON during analog loopback. |

**Table 11. Interface Memory Definitions (Continued)**

| Mnemonic | Name | Memory Location | Description |
|---|---|---|---|
| DTMF | Touch Tones/Pulse Dialing | 1:B:1 | When configuration bit DTMF is a 1, it tells the modem to auto dial using tones; and when 0, the modem will dial using pulses.<br><br>The timing for the pulses and tones are as follows (power-on timing):<br><br>Pulses — Relay open 64 ms<br>Relay closed 36 ms<br>Interdigit delay 750 ms<br><br>Tones — Tone duration 95 ms<br>Interdigit delay 70 ms<br><br>The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. The output power level of the DTMF tones is as follows:<br><br>±15 dBm ±1 measured at TXA for the R2424M<br>−1 dBm ±1 measured at TIP/RING for the R2424DC |
| DTR | Data Terminal Ready | 1:D:3 | Control bit DTR must be a 1 for the modem to enter the data state, either manually or automatically. DTR must also be a 1 in order for the modem to automatically answer an incoming call.<br><br>During the data mode, DTR must remain at a 1, otherwise the connection will be terminated if DTR resets to a 0 for greater than 50 ms. |
| EF | Enable Filters | 1:9:1 | Setting CRQ in the transmitter to a 1 disables the high and low band filters used in data mode so that call progress tone detection can be done. Setting CRQ in the receiver to a 1 inserts a passband filter in the receive path which passes energy in the 345 Hz to 635 Hz bandwidth. The high and low band filters must be enabled and the passband filter disabled for the answer tone and carrier to be detected. This occurs automatically during the auto dial process when EF is set to a 0. In this case, the high and low band filters are disabled when CRQ in the transmitter is set to a 1. If tone detection is required, CRQ in the receiver should be set to a 1. After dialing and call progress tone detection, CRQ in the receiver is set to a 0 and FF is loaded into the dial digit register. (Loading FF enables the high and low band filters). At this time, the answer tone can be detected. To re-enable the high and low band filters disabled by setting CRQ in the transmitter, set EF to a 1. After CRQ in the transmitter and receiver is set to a 1 and tone detection is completed, it may be necessary to detect the answer tone before loading FF into the dial digit register (see the section on sending 1300 Hz calling tone). At that point, EF can be set to a 1 and CRQ in the receiver set to a 0 so the answer tone can be detected (using the ATD bit) and the 1300 Hz calling tone can still be sent. Once the answer tone is detected, FF should be loaded into the dial digit register and the EF bit set to a 0. |
| ENSI | Enable New Status Interrupt | (0,1):E:6 | When handshake bit ENSI is a 1, it causes an interrupt to occur when the status bits in registers (0:[8,9]) and (1:8) are changed by the modem. (NEWS = 1). The IRQ bit will be set to a 1 and the $\overline{IRQ}$ signal will be generated. The interrupt is cleared by writing a 0 into the NEWS bit. |
| ERDL | Enable Response to Remote Digital Loopback | (0,1):A:7 | When configuration bits ERDL are a 1, it enables the modem to respond to another modem's remote digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS, DSR and RLSD bits to a 0 and turns the $\overline{CTS}$, $\overline{DSR}$ and $\overline{RLSD}$ signals to a logic 1. The TM bit is set to inform the user of the test status. When the ERDL bits are a 0, no response will be generated. |
| GTE | Guard Tone Enable | 1:B:4 | When configuration bit GTE is a 1, it causes the specified guard tone to be transmitted (CCITT configurations only), according the state of the GTS bit. Note: The guard tone will only be transmitted by the answering modem. |

**Table 11. Interface Memory Definitions (Continued)**

| Mnemonic | Name | Memory Location | Description |
|---|---|---|---|
| GTS | Guard Tone Select | 1:B:3 | When configuration bit GTS is a 0, it selects the 1800 Hz tone; when GTE is a 1 it selects the 550 Hz tone. The selected guard tone will be transmitted only when GTE is enabled. |
| IRQ | Interrupt | (0,1):E:7 | When status bit IRQ is a 1, it indicates that an interrupt has been generated. The $\overline{IRQ}$ hardware signal is generated following the setting of the IRQ bit. $\overline{IRQ}$ is cleared when either the NEWS bit is reset to a 0 or the DDR is loaded with a number. |
| LCD | Loss of Carrier Disconnect | 0:D:2 | When configuration bit LCD is a 1, the modem terminates a call when a loss of received carrier energy is detected after 400 ms. After the first 40 ms of loss of carrier, RLSD goes off. 360 ms later, if no carrier is detected, CTS goes off, and the modem goes on-hook. If energy above threshold is detected during the 360 ms period, RLSD will be set to a 1 again. If further loss of energy occurs, the 400 ms time frame is restarted.<br><br>If LCD is set to a 0, RLSD will be set to a 1 when energy is above threshold, but will not force the modem on-hook when energy falls below threshold. In this case, it is necessary to re-enable LCD in order to put the modem on-hook.<br><br>LCD is not automatically disabled in leased line operation. The user must write a 0 into LCD bits for this to occur. |
| LL | Leased Line | 1:9:4 | When configuration bit LL is a 1, the modem is in leased line operation; when 0, the modem is in switched line operation. When LL is set to a 1, the modem immediately goes off-hook and into data mode. |
| MODE | Mode Select | (0,1):A:(0,3) | These bits select the compatibility at which the modem is to operate, as shown below:<br><br>**Configuration Word**<br>**3 2 1 0** — **Configuration**<br>0 0 0 0 — Bell 2400 — 2400 Sync.<br>0 0 0 1 — Bell 2400 — 2400 Async.<br>0 0 1 0 — Bell 212A — 1200 Sync.<br>0 0 1 1 — Bell 212A — 1200 Async.<br>0 1 0 0 — Bell 212A — 0 to 300 Async.<br>1 0 0 0 — V.22A — 1200 Sync.<br>1 0 0 1 — V.22B — 1200 Async.<br>1 0 1 0 — V.22A — 600 Sync.<br>1 0 1 1 — V.22B — 600 Async.<br>1 1 0 0 — V.22 bis — 2400 Sync.<br>1 1 0 1 — V.22 bis — 2400 Async.<br>1 1 1 0 — V.22 bis — 1200 Sync.<br>1 1 1 1 — V.22 bis — 1200 Async.<br><br>NOTE: The Mode bits in both chips should be set exclusively of all other bits, followed immediately by the setting of the NEWC bits. This will ensure proper modem configuration.<br><br>*Automatic Reconfiguration*<br><br>The modem is capable of automatically falling back during the handshake to the compatibility of a remote modem. The modem can be in either the answer or originate mode for this to occur. The compatibilities that the modem are limited to adapt to are V.22 bis, V.22 A/B (1200 bps), Bell 212 and Bell 103. If the R2424 is to originate in a specific configuration, the MODE bits must be set.<br><br>When the answer modem is configured for Bell 300 asynchronous and is called by a 1200 bps modem, the handshake will be completed at 1200 bps. |
| NAT | No Answer Tone | 1:9:7 | When configuration bit NAT is a 1, the modem will not transmit the 2100 Hz CCITT answer tone. This bit is only valid for CCITT configurations. With this bit enabled in answer mode, when the modem goes off-hook it will remain silent for 75 ms and then transmit unscrambled ones. |

**Table 11. Interface Memory Definitions (Continued)**

| Mnemonic | Name | Memory Location | Description |
|---|---|---|---|
| NEWC | New Configuration | (0,1):E:3 | When the NEWC bit is a 1, it tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC to a 0. NEWC must be set to a 1 after a new configuration has been written into the following registers: (0:[A–D]) and (1:[9–D]). The remaining registers do not require the use of NEWC to tell the modem that new data was written into them. |
| NEWS | New Status | (0,1):E:5 | When handshake bit NEWS is a 1, it tells the user that there has been a change of status in the status registers. The user must write a 0 into NEWS to reset it. This action also causes the interrupt to be cleared. |
| NTS | No Transmitter Scrambler | 1:9:0 | When configuration bit NTS is a 1, when the modem is off-hook it will transmit all data in an unscrambled form. This bit should be disabled if the normal modem handshake is desired. |
| ORG | Originate/Answer | 1:9:5 | When configuration bit ORG is a 1, the modem is in originate mode; and when a 0 the modem is in answer mode. (This is only valid in manual originate/answer and analog loopback). If ORG is a 1 in analog loopback, the modem will transmit in the high band and receive in the low band. If ORG is a 0 in analog loopback, the modem will transmit in the low band and receive in the high band. |
| (None) | RAM Access R | 0:F:0–7 | Contains the RAM access code used in reading RAM locations in chip 0 (receiver device). |
| (None) | RAM Access T | 1:F:0–7 | Contains the RAM access code used in reading RAM locations in chip 1 (transmitter device). |
| XRAMRL | RAM Data XRL | 0:2:0–7 | Least significant byte of 16-bit word X used in reading RAM locations in chip 0. |
| XRAMRM | RAM Data XRM | 0:3:0–7 | Most significant byte of 16-bit word X used in reading RAM locations in chip 0. |
| XRAMTL | RAM Data XTL | 1:2:0–7 | Least significant byte of 16-bit word X used in reading RAM locations in chip 1. |
| XRAMTM | RAM Data XTM | 1:3:0–7 | Most significant byte of 16-bit word X used in reading RAM locations in chip 1. |
| YRAMRL | RAM Data YRL | 0:4:0–7 | Least significant byte of 16-bit word Y used in reading RAM locations in chip 0. |
| YRAMRM | RAM Data YRM | 0:5:0–7 | Most significant byte of 16-bit word Y used in reading RAM locations in chip 0. |
| YRAMTL | RAM Data YTL | 1:4:0–7 | Least significant byte of 16-bit word Y used in reading RAM locations in chip 1. |
| YRAMTM | RAM Data YTM | 1:5:0–7 | Most significant byte of 16-bit word Y used in reading RAM locations in chip 1. |
| RDL | Remote Digital Loopback | (0,1):A:6 | When configuration bits RDL are a 1, it causes the modem to initiate a request for the remote modem to go into digital loopback. RXD is clamped to a mark and the CTS bit and $\overline{CTS}$ signal will be reset until the loop is established. The TM bit is not set in this case, since the local modem initiated the request. RDL does not function in 300 bps. |
| RI | Ring Indicator | 1:8:4 | When status bit RI is a 1, it indicates that a ringing signal is being detected. The RI bit follows the ringing signal with a 1 during the on time and a zero during the off time coincident with the $\overline{RI}$ signal. The following are the RI bit response times:<br>**RI Bit Transition** — **Response**<br>OFF-to-ON* — 110 ±50 ms (50% duty cycle)<br>ON-to-OFF — 450 ±50 ms<br>*The OFF-to-ON time is duty cycle dependent: 890 ms (15%) ≥ time ≥ 50 ms (100%)<br>This OFF-to-ON (or ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent transition of the RI bit. |

**Table 11. Interface Memory Definitions (Continued)**

| Mnemonic | Name | Memory Location | Description |
|---|---|---|---|
| RLSD | Received Line Signal Detector | 0:8:0 | When status bit RLSD is a 1, it indicates that the carrier has successfully been received. RLSD will not respond to the guard tones or answer tones. RLSD response times are given below:<br><br>**$\overline{\text{RLSD}}$[1]** — OFF-to-ON: Constant Carrier 40 to 65 ms, Controlled Carrier 40 to 65 ms; ON-to-OFF: Constant Carrier 40 to 65 ms, Controlled Carrier 40 to 65 ms<br><br>**Note:**<br>1. After handshake has occurred. |
| RSD | Receive Space Disconnect | 0:D:1 | When configuration bit RSD is a 1, the modem goes on-hook after receiving approximately 1.6 seconds of continuous spaces. |
| RTRN | Retrain (2400 bps only) | 1:9:6 | When configuration bit RTRN is a 1, the modem sends the training sequence. It resets when the training sequence from the remote modem has successfully been received. If the sequence has not been successfully received from the remote modem, CTS will remain OFF. In order to put the modem back in the data mode, it is necessary to write a 0 into the RTRN bit, then repeat the retrain sequence. |
| RTS | Request-to-Send | 1:9:3 | When control bit RTS is a 1, the modem transmits any data on TXD when CTS becomes active. In constant carrier mode, RTS should be set the same time as DTR and then left ON. In controlled carrier operation, independent operation of RTS turns the carrier ON and OFF. The responses to RTS are shown (assume the modem is in data mode).<br><br>**Leased or Dial Line[1] / RTS Off / RTS On**<br>Controlled Carrier: CTS OFF, Carrier OFF / Carrier ON, 210 to 275 ms Scrambled 1's Transmitted, CTS ON<br>Constant Carrier: CTS OFF, Carrier ON, Scrambled 1's Transmitted / CTS ON, Carrier ON, Data Transmitted<br><br>**Note:**<br>1. After handshake is complete.<br><br>For ease of use in constant carrier mode, RTS should be turned ON the same time as DTR. |
| SPEED | Speed Indication | 0:9:(4,5) | The SPEED status bits reflect the speed at which the modem is operating. The SPEED bit representations are shown.<br><br>4 5 Speed<br>0 0 0-300<br>0 1 600<br>1 0 1200<br>1 1 2400<br><br>**Note:**<br>The SPEED bits are not active in analog loopback and leased line mode. |

**Table 11. Interface Memory Definitions (Continued)**

| Mnemonic | Name | Memory Location | Description |
|---|---|---|---|
| SSD | Send Space Disconnect | 1:D:0 | When configuration bit SSD is a 1, it causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR goes from active to inactive state. |
| ST | Self Test | (0,1):A:4 | When configuration bit ST is a 1, self test is activated. ST must be a 0 to end the test. It is possible to perform self test in analog loopback with or without a DTE connected. During any self test, TXD and RTS are ignored. Self test does not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver.<br><br>Error detection is accomplished by monitoring the self test error counter in the RAM. If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic register when the RAM access code 00 is loaded in the diagnostic control register (0:F).<br><br>*Self Test End-to-End (Data Mode)*<br><br>Upon activation of self test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler.<br><br>*Self Test with Loop 3*<br><br>Loop 3 is applied to the modem as defined in Recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test, In this test DTR is ignored.<br><br>*Self Test with Loop 2 (Data Mode)*<br><br>The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test.<br><br>ST does not function in 300 bps. |
| 3DB | 3 dB Loss to Receive Signal | 1:B:2 | When configuration bit 3DB is a 1, it attenuates the received signal 3 dB. This is only used if the modem will see 0 dBm or greater line signal at the receiver input. Insertion of the 3 dB loss will then prevent saturation. |
| TM | Test Mode | 0:8:1 | When status bit TM is a 1, it indicates that the modem has completed the handshake and is in one of the following test modes: AL or RDL. |
| TONE | Tone Detect | 0:8:7 | TONE follows the energy detected in the 340 to 640 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle of the TONE bit. TONE is active only when CRQ in chip 0 is a 1.<br><br>Detection Range: -10 to -43 dBm<br>Response Time: 17 ±2 ms |
| TXCLK | Transmit Clock Select | 1:C:(5,6) | TXCLK allows the user to designate the origin of the transmitter data clock, as shown below:<br><br>**Configuration Word**<br>**Transmit Clock** — **6** **5**<br>Internal — 0 0<br>External — 1 0<br>Slave — 1 1<br><br>If external clock is chosen the user clock must be input at XTCLK. The clock characteristics must be the same as TDCLK. The external clock will be reflected by TDCLK.<br><br>If slave clock is chosen the transmitter is slaved to the receive clock. This is also reflected by TDCLK. |

Table 11. Interface Memory Definitions (Continued)

| Mnemonic | Name | Memory Location | Description |
|---|---|---|---|
| TX LEVEL | Transmit Level | 1:B:(5–7) | TX LEVEL allows the user to change the transmit level at TIP and RING (assuming the DAA has 10 dBm attenuation in the transmit path).<br><br>Configuration Word 7 6 5 / Transmit Level (± 1.0 dBm) (at TIP and RING)<br>0 0 0 — –10 dBm<br>0 0 1 — –12 dBm<br>0 1 0 — –14 dBm<br>0 1 1 — –16 dBm<br>1 0 0 — –18 dBm<br>1 0 1 — –20 dBm<br>1 1 0 — –22 dBm<br>1 1 1 — –24 dBm |

### Internal Modem Timing

In a microprocessor environment it is necessary to know how long various functions last or what the response times of certain functions are. Since the modem is a part of the microprocessor environment its timing and response times are necessary. Table 12 provides the timing relationships between interface memory bits and modem functions.

Table 12. Internal Modem Timing

| Parameter | Time Interval |
|---|---|
| NEWC bit checked | |
| Transmitter | Once per sample[1] |
| Receiver | Once per baud[2] |
| NEWC bit set by host until modem action | |
| Transmitter | ≤ One baud time |
| Receiver | One baud time |
| Control, Configuration bits read | |
| Transmitter | Only after NEWC is set |
| Receiver | ST, RSD—every sample, all others after NEWC set |
| Status bits updated | |
| Transmitter | Once per sample |
| Receiver | Once per baud |
| Status change reflected by NEWS, IRQ | |
| Transmitter | MIN < one sample time<br>MAX one sample time |
| Receiver | MIN one sample time<br>MAX one baud time |
| Memory status reflected to modem pin | |
| Transmitter | 33.33 μs |
| Receiver | 33.33 μs |

1. Sample Time = 7200 Hz 2. Baud Time = 600 Hz

## AUTO DIAL SEQUENCE

The following flow chart defines the auto dial sequence via the microprocessor interface memory.

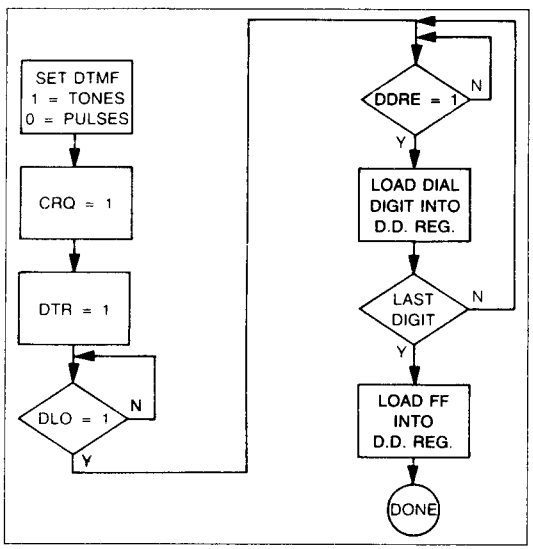



Figure 13. Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

## SIGNAL PROCESSOR RAM ACCESS

### RAM AND DATA ORGANIZATION

Each signal processor contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16-bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

### Interface Memory Locations

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit normally transfers a word from RAM to interface memory once each clock cycle of the SP device. In the transmitter, a word is transferred from SP RAM to the interface memory every sample time. In the receiver, a word is transferred from RAM to the interface memory every sample time as well. Each RAM word transferred to the interface memory is 32-bits long. These bits are written by the SP logic unit into interface memory registers 5, 4, 3, and 2. Registers 3 and 2 contain the most significant byte and least significant byte, respectively, of the XRAM data. Registers 5 and 4 contain the most and least significant bytes of YRAM data, respectively.

### RAM Access Codes

The SP logic unit determines the SP RAM address to read from, or write to, by the code stored in the RAM Access bits of interface memory register F (RAM Access R in the receiver 0:F and RAM Access T in the transmitter 1:F).

Only the transmitter (chip 1) allows data to be transferred from interface memory to SP RAM. When set to a 1, bit 1:F:7 signals the SP logic unit to disable transfer of SP RAM data to the interface memory, and instead, to transfer data from interface memory to SP RAM. When writing into SP RAM, 32 bits of data in the XRAM and YRAM registers will be written into the appropriate SP RAM location as specified by the RAM access code (82-86) in register 1:F (Table 13). Once the data is written into the RAM access register 1:F, the XRAM registers 1:2 and 1:3 or the YRAM registers 1:4 and 1:5, set the NEWC bit 1:E:3 to a 1. This action causes the information to be transferred from interface memory into SP RAM. Bit 7 of register 1:F is cleared to a 0 by the modem after the RAM is read. New data can be written into the SP RAM after the NEWC bit is reset to a 0 by the SP.

**Note:**

Any transmitter RAM Write operation must always be preceded by a RAM read from the desired location. This is to guarantee that the correct information is written into the 16 unchanged bits, since all transmitter RAM operations are 32 bit transfers with typically only 16 of the bits used.

Both the transmitter and receiver (chips 1 and 0, respectively) allow data to be transferred from SP RAM into the interface memory. A 0 in transmitter bit 1:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the RAM access code in register 1:F. A 0 in receiver bit 0:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the access code in register 0:F. To read the SP RAM in chip 1 (transmitter), load into 1:F the RAM access code which identifies the 32 bits of data to transfer to the XRAM and YRAM registers. Next, set the NEWC bit 1:E:3 to a 1. After transferring the data from RAM to the XRAM or YRAM registers, the NEWC bit is reset to a 0 by the SP. Chip 0 (receiver), on the other hand, will provide the XRAM and YRAM data one sample time following the loading of the RAM access code into register 0:F, and will continue to provide the same data at one sample time intervals until a new RAM access code is loaded.

When reading from or writing into RAM, no bits are provided for handshaking or interrupt functions. The NEWC bit can be used as a mechanism to provide sample and baud intervals. Since the NEWC bit is checked, once per baud in chip 0 and once per sample in chip 1, the user can set the NEWC bit and wait for it to be cleared. Depending on which chip the NEWC bit was set, the time interval from the setting to the clearing of the NEWC bit will be either one sample or one baud time. This, however, will not guarantee that the action of reading and writing the XRAM and YRAM will occur in the middle of an actual sample or baud time.

Table 13. RAM Access Codes

| Node | Function | RAM Access Code | | Chip | Reg. No. |
|---|---|---|---|---|---|
| | | RAM Read | RAM Write | | |
| 1 | Demodulator Output | 56 | – | 0 | 2, 3, 4, 5 |
| 2 | Low Pass Filter Output | 40 | – | 0 | 2, 3, 4, 5 |
| 3 | Input Signal to Equalizer Taps | 41–4D | – | 0 | 2, 3, 4, 5 |
| 4 | AGC Gain Word | 14 | – | 0 | 2, 3 |
| 5 | Equalizer Tap Coefficients | 01–0D | – | 0 | 2, 3, 4, 5 |
| 6 | Equalizer Output | 53 | – | 0 | 2, 3, 4, 5 |
| 7 | Rotated Equalizer Output (Received Point Eye Pattern) | 11 | – | 0 | 2, 3, 4, 5 |
| 8 | Decision Points (Ideal Eye Pattern) | 51 | – | 0 | 2, 3, 4, 5 |
| 9 | Rotated Error | 52 | – | 0 | 2, 3, 4, 5 |
| 10 | Rotation Angle | 12 | – | 0 | 4, 5 |
| 11 | Phase Error | 10 | – | 0 | 2, 3 |
| 12 | Self Test Error Counter | 00 | – | 0 | 2, 3 |
| | DTMF Tone Duration | 02 | 82 | 1 | 4, 5 |
| | DTMF Interdigit Delay | 03 | 83 | 1 | 2, 3 |
| | Pulse Interdigit Delay | 03 | 83 | 1 | 4, 5 |
| | Pulse Relay Make Time | 04 | 84 | 1 | 2, 3 |
| | Pulse Relay Break Time | 04 | 84 | 1 | 4, 5 |
| | Handshake Abort Counter | 05 | 85 | 1 | 4, 5 |
| | Handshake Abort Timer | 06 | 86 | 1 | 2, 3 |
| | CTS Off-Time | 07 | 87 | 1 | 2, 3 |

NOTE: 1. All the chip 1 access codes are not valid before R5310-18.
2. Access codes are hexadecimal.
3. Only chip 1 RAM can be written.
4. CTS Off-Time is not valid before R5310-22.

## ERROR RATES

Bit error rate (BER) is a measure of the throughput of data on the communication channel. It is the ratio of the number of received bits in error to the number of transmitted bits. This number increases with decreasing signal-to-noise ratio (SNR). The type of line disturbance and the modem configuration affect the BER.

Tables 14 through 16 summarize the BERs for various conditions. Figure 14 shows the BER measurement setup.

Table 14. BER Summary

| R2424 | | Signal to Noise Ratio | |
|---|---|---|---|
| Data Rate | Bit Error Rate | Originate Mode | Answer Mode |
| 2400 bps | $1 \times 10^{-5}$ | 16.6 dB | 16.2 dB |
| 1200 bps | $1 \times 10^{-5}$ | 8.2 dB | 7.9 dB |
| 600 bps | $1 \times 10^{-5}$ | 5.0 dB | 5.0 dB |
| 300 bps | $1 \times 10^{-5}$ | 9.2 dB | 7.0 dB |

**Test Condition: Signal Level = –30 dBm,**
Sync for 2400 bps, 1200 bps, 600 bps,
Async for 300 bps,
**With 3002 Unconditioned Line.**

Table 15. BER Summary

| R2424 | | Signal to Noise Ratio | |
|---|---|---|---|
| Data Rate | Bit Error Rate | Originate Mode | Answer Mode |
| 2400 bps | $1 \times 10^{-5}$ | 19.0 dB | 17.3 dB |
| 1200 bps | $1 \times 10^{-5}$ | 8.3 dB | 8.1 dB |
| 600 bps | $1 \times 10^{-5}$ | 5.0 dB | 5.0 dB |
| 300 bps | $1 \times 10^{-5}$ | 10.4 dB | 7.2 dB |

**Test Condition: Signal Level = – 43 dBm,**
Sync for 2400 bps, 1200 bps, 600 bps,
Async for 300 bps,
**With 3002 Unconditioned Line.**

Table 16. BER Summary

| R2424 | | Signal to Noise Ratio | |
|---|---|---|---|
| Data Rate | Bit Error Rate | Originate Mode | Answer Mode |
| 2400 bps | $1 \times 10^{-5}$ | 17.0 dB | 16.6 dB |
| 1200 bps | $1 \times 10^{-5}$ | 7.7 dB | 7.9 dB |
| 600 bps | $1 \times 10^{-5}$ | 4.6 dB | 4.5 dB |
| 300 bps | $1 \times 10^{-5}$ | 9.3 dB | 6.2 dB |

**Test Condition: Signal Level = –40 dBm,**
Sync for 2400 bps, 1200 bps, 600 bps,
Async for 300 bps,
**Back-To-Back.**

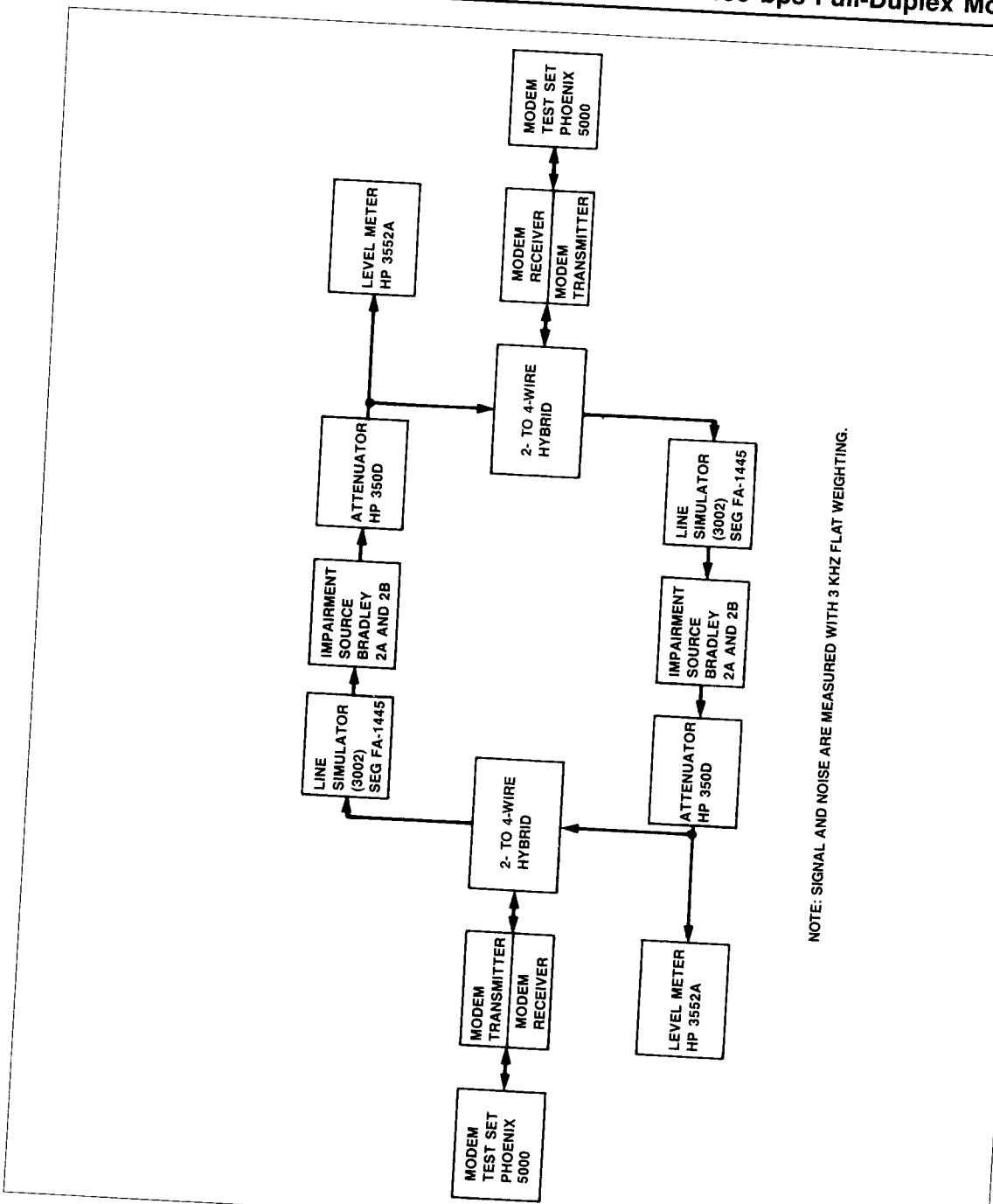



Figure 14. 2-Wire Full-Duplex Bit Error Rate Performance Test Setup (Bidirectional)

**Table 17. Modem Power Requirements**

| Voltage | Tolerance | Current (Typical) @ 25°C | Current (Max) @ 0°C |
|---|---|---|---|
| +5 Vdc | ±5% | 390 mA | <455 mA |
| +12 Vdc | ±5% | 25 mA | < 30 mA |
| -12 Vdc | ±5% | 4 mA | < 5 mA |
| **Note:** All voltages must have ripple ≤0.1 volts peak-to-peak. | | | |

**Table 18. Modem Environmental Restrictions**

| Parameter | Specification |
|---|---|
| Temperature | |
| Operating | 0°C to +60°C (32°F to 140°F) |
| Storage | -40°C to +80°C (-40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container) |
| Relative Humidity: | Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less. |
| Altitude | -200 feet to +10,000 feet |

**Table 19. Modem Mechanical Considerations**

| Parameter | Specification |
|---|---|
| DIN Connector Version | |
| Board Structure: | Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female. |
| Mating Connector: | Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent. |
| PCB Dimensions: | |
| DC Version | |
| Width | 3.937 in. (100 mm) |
| Length | 4.725 in. (120 mm) |
| Height | 0.75 in. (19 mm) |
| M Version | |
| Width | 3.937 in. (100 mm) |
| Length | 3.328 in. (82 mm) |
| Height | 0.40 in. (10.2 mm) |
| Weight (max): | 0.45 lbs. (0.20 kg.) |
| Lead Extrusion (max.): | 0.100 in. (2.54 mm) |
| DIP Connector Version | |
| Board Structure | Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration. |
| Dimensions | |
| Width | 2.0 in. (50.8 mm) |
| Length | 3.5 in. (88.9 mm) |
| Height | 0.2 in. (5.08 mm) above, 0.13 in. (3.30 mm) below |
| Weight (max.) | 2.6 oz. (73g) |
| Pin Length (max.) | 0.53 in. (13.5 mm) above |

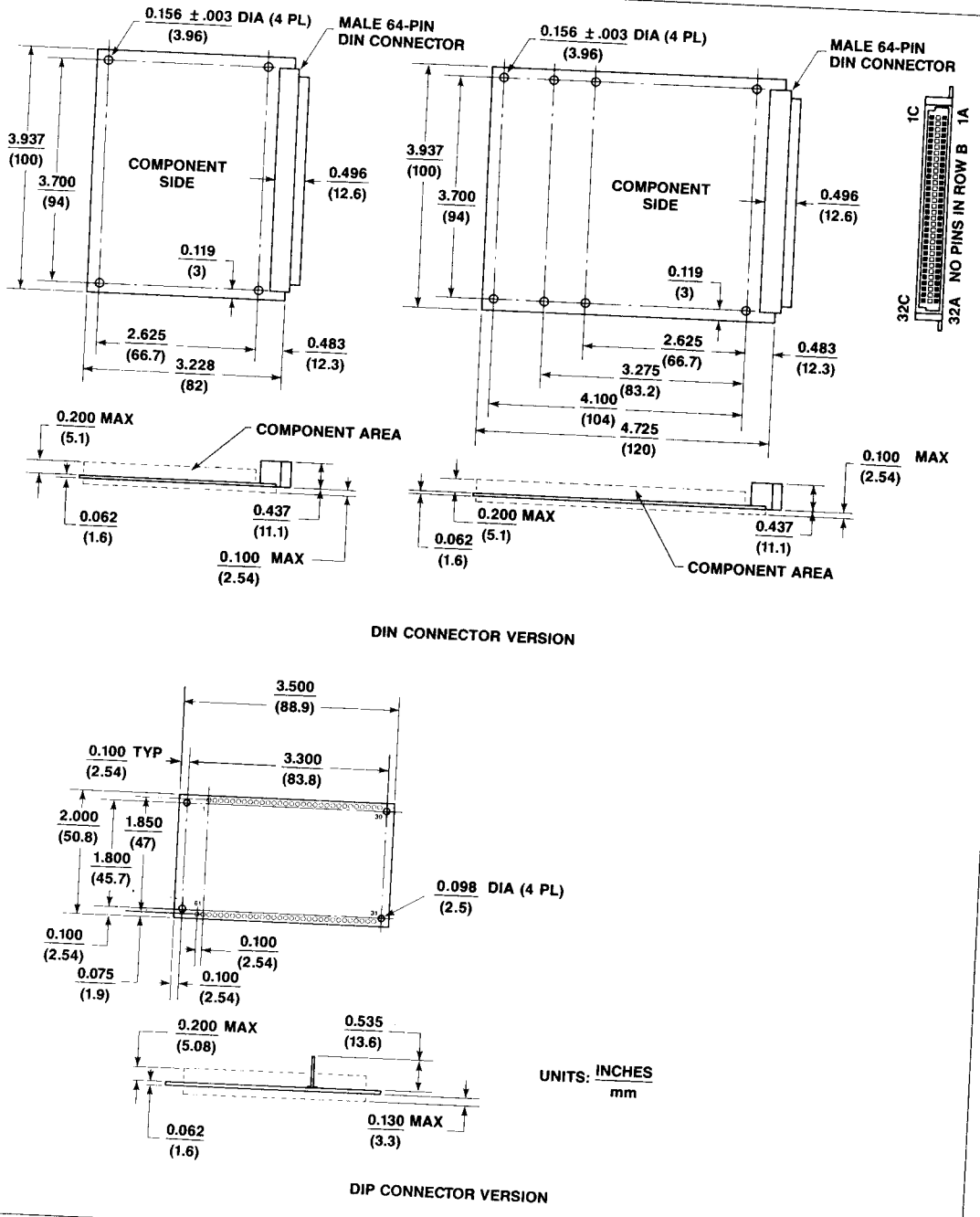



Figure 15. R2424 Modem Dimensions and Pin Locations

## R2424 MODEM INSTALLATION AND MAINTENANCE

This section contains installation instructions and maintenance procedures for the Rockwell R2424DC Modem. It also contains a special notice from the Canadian Department of Communications (DOC) for Canadian operation and from the Federal Communications Commission (FCC) for United States operation.

## GENERAL DESCRIPTION

The Rockwell R2424DC modem is designed to be used with the United States or Canadian Telephone Switched Networks in 2-wire full-duplex dial-up operation. The modem requires protective circuitry registered with the Federal Communications Commission (FCC) Part 68 which allows direct connection to the U.S. switched telephone network. This circuitry also complies with the Canadian Department of Communications (DOC) Terminal Attachment Program (TAP) which similarly defines their switched telephone network requirements.

The R2424DC features automatic dial and answer capabilities along with surge suppression and hazardous voltage and longitudinal balance protection. Its maximum output signal level at the telephone interface is set at $-10$ dBm $\pm 1$ dBm (permissive mode of operation).

Two standard telephone jack connectors (RJ11s) are mounted side by side on one edge of the board and are wired in parallel. One is for connection to the telephone line network and the other for the telephone headset connection.

## INSTALLATION AND SIGNAL ROUTING INSTRUCTIONS

### PHYSICAL MOUNTING

The modem module may be physically incorporated into the customer's end product by utilizing the four corner 0.156" diameter mounting holes (for the self-hooking plastic type standoffs or for bolting it down to some rigid structure) or by installing the module into card guides.

### ELECTRICAL INTERFACING INSTRUCTIONS

The electrical interfacing is accomplished via the DIN (Euro) connector (for external power inputs and digital logic signals) and the telco connectors (for the telephone network connection). Note that the telephone interface connectors are physically separated from the modem interface control connector and extreme care must be taken in routing the telephone interface leads from the modem to the telephone network (line connector jack in the wall).

### FCC RULES PART 68 REQUIREMENTS

The FCC Rules Part 68 requires that the telephone interface leads shall:

1. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use the same connector as leads or metallic paths connecting to power connections.

   **Note**

   Power connections are defined as the connections between commercial power and any transformer, power supply rectifier, converter or other circuitry associated with the modem. The connections of the interface pins (including the + 12 Vdc, – 12 Vdc and + 5 Vdc) are not considered power connections.

2. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use adjacent pins on the same connector as metallic paths that lead to unregistered equipment, when specification details provided to the FCC do not show that the interface voltages are less than nonhazardous voltage source limits in Part 68.

   **Note**

   All the DIN connector interface voltages to the modem have been established as non-hazardous.

### ROUTING OF TELEPHONE INTERFACE LINES

In routing the telephone interface leads from the modem telephone connector jacks to the telephone line network connection, the following precautions should be strongly considered for safety.

1. The telephone interface routing path should be as direct and as short as possible.
2. Any cable used in establishing this path should contain no signal leads other than the modem telephone interface leads.
3. Any connector used in establishing this path shall contain not commercial power source signal leads, and adjacent pins to the TIP and RING (T and R) pins in any such connector shall not be utilized by any signals other than those shown in this document.

## MAINTENANCE PROCEDURE

Under the FCC Rules, no customer is authorized to repair modems. In the event of a Rockwell modem malfunctioning, return it for repair to an authorized ROCKWELL INTERNATIONAL distributor (if in Canada) or send it directly to the Semiconductor Products Division, Rockwell International Corporation, El Paso, Texas 79906.

## SPECIAL INSTRUCTION TO USERS

If the Rockwell modem has been registered with the Federal Communications Commission (FCC), you must observe the following to comply with the FCC regulations:

A. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.

B. It is prohibited to connect the modem to pay telephones or party lines.

C. You are required to notify the local telephone company of the connection or disconnection of the modem, the FCC registration number, the ringer equivalence number, the particular line to which the connection is made and the telephone number to be associated with the jack.

**Note**

If the proper jacks are not available, you must order the proper type of jacks to be installed by the telephone company (VSOC RJ11 for permissive mode of operation).

D. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only if it can be determined that the telephone line and not the modem is the source of trouble. If the Rockwell modem needs repair, return it to the ROCKWELL INTERNATIONAL CORPORATION. This applies to the modem whether it is in or out of warranty. Do not attempt to repair the unit as this is a violation of the FCC rules and may cause danger to persons or to the telephone network.

## TELEPHONE COMPANY RIGHTS AND RESPONSIBILITIES

A. The Rockwell modem contains protective circuitry to prevent harmful voltages to be transmitted to the telephone network. If such harmful voltages do occur, then the telephone company may temporarily discontinue service to you. In this case, the telephone company should:

1. Promptly notify you of the discontinuance.
2. Afford you the opportunity to correct the situation which caused the discontinuance.
3. Inform you of your right to bring a complaint to the FCC concerning the discontinuance.

B. The telephone company may make changes in its facilities and services which may affect the operation of your equipment. It is, however, the telephone company's responsibility to give you adequate notice in writing to allow you to maintain uninterrupted service.

## LABELING REQUIREMENTS

A. The FCC requires that the following label be prominently displayed on the outside surface of the customer's end product and that the size of the label should be such that all the required information is legible without magnification.

Sample label below:

Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.

FCC Registration Number: AMQ9SQ-14211-DM-E

Ringer Equivalence: 0.9B

**Note**

The Rockwell modem module has the FCC registration number and ringer equivalence number permanently affixed to the solder side of the PCB and any unit containing this modem shall use this information for the label requirements.

## SPECIAL NOTICE FROM THE CANADIAN DEPARTMENT OF COMMUNICATIONS

The Canadian Department of Communications label identifies certified equipment. This certification means that the equipment meets certain telecommunications network protective, operational and safety requirements. The Department does not guarantee the equipment will operate to the user's satisfaction.

Before installing this equipment, users should insure that it is permissible to be connected to the facilities of the local telecommunications company. The equipment must also be installed using an approved method of connection. In some cases, the company's inside wiring associated with a single line individual service may be extended by means of a certified jack-plug-cord ensemble (telephone extension cord). The customer should be aware that the compliance with the above conditions may not prevent degradation of service in some situations. Existing telecommunications company requirements do not permit their equipment to be connected to customer-provided jacks except where specified by individual telecommunications company tariffs.

The Department of Communications requires the Certificate Holders to identify the method of network connection in the user literature provided with the certified terminal equipment.

Repairs to certified equipment should be made by an authorized Canadian maintenance facility designated by the supplier. Any repairs or alterations made by the user to this equipment, or equipment malfunctions may give the telecommunications company cause to request the user to disconnect the equipment.

Users should ensure for their own protection that the electrical ground connections of the power utility, telephone lines and internal metallic water pipe system, if present, are connected together. This precaution may be particularly important in rural areas.

**CAUTION**

Users should not attempt to make such connections themselves, but should contact the appropriate electric inspection authority, or electrician, as appropriate.