

## Bipolar circuit

PLL divider with programmable dividing ratio 1:2 to 1:8191

Together with the types S 0436, TBB 1331 A, and a voltage-controlled oscillator a frequency and phase comparison circuit can be designed, intended for the channel selection in TV sets.

Programming allows quartz-controlled setting of the oscillator frequency for the television bands I/III/IV/V) in 125 kHz raster.

- Few external components
- Internal time base
- High noise immunity

Type	Ordering code	Package outline
S 0437	Q67000-A1347	DIP 16

## Maximum ratings

Supply voltage	$V_9$	6.5	V
	$V_3$	13.5	V
Input voltage IFO	$V_{15}$	16	V
Input voltage PLE	$V_{14}$	16	V
Input voltage divider F, $\bar{F}$	$V_7; V_8$	7.5	V
Output voltage clock CL	$V_{12}$	16	V
Sync. output voltage SYNC	$V_{13}$	16	V
Thermal resistance (system-air)	$R_{th SA}$	90	K/W
Junction temperature	$T_j$	150	°C
Storage temperature range	$T_{stg}$	-40 to 125	°C

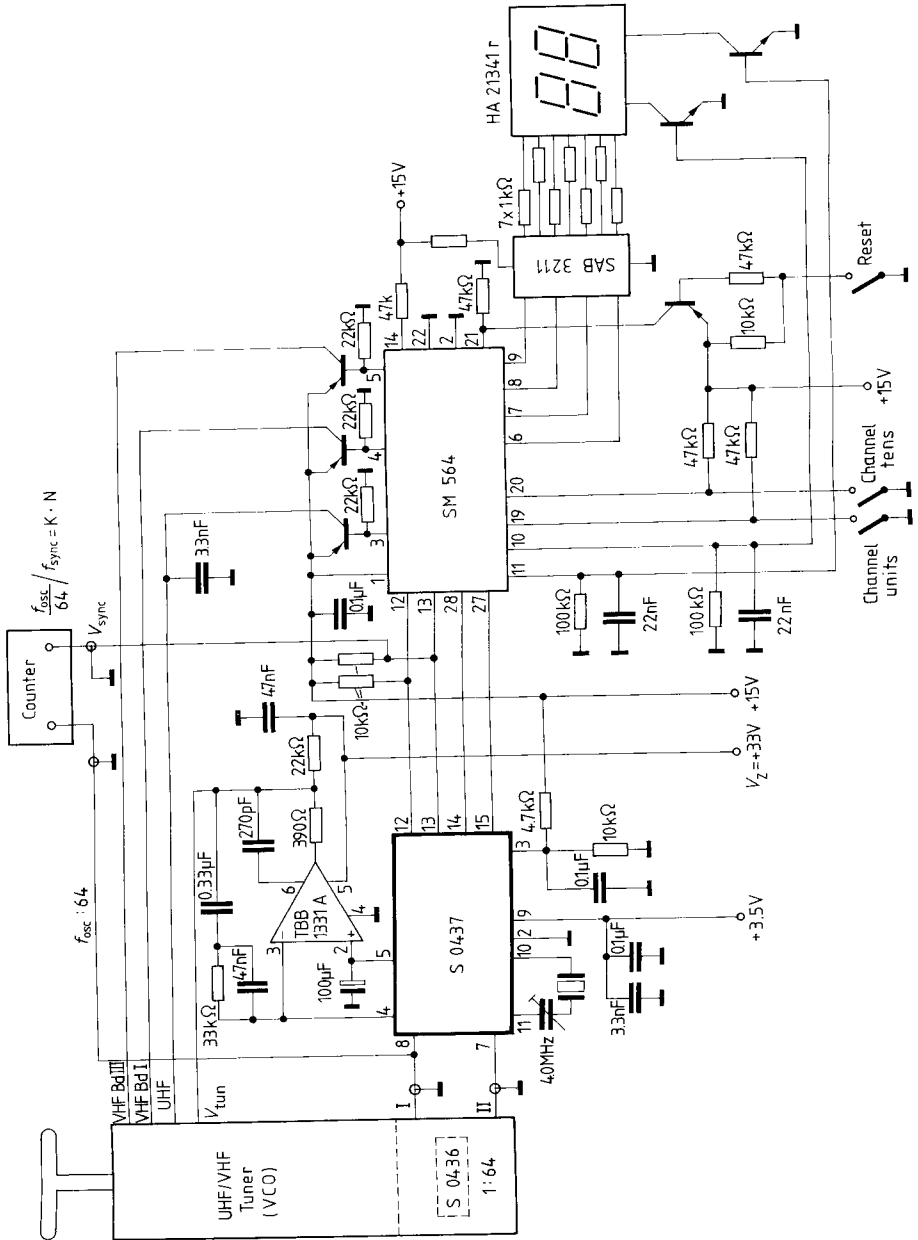
## Range of operation

Supply voltage range	$V_9$	3.25 to 3.75	V
	$V_3$	3.5 to 12.5	V
Input frequency	$f_i$	≤ 15	MHz
Ambient temperature range	$T_{amb}$	0 to 60	°C

**Characteristics** ( $V_G = 3.5 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ) according to test circuit

		min	typ	max	
Current consumption	$I_9$	100	150	200	mA
	$I_3$			1	mA
Input level					
	$I_{7/8 \text{ H}} = 2.4 \text{ mA}$		6.2		V
	$I_{7/8 \text{ L}} = 2.2 \text{ mA}$		5.3		V
<b>Inputs IFO, PLE</b>					
$(V_{\text{pp}} = 15 \text{ V}; \tau = 500 \text{ } \mu\text{s}; T/\tau = 250)$					
	$V_{14/15 \text{ H}}$	14	14.5	15	V
	$I_{14/15 \text{ H}}$			1.5	mA
	$I_{14/15 \text{ L}}$			50	$\mu\text{A}$
Set-up time	$t_S$		1.5		$\mu\text{s}$
Hold time	$t_H$		3.0		$\mu\text{s}$
<b>Clock output CL</b>					
$(V_{\text{pp}} = 15 \text{ V}; R_L \geq 6.8 \text{ k}\Omega)$					
	$V_{12 \text{ H}}$	14	14.5	15	V
	$V_{12 \text{ L}}$			1.5	V
Switching times					
	High pulse width		4		$\mu\text{s}$
	Low pulse width		12		$\mu\text{s}$
	High-low transition time ( $R_L = 9.5 \text{ k}\Omega$ )			0.5	$\mu\text{s}$
	Low-high transition time ( $C_L = 50 \text{ pF}$ )			1.5	$\mu\text{s}$
<b>Synchronous output SYNC</b>					
$(V_{\text{pp}} = 15 \text{ V}; R_L \geq 6.8 \text{ k}\Omega)$					
	$V_{13 \text{ H}}$	14	14.5	15	V
	$V_{13 \text{ L}}$			1.5	V
Switching times					
	High pulse width		8		$\mu\text{s}$
	Low pulse width		504		$\mu\text{s}$
	High-low transition time ( $R_L = 9.5 \text{ k}\Omega$ )			0.5	$\mu\text{s}$
	Low-high transition time ( $C_L = 50 \text{ pF}$ )			1.5	$\mu\text{s}$
	Delay time		4		$\mu\text{s}$
<b>Phase detector output PD</b>					
	$I_{4 \text{ Load}}$		+100		$\mu\text{A}$
	$I_{4 \text{ Sink}}$		-100		$\mu\text{A}$
PD reference PD REF	$V_3$	$\frac{V_3}{2} + 0.2$		$\frac{V_3}{2} + 0.7$	V
Divider input sensitivity ( $f_i = 15 \text{ MHz}$ )	$V_{7/8 \text{ pp}}$	600	800	1000	mV
Lock indication output LOCK IND	$V_{6 \text{ L}}$		0		V
$(R_L = 10 \text{ k}\Omega)$	$V_{6 \text{ H}}$	2.5			V

Test circuit



### Functional description

S 0437 includes a 13 bit parallel-programmable synchronous divider (divider factor  $N = 2$  to 8191), a 13 bit shift register, a quartz oscillator ( $f_{osc} = 4.0$  MHz) with subsequent divider (divider factor  $Q = 2048$ ) and a frequency and phase sensitive digital phase detector. The dividing factor  $N$  — in 13 digit dual code — is serially input into a 13 bit shift register with parallel output. As first bit the LSB (least significant bit) is pushed in, and the MSB (most significant bit) as last one. Acceptance at the information input (IFO) only takes place when the enable input is at high level (PLE). The shifting clock ( $f = 62.5$  kHz) is available at the open collector output (CL). Shifting is done by the low — high transition of the shifting cycle.

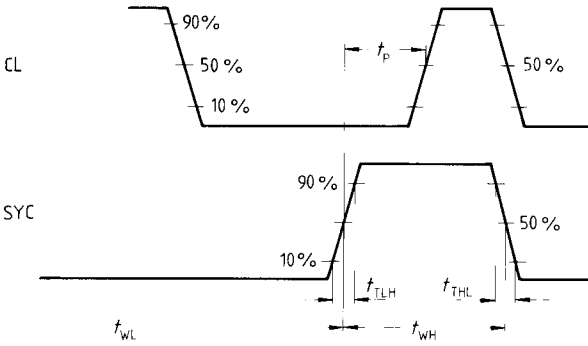
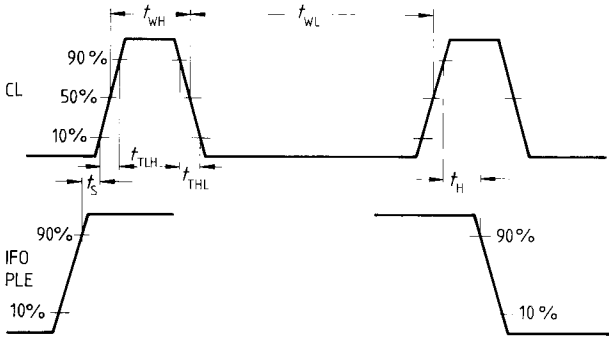
Referred to the high — low transition of the enable input, only the last 13 cycles are utilized. Possible preceding dummy bits remain without importance. H level of the enable input is only allowed to exist when the synchronous output (SYC) is at L level. The synchronous divider has balanced pushpull clock inputs ( $F, \bar{F}$ ) for ECL level.

L signal is obtained at the output LOCK IND in case of frequency and phase synchronization.

The phase detector may be operated with a separated voltage supply ( $V_{S2}$ ). From the output phase detector (PD), the fine tuning voltage for the VCO (tuner) is gained by means of an active PI network (OP AMP). The output PD REF can be used as reference potential for the operational amplifier.



Pulse diagram



Timing diagram

