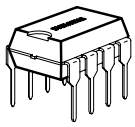
SIEMENS

Nonvolatile Memory 1-Kbit E²PROM SDA 2506-5

Preliminary Data **MOS IC**

Features

- Word-organized, reprogrammable nonvolatile memory in n-channel floating-gate technology
- 128 × 8-bit organization
- Supply voltage 5 V
- Three lines between control processor and E²PROM for data transfer and chip control
- Serial data bus (eight data bits, seven address bits, one control bit)
- More than 10^4 reprogramming cycles per address
- Data retention for more than ten years (operating-temperature range)
- Unlimited number of readout operations without refresh
- Erase or write in 10 ms
- Temperature range 0 to 70 ˚C



P-DIP-8

Type	Ordering Code	Package
SDA 2506-5	Q67100-H5090	P-DIP-8

Circuit Description

Data Transfer and Chip Control

Three lines, each with several functions, are necessary for overall data transfer between the control processor and the E^2PROM:

a) Data line D
– bidirectional serial data transfer
– serial entry of address and control bit
– direct control, D = 1 for erase, D = 0 for write

b) Clock line Φ
– shift clock for data, address and control bits
– start readout with transfer of data from memory into shift register or start of data change during reprogramming

c) Chip-enable line $\overline{CE}$
– chip reset and data input (active high)
– chip enable (active low)

Before the chip is enabled, data, address and control information is clocked in on the bidirectional data bus. These data are retained in the shift register during reprogramming and readout until the second clock pulse. The following data formats have to be entered:

a) Readout memory, one 8-bit control word consisting of
– seven address bits A0 through A6 (A0 first as LSB)
– one control bit CB = "0" after A6

Reprogram Memory

b) Erase, 8-bit input information consisting of
– seven bits of address information A0 through A6 (A0 first as LSB)
– one bit of control information CB = "1" after A6

c) Write, 16-bit input information consisting of
– eight bits of new memory information D0 through D7 (D0 first as LSB)
– seven bits of address information A0 through A6 (A0 first as LSB after D7)
– one bit of control information CB = "1" after A6

d) Erase and write, 16-bit input information consisting of
– eight bits of new memory information D0 through D7 (D0 first as LSB)
– seven bits of address information A0 through A6 (A0 first as LSB after D7)
– one bit of control information CB = "1" after A6

Read (see figure 1)

After data entry, and with CB = 0, the readout operation of the selected word address is started with the transition of $\overline{CE}$ from "1" to "0". The information on the data line during chip enable has no effect.

With the first clock pulse after $\overline{CE}$ = 0, the data word of the selected memory address is transferred into the shift register. With the trailing edge of the first clock pulse the data output goes low-impedance and the first data bit D0 can be read on the data pin. Every further clock pulse shifts another data bit to the output. The data line goes high-impedance again when $\overline{CE}$ changes from "0" to "1".

Reprogram (see figure 2a, 2b and 3)

A complete reprogramming operation consists of an erase operation followed by a write operation. During erase, all bits of the selected word are set to a uniform 1 state, and during write, 0 states are created according to the information in the shift register.

A reprogramming operation is started when, after data entry in chip enable, the control bit CB = "1" appears in the appropriate cell of the shift register. Whether an erase or a write operation is performed will depend on the information on data line D during chip enable.

For resetting to the "1" state there must also be a "1" on the data input during the transition of $\overline{CE}$ from high to low. If a write operation to the 0 state is to be started however, there must be a 0 on the data line during chip enable.

Reset

A memory that is not selected is automatically in reset status because of the "1" state of $\overline{CE}$. All flipflops of the process control are reset. The information in the shift register is retained on the other hand and is not altered until data are shifted. The reset status is also produced by an on-chip circuit when the memory is powered on.

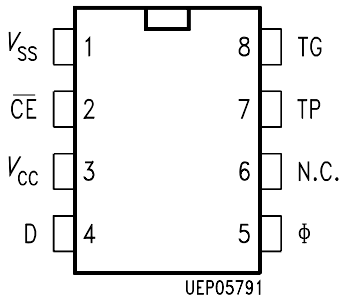
After chip enable a start pulse is required on clock line Φ to initiate programming. The control information on data line D must remain stable until the rising edge of the start pulse. The programming operation begins with the trailing edge of the start pulse and ends with transition of $\overline{CE}$ from low to high.

The reprogramming of a word begins with an erase operation. For this the word address is entered together with control bit CB = "1". The entry of the data word is omitted for an erase. But at this point the data for a following write operation can be entered. If this is intended, the data D0 through D7 for the write operation are entered before entry of the control word for the erase operation. For the erase the data line has to be kept high during chip enable, i.e. transition of $\overline{CE}$ from high to low, and until the falling edge of the start pulse. An erase operation can be followed immediately by a write operation without entry of the data and word address. For this the data line is sent low, $\overline{CE}$ is again driven from high to low (chip enable) and the start pulse for the write operation is put on clock line Φ. The data line must be kept low until the falling edge of the start pulse (**see figure 3**).

Erase and write can also be executed separately. For writing, a 16-bit control word (word address with control bit CB = "1", data D0-D7) is entered. For erasing, only the word address and CB = "1" are entered. For the erase operation the data line must be kept high during chip enable and until the falling edge of the start pulse, and for the write operation it must be kept low (**see figure 2a and 2b**).

Total Erase

If input TP2 (pin 7) is put on V_{CC} = 5 V, this activates the mode for total erasure of memory. The word address 0 and control bit CB = "1" must be entered. The data line has to be kept high during chip enable (transition of $\overline{CE}$ from high to low) and until the falling edge of the start pulse. A total erase operation is ended when $\overline{CE}$ goes from low to high and by switching input TP2 to 0 V.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	$\overline{CE}$	$\overline{CE}$ = 1 for control-world input $\overline{CE}$ = 0 for reprogramming and data output
3	V_{CC}	Supply voltage + 5 V
4	D	Bidirectional data input/output line, for reprogramming: D = 1 erase D = 0 write
5	Φ	Clock
6	N.C.	Not connected (open)
7	TP	Test pin (V_{SS})
8	TG	Test pin (open)

Block Diagram

Absolute Maximum Ratings

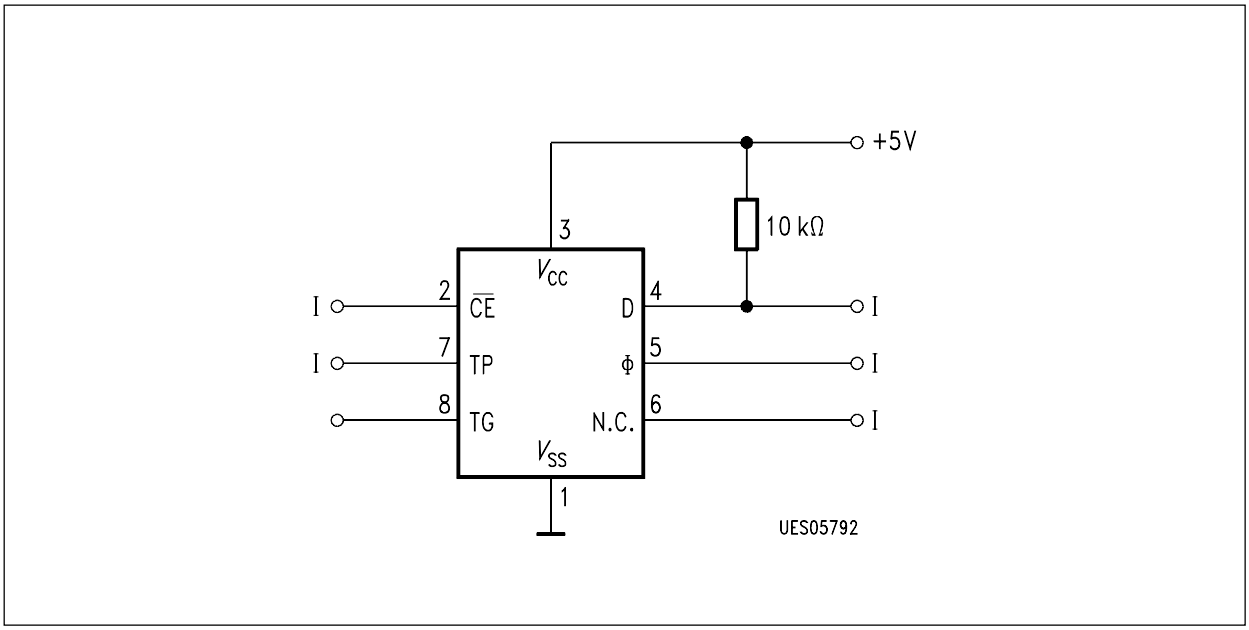
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{CC}	– 0.3	6	V
Input voltage	V_{I}	– 0.3	6	V
Power dissipation	P_{D}		40	mW
Storage temperature	T_{stg}	– 40	125	˚C
Thermal resistance (system-air)	$R_{th\ SA}$		100	K/W

Operating Range

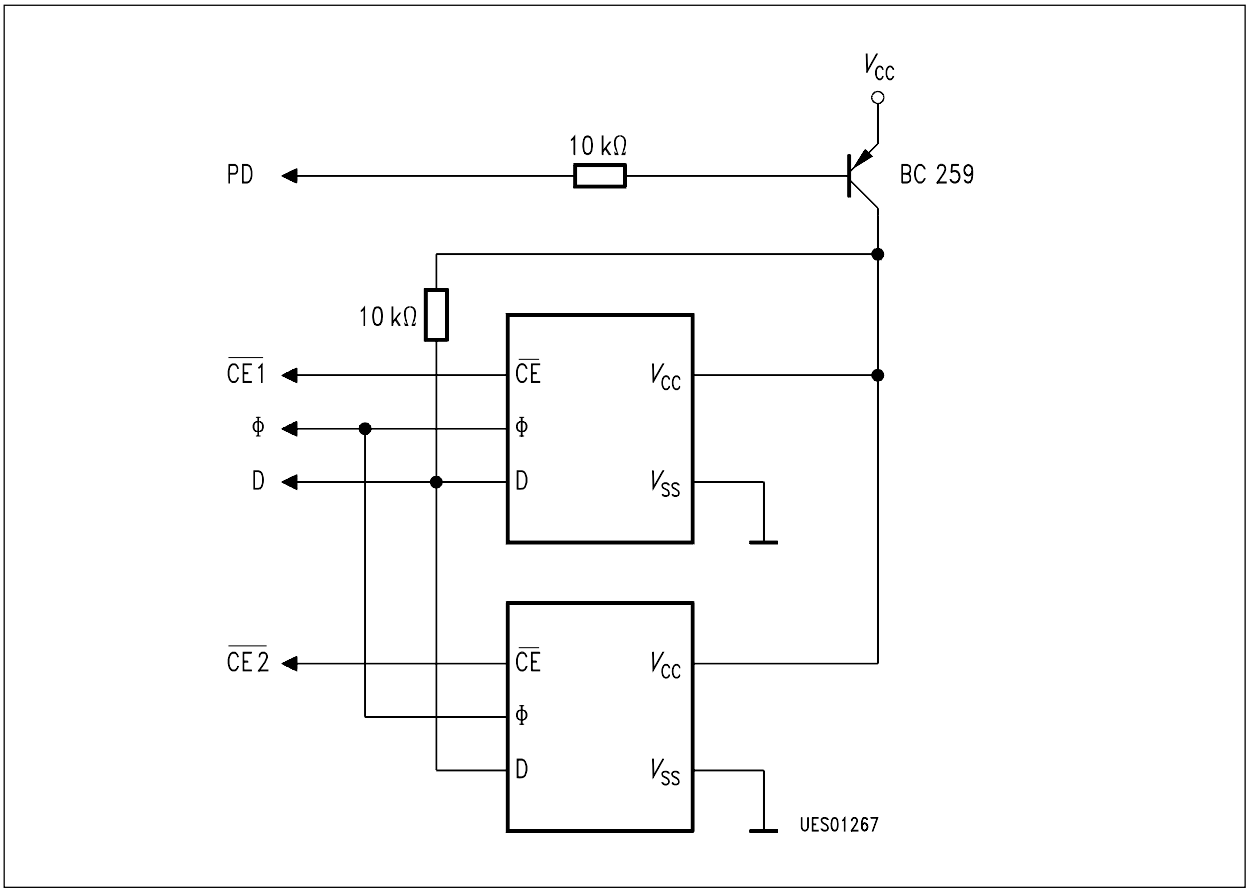
Supply voltage	V_{CC}	4.75	5.25	V
Ambient temperature	T_{A}	0	70	˚C

Characteristics
T_A = 25 ℃

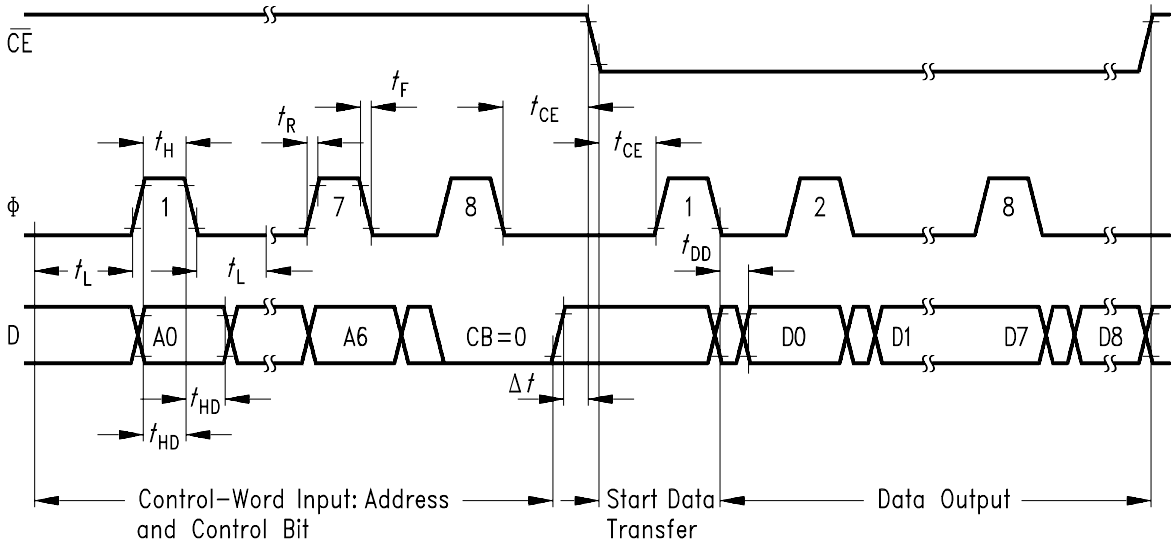
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{CC}	4.75	5	5.25	V	
Supply current	I_{CC}			3	mA	V_{CC} = 5.25 V
Inputs						
Input voltage (D, Φ, $\overline{CE}$)	V_L			0.8	V	
Input voltage (D, Φ, $\overline{CE}$)	V_H	2.4			V	
Input current (D, Φ, $\overline{CE}$)	I_H			10	µA	V_H = 5.25 V
Data Output D (open drain)						
L-output current	I_L			0.5	µA	V_L = 0.8 V
H-output current	I_H			10	µA	V_H = 5.25 V
Clock Pulse Φ						
High duration	t_H	2.5		60	µs	
Low duration	t_L	5			µs	
Time between rising and falling edge $\overline{CE}$ to D	Δt	2.5			µs	
Time between rising and falling edge $\overline{CE}$ to Φ	t_{CE}	5			µs	
Data hold (before/after Φ falling edge)	t_{HD}	2.5			µs	
Data delay (after Φ falling edge)	t_{DD}	2.5			µs	
Rise time	t_R			1	µs	
Fall time	t_F			1	µs	
Erase time	t_{ER}	10		20	ms	
Write time	t_{WR}	10		20	ms	
Total erase	t_{GL}			20	ms	



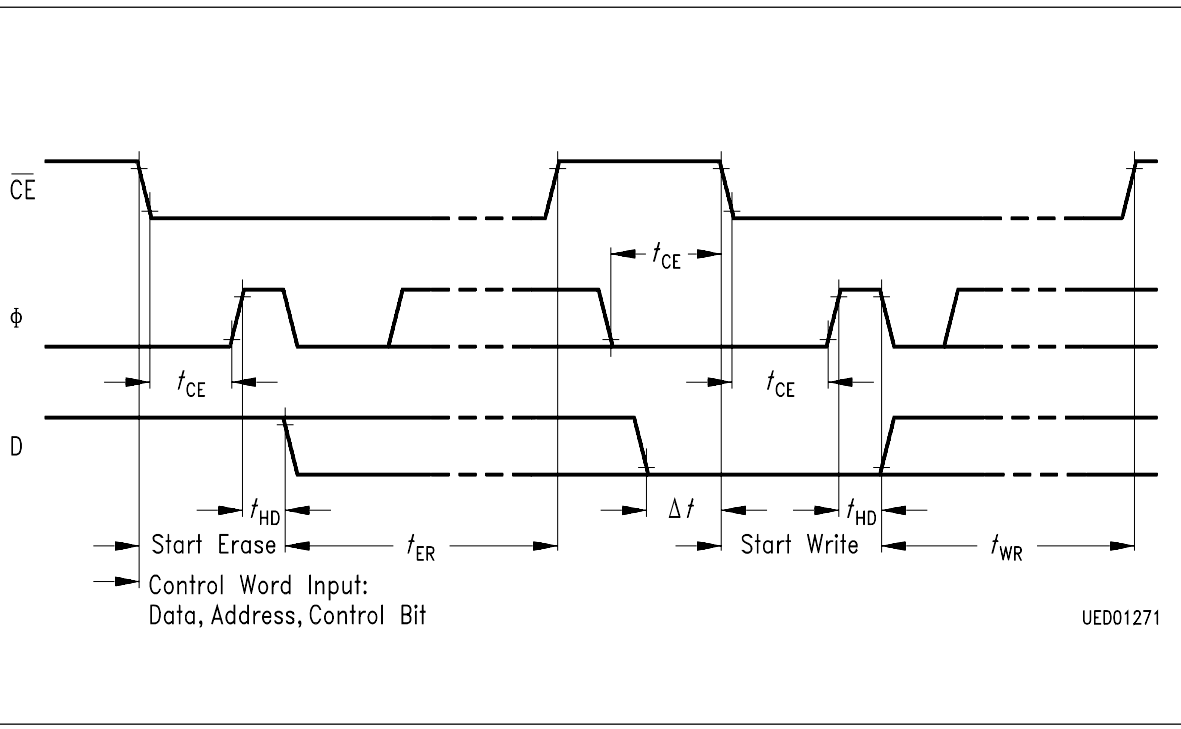
Test Circuit



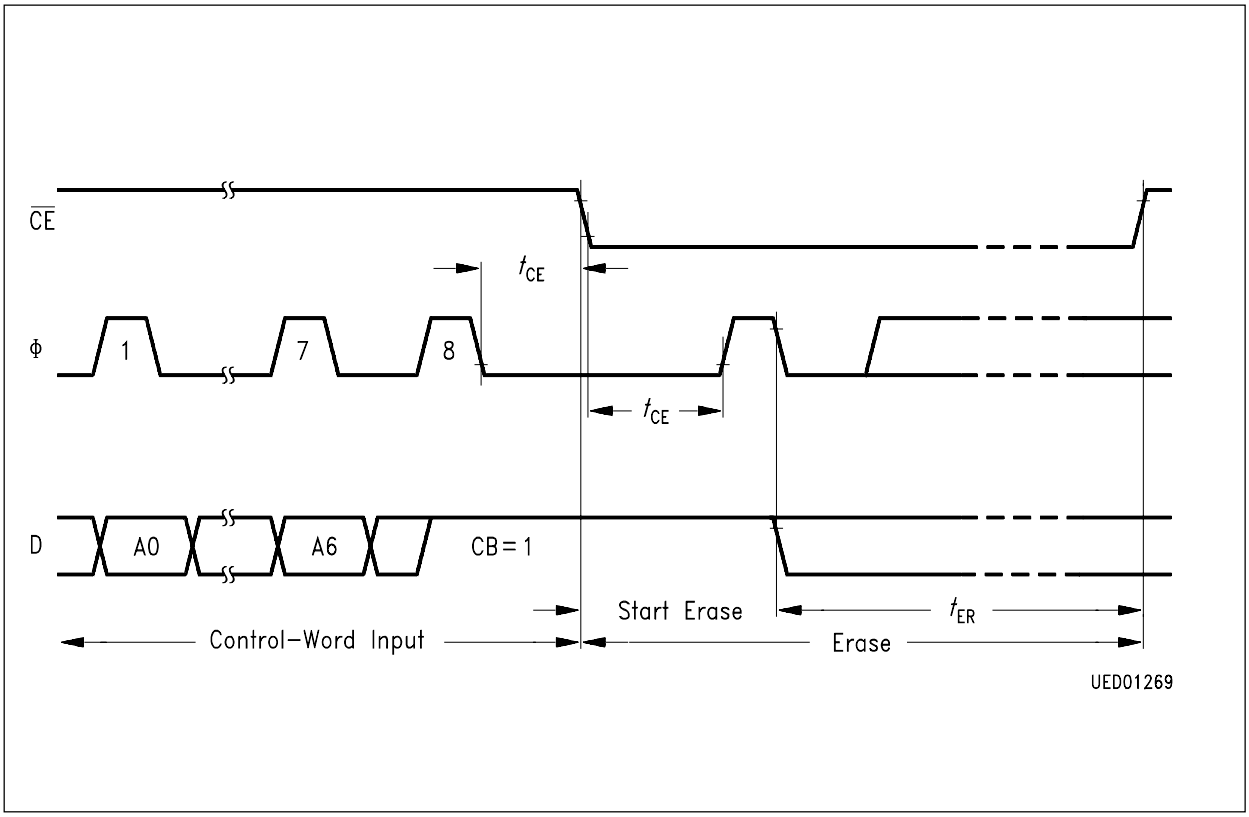
Application Circuit



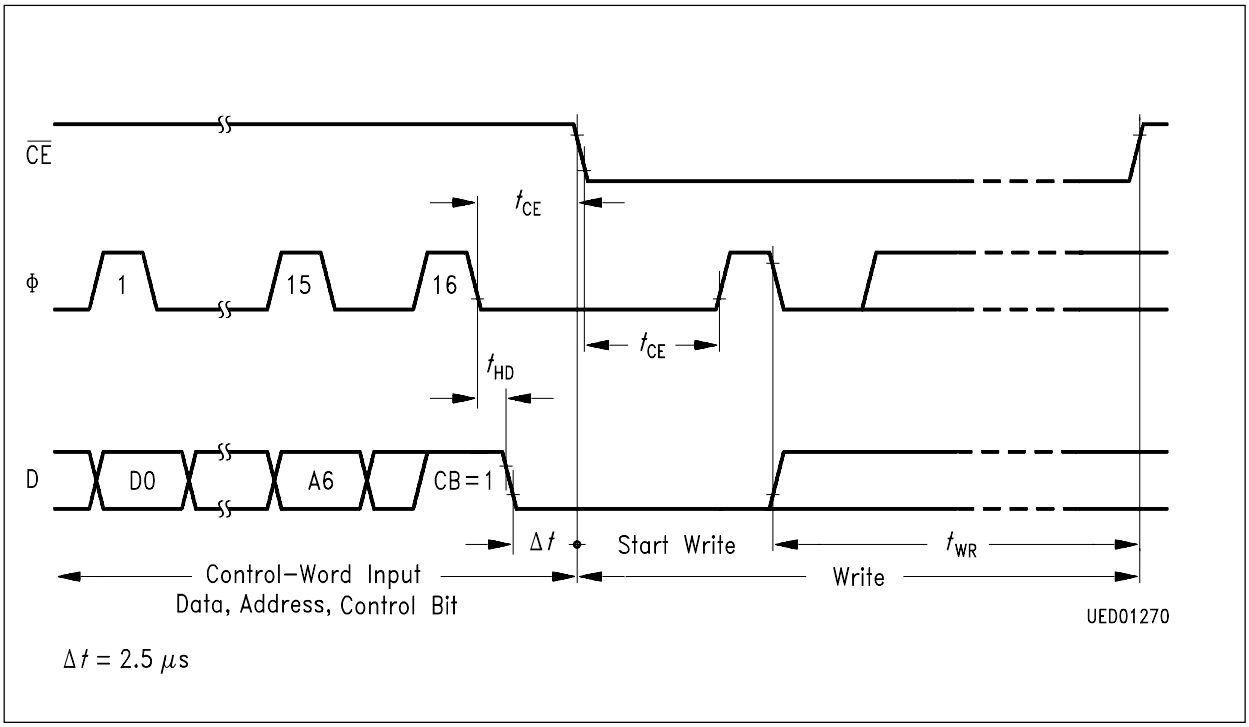
Read



Reprogramming Erase and Write



Reprogram/Erase



Reprogram/Write