

MH25609J-85,-10,-12,-15/ MH25609JA-85,-10,-12,-15

PAGE MODE 262144-WORD BY 9-BIT DYNAMIC RAM

DESCRIPTION

The MH25609J, JA is 262144 word x 9 bit dynamic RAM and consists of nine industry standard 256K x 1 dynamic RAMs in plastic leaded chip carrier.

The mounting of plastic leaded chip carrier on a single in-line package provides any application where high densities and large quantities of memory are required.

MH25609JA is a leaded type-memory module, allowing direct insertion to normal through-hole-board like DIP devices.

MH25609J is a socket type-memory module, suitable for easy interchanging or addition of modules.

FEATURES

- High-speed

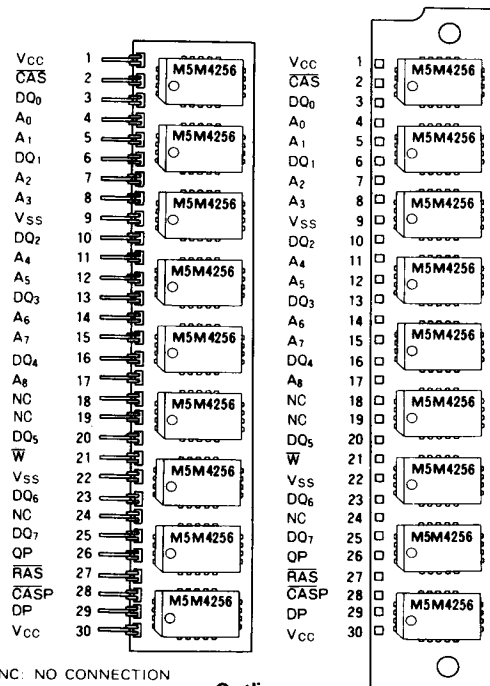
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
MH25609J-85 MH25609JA-85	85	160	2700
MH25609J-10 MH25609JA-10	100	190	2340
MH25609J-12 MH25609JA-12	120	220	2070
MH25609J-15 MH25609JA-15	150	260	1800

- Utilizes industry standard 256K RAMs in plastic leaded carriers
- 30 pins Single In-line Package
- Single +5V ($\pm 10\%$) supply operation
- Low standby power dissipation 225mW (max)
- Low operation power dissipation.
 - MH25609J-85/MH25609JA-85 3.47W (max)
 - MH25609J-10/MH25609JA-10 3.24W (max)
 - MH25609J-12/MH25609JA-12 2.97W (max)
 - MH25609J-15/MH25609JA-15 2.75W (max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.15 μ F x 9) decoupling capacitors
- 256 refresh cycles every 4ms, A₈ Pin is not need for refresh
- Common $\overline{\text{CAS}}$ control for eight common Data-In and Data-Out lines.
- Separate $\overline{\text{CAS}}$ ($\overline{\text{CASP}}$) control for one separate pair of Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operation to prevent contention on Data-In and Data-Out.
- Bit nine (DP, QP) controlled by $\overline{\text{CASP}}$ is generally used for parity.

APPLICATION

Main memory unit for computers, Microcomputer memory

PIN CONFIGURATION (TOP VIEW)



30N5 (MH25609JA)

30N9 (MH25609J)



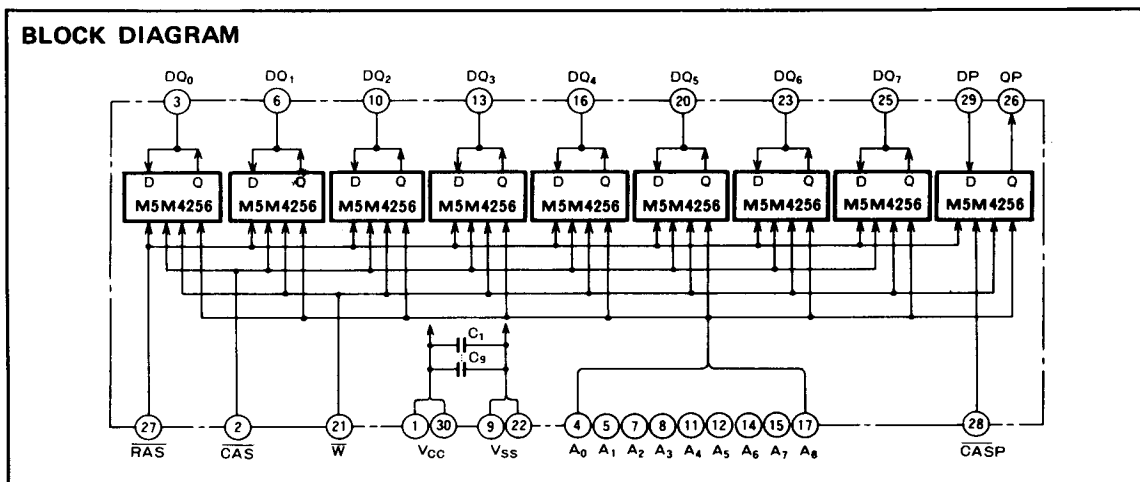
FUNCTION

The MH25609J, JA provides, in addition to normal read and early write operations, a number of other functions, e.g., page mode, RAS-only refresh, hidden refresh and CAS before RAS refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	D	Row address	Column address	Q	
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES
Early write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES
$\overline{\text{CAS}}$ before RAS refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1 ~ 7	V
V _I	Input voltage		-1 ~ 7	V
V _O	Output voltage		-1 ~ 7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a = 25°C	9	W
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low-level input voltage all inputs	-2		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
V _{OH}	High-level output voltage	I _{OH} = -5mA	2.4		V _{CC}	V	
V _{OL}	Low-level output voltage	I _{OL} = 4.2mA	0		0.4	V	
I _{OZ}	Off-state output current	0 floating 0V ≤ V _{OUT} ≤ 5.5V	-20		20	μA	
I _I	Input current	0V ≤ V _{IN} ≤ V _{CC} , Other input pins = 0V	-90		90	μA	
I _{CC1(AV)}	Average supply current from V _{CC} , operating (Note 3, 4)	R _{AS} , C _{AS} cycling t _{CR} = t _{CW} = min, output open	MH25609-85		630	mA	
			MH25609-10		585		
			MH25609-12		540		
			MH25609-15		495		
I _{CC2}	Supply current from V _{CC} , standby	R _{AS} = C _{AS} = V _{IH} output open			40.5	mA	
I _{CC3(AV)}	Average supply current from V _{CC} , refreshing (Note 3)	R _{AS} cycling C _{AS} = V _{IH} t _{C(RAS)} = min, output open	MH25609-85		540	mA	
			MH25609-10		495		
			MH25609-12		450		
			MH25609-15		405		
I _{CC4(AV)}	Average supply current from V _{CC} , page mode (Note 3, 4)	R _{AS} = V _{IL} , C _{AS} cycling t _{CPG} = min, output open	MH25609-85		495	mA	
			MH25609-10		450		
			MH25609-12		405		
			MH25609-15		360		
I _{CC6(AV)}	Average supply current from V _{CC} , automatic refreshing (Note 3)	C _{AS} before R _{AS} refresh cycling t _{O(RAS)} = min, output open	MH25609-85		585	mA	
			MH25609-10		540		
			MH25609-12		495		
			MH25609-15		450		
C _{I(A)}	Input capacitance, address inputs	V _I = V _{SS} f = 1MHz V _I = 25mVrms			60	pF	
C _{I(DO)}	Data input/data output capacitance				17	pF	
C _{I(W)}	Input capacitance, write control input				75	pF	
C _{I(RAS)}	Input capacitance, R _{AS} input				75	pF	
C _{I(CAS)}	Input capacitance, C _{AS} input				70	pF	
C _{I(CASP)}	Input capacitance, C _{ASP} input				13	pF	
C _{I(DP)}	Input capacitance				17	pF	
C _{O(OP)}	Output capacitance		V _O = V _{SS} , f = 1MHz, V _I = 25mVrms			12	pF

- Note 2: Current flowing into an IC is positive, out is negative.
 3. I_{CC1(AV)}, I_{CC3(AV)}, I_{CC4(AV)} and I_{CC6(AV)} are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
 4. I_{CC1(AV)} and I_{CC4(AV)} are dependent on output loading. Specified values are obtained with the output open.



TIMING REQUIREMENTS (For Read, Early Write, Refresh, and Page-Mode Cycle)

($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = -5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time	t_{REF}		4		4		4		4	ms
$t_{W(RASH)}$	\overline{RAS} high pulse width	t_{RP}	65		80		90		100		ns
$t_{W(RASL)}$	\overline{RAS} low pulse width	t_{RAS}	85	10000	100	10000	120	10000	150	10000	ns
$t_{W(CASL)}$	\overline{CAS} low pulse width	t_{CAS}	45	10000	50	10000	60	10000	75	10000	ns
$t_{W(CASH)}$	\overline{CAS} high pulse width (Note 8)	t_{CPN}	20		20		25		25		ns
$t_{h(RAS-CAS)}$	\overline{CAS} hold time after \overline{RAS}	t_{CSH}	85		100		120		150		ns
$t_{h(CAS-RAS)}$	\overline{RAS} hold time after \overline{CAS}	t_{RSH}	45		50		60		75		ns
$t_{d(CAS-RAS)}$	Delay time, \overline{CAS} to \overline{RAS} (Note 9)	t_{CRP}	10		10		10		10		ns
$t_{d(RAS-CAS)}$	Delay time, \overline{RAS} to \overline{CAS} (Note 10)	t_{RCD}	15	40	15	50	20	60	25	75	ns
$t_{SU(RA-RAS)}$	Row address setup time before \overline{RAS}	t_{ASR}	0		0		0		0		ns
$t_{SU(CA-CAS)}$	Column address setup time before \overline{CAS}	t_{ASC}	-5		-5		-5		-5		ns
$t_{h(RAS-RA)}$	Row address hold time after \overline{RAS}	t_{RAH}	10		10		15		20		ns
$t_{h(RAS-CA)}$	Column address hold time after \overline{CAS}	t_{CAH}	15		15		20		25		ns
$t_{h(RAS-CA)}$	Column address hold time after \overline{RAS}	t_{AR}	55		65		80		100		ns
t_{THL}	Transition time	t_T	3	50	3	50	3	50	3	50	ns
t_{TLH}			3	50	3	50	3	50	3	50	ns

- Note 5. An initial pause of 500 μ s is required after power-up followed by any eight \overline{RAS} or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
 6. The switching characteristics are defined at $t_{THL} = t_{TLH} = 5\text{ns}$.
 7. Reference levels of input signals are $V_{IH\ min}$ and $V_{IL\ max}$. Reference levels for transition time are also between V_{IH} and V_{IL} .
 8. Except for page-mode.
 9. $t_{d(CAS-RAS)}$ requirement is only applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
 10. Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{d(RAS)}$ max can be met, $t_{d(RAS-CAS)}$ max is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{d(CAS)}$.
 $t_{d(RAS-CAS)}\ min = t_{h(RAS-RA)}\ min + 2t_{THL}(t_{THL}) + t_{su(CA-CAS)}\ min$.

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted)

Read Cycle

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	t_{RC}	160		190		220		260		ns
$t_{SU(R-CAS)}$	Read setup time before \overline{CAS}	t_{RCS}	0		0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after \overline{CAS} (Note 11)	t_{RCH}	0		0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after \overline{RAS} (Note 11)	t_{RRH}	10		10		10		10		ns
$t_{DIS(CAS)}$	Output disable time (Note 12)	t_{OFF}	0	20	0	25	0	30	0	35	ns
$t_{a(CAS)}$	\overline{CAS} access time (Note 13)	t_{CAC}		45		50		60		75	ns
$t_{a(RAS)}$	\overline{RAS} access time (Note 14)	t_{RAC}		85		100		120		150	ns

- Note 11. Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
 12. $t_{DIS(CAS)}$ max defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL} .
 13. This is the value when $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max. Test conditions; Load = 2TTL, $C_L = 100\text{pF}$.
 14. This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)}$ max. When $t_{d(RAS-CAS)} \geq t_{d(RAS-CAS)}$ max, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, $C_L = 100\text{pF}$.

Write Cycle

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	t_{RC}	160		190		220		260		ns
$t_{SU(W-CAS)}$	Write setup time before \overline{CAS} (Note 15)	t_{WCS}	-10		-10		-10		-10		ns
$t_{h(CAS-W)}$	Write hold time after \overline{CAS}	t_{WCH}	15		20		25		30		ns
$t_{h(RAS-W)}$	Write hold time after \overline{RAS}	t_{WCR}	55		70		85		105		ns
$t_{h(W-RAS)}$	\overline{RAS} hold time after write	t_{RWL}	30		35		40		45		ns
$t_{h(W-CAS)}$	\overline{CAS} hold time after write	t_{CWL}	30		35		40		45		ns
$t_{W(W)}$	Write pulse width	t_{WP}	15		20		25		30		ns
$t_{SU(D-CAS)}$	Data-in setup time before \overline{CAS}	t_{DS}	0		0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after \overline{CAS}	t_{DH}	15		20		25		30		ns
$t_{h(RAS-D)}$	Data-in hold time after \overline{RAS}	t_{DHR}	55		70		85		105		ns

Note 15. When $t_{su(W-CAS)} < t_{su(W-CAS)}\ min$, Data input will contend with the data output because of the common I/O feature.



Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CPG}	Page-mode cycle time	t_{PC}	80		100		120		145		ns
$t_{W(CASH)}$	CAS high pulse width	t_{CP}	25		40		50		60		ns
t_{CPGRW}	Page-mode read-write cycle time	—	105		130		155		180		ns

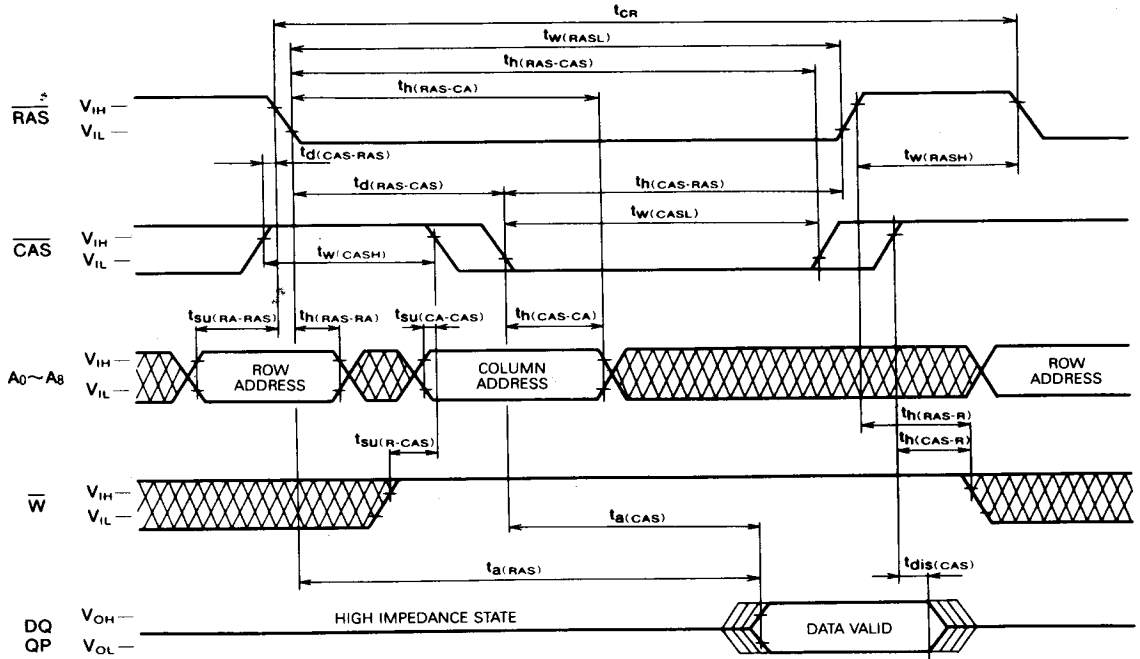
CAS before RAS Refresh Cycle (Note 16)

Symbol	Parameter	Alternative Symbol	Limits								Unit
			MH25609-85		MH25609-10		MH25609-12		MH25609-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{SUR(CAS-RAS)}$	CAS setup time for auto refresh	t_{CSR}	10		10		10		10		ns
$t_{HR(RAS-CAS)}$	CAS hold time for auto refresh	t_{CHR}	15		20		25		30		ns
$t_{dR(RAS-CAS)}$	Precharge to CAS active time	t_{RPC}	0		0		0		0		ns

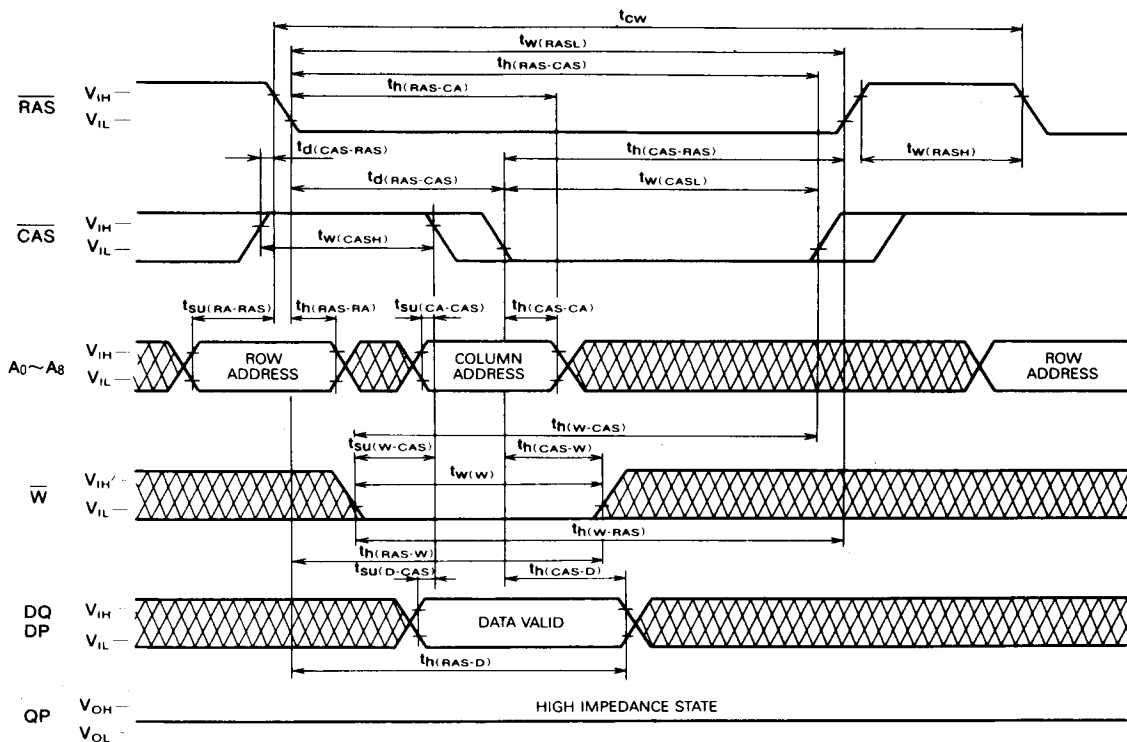
Note 16. Eight or more CAS before RAS cycles is necessary for proper operation of CAS before RAS refresh mode.

TIMING DIAGRAMS (Note 17)

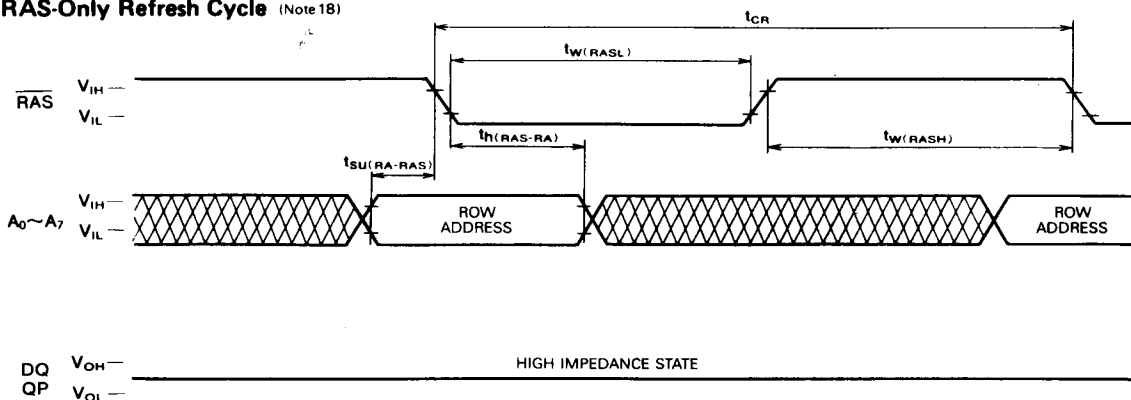
Read Cycle



Early Write Cycle



RAS-Only Refresh Cycle (Note 18)

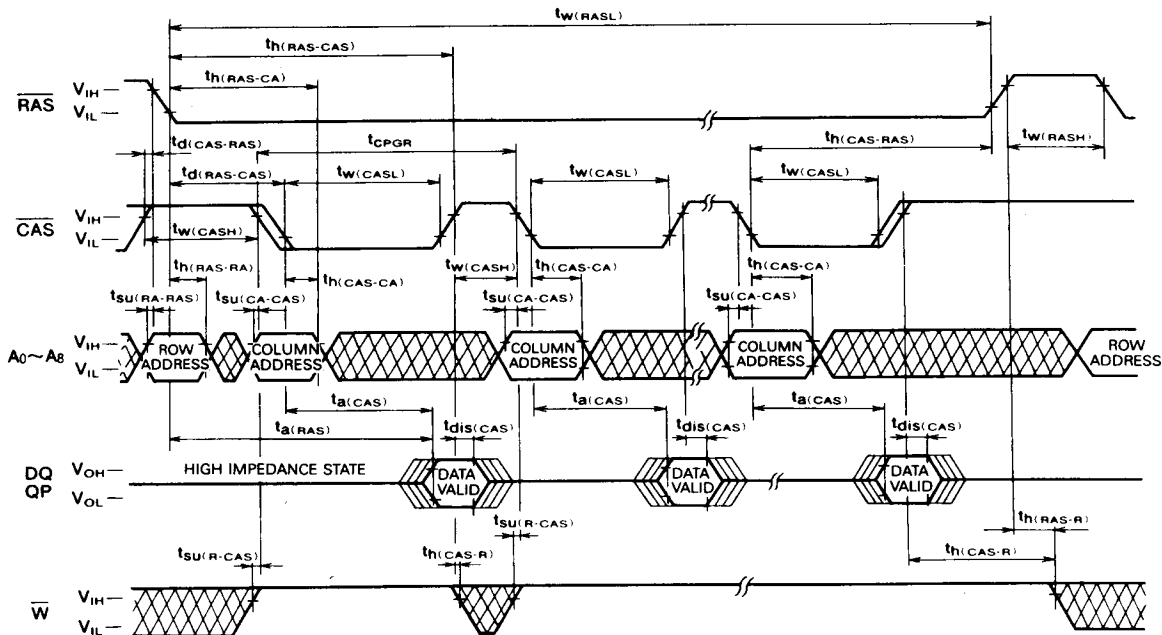


Note 17: Indicates the don't care input.
 The center-line indicates the high-impedance state.

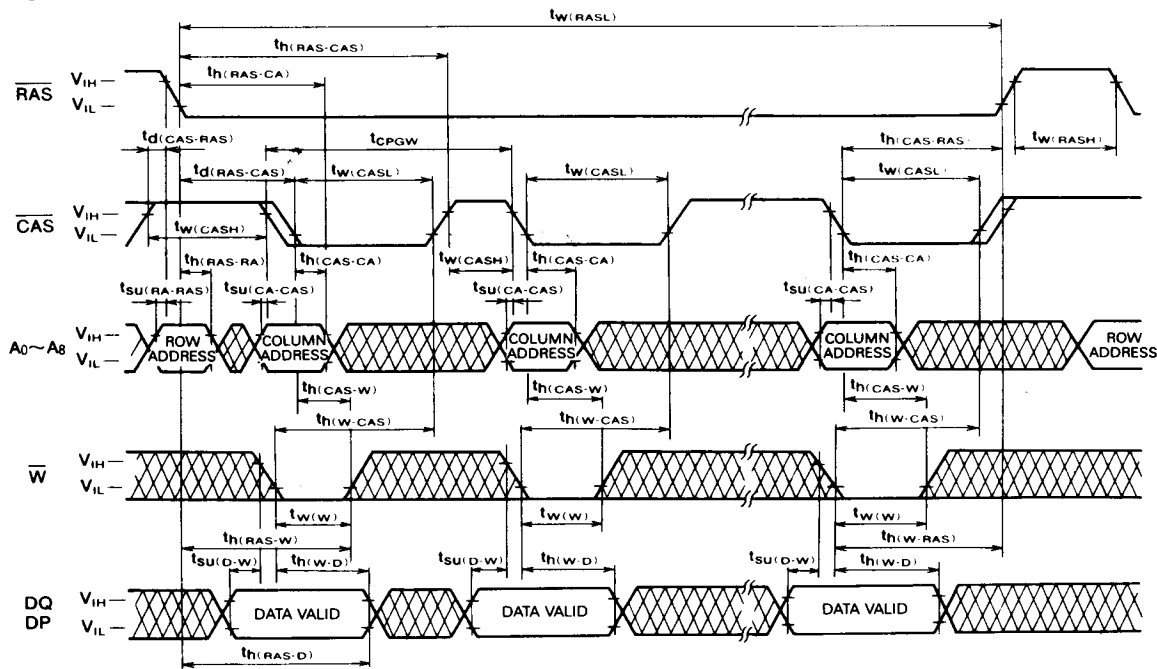
Note 18: $\overline{CAS} = V_{IH}$, \overline{W} , $D =$ don't care.
A8 may be V_{IH} or V_{IL} .



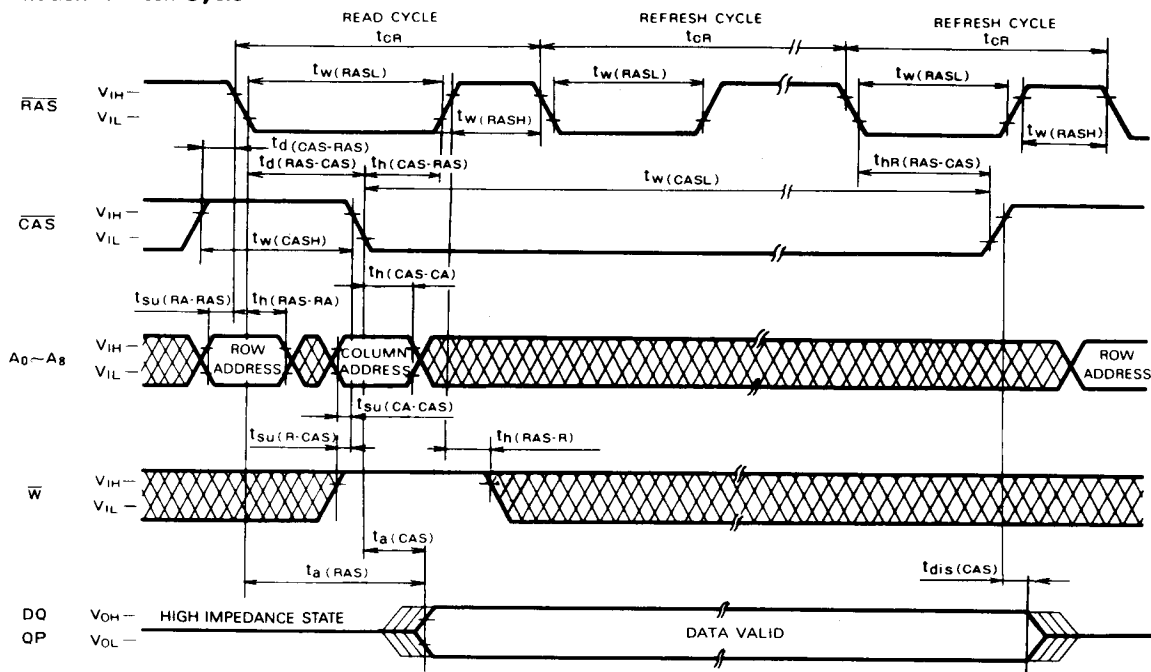
Page-Mode Read Cycle



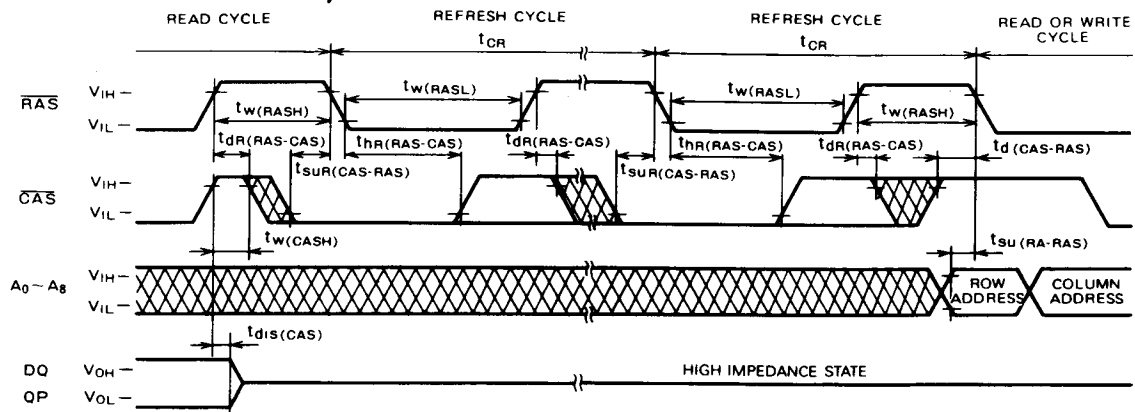
Page-Mode Write Cycle



Hidden Refresh Cycle



\overline{CAS} before \overline{RAS} Refresh Cycle (Note 19)



Note 19 \overline{W} , D = don't care.