Pulse-Width Modulator

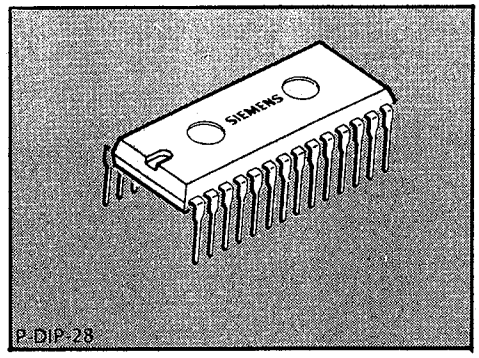
SLE 4520

Preliminary Data

MOS IC

Features

- Digital sine synthesis for controlling the speed and torque of three-phase motors
- 2-chip solution (e.g. SAB 8051 with SLE 4520) for easy configuration of a powerful frequency converter.
- Motor frequencies from 0 to 3 kHz selectable at a switching frequency up to 23.4 kHz
- Adaptation to different output stages through programmable dead time.
- Functional and performance features determined by dedicated software.



Type	Ordering Code	Package
SLE 4520	Q671000-H8271	P-DIP-28

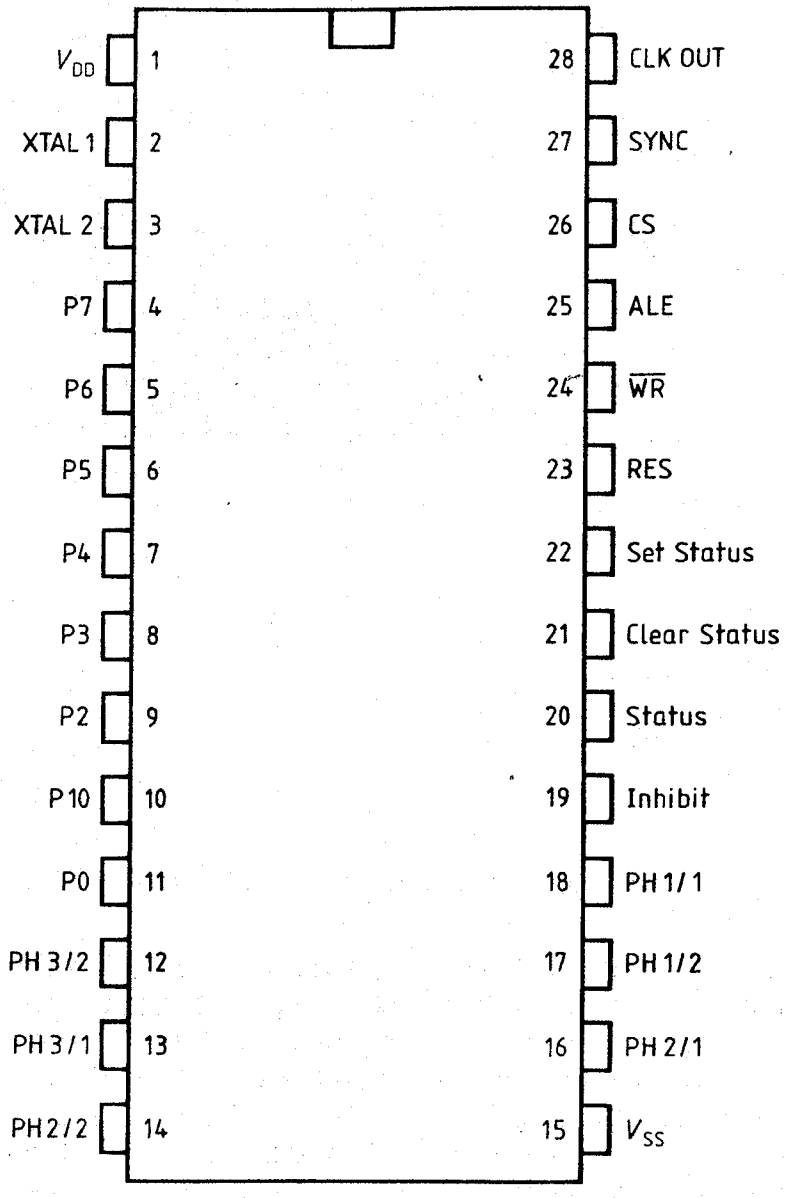
Application

The new pulse-width modulator (PWM) converts an 8-bit data word into a rectangular signal of corresponding width.

Three independently operating channels consisting of a latch, loadable counter and zero detector are used for this purpose. Together with a microcontroller (e.g. SAB 8051) and suitable software, pulses are generated to drive AC converters and inverters (three-phase) with an almost unlimited range of waveforms (sinusoidal, triangular) and phase relationships. An oscillator with clock output, a programmable prescaler to adapt the switching frequency to the requirements of the output stage, an interlocking stage with status flipflop and the ability to program dead times are features that recommend the SLE 4520 for use in frequency converters to drive three-phase induction motors.

Speed control of three-phase motors is easily done when such motors are supplied with a three-phase voltage the *V/f* ratio of which is kept almost constant with variable frequency. For the generation of this three-phase voltage a frequency converter is required, which rectifies and filters the AC supply voltage and, subsequently, reconverts it into an AC voltage of another frequency the aid of a drive circuit and three power half-bridges. In order to avoid high losses the output stages operate in switched mode and are driven by rectangular pulses which increase or decrease in width, depending on the waveform of the sinusoidal function. To produce such pulses with a repetition frequency (switching frequency) up to and above the audible range, a drive block consisting of the SAB 8051 microcontroller and the SLE 4520 PWM as a minimum configuration has proved to be best suited to do the job.

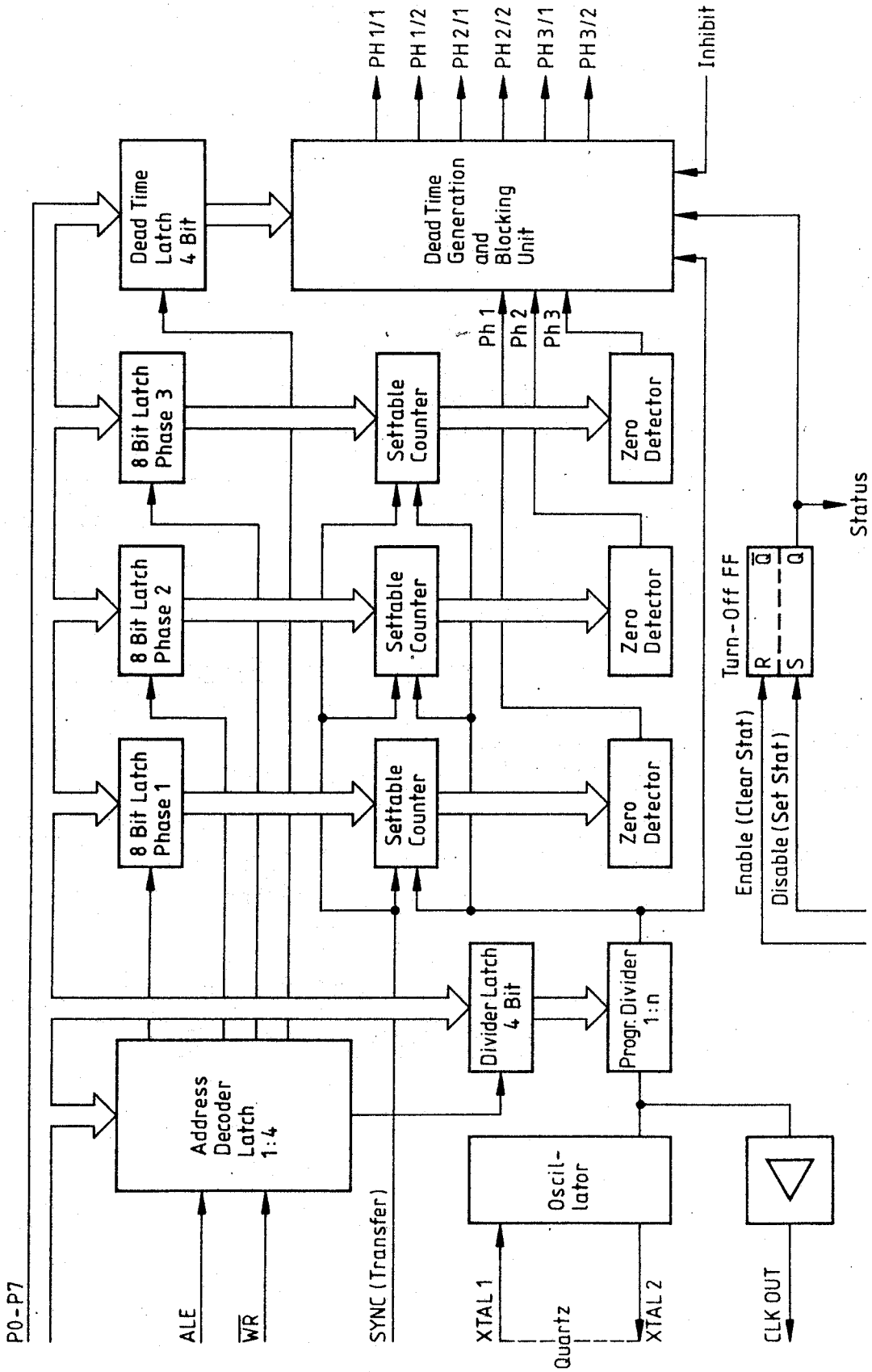
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_{DD}	+5 V pin
2	XTAL1	Crystal pin
3	XTAL2	Crystal pin
4	P7	Data bus pins (inputs)
5	P6	
6	P5	
7	P4	
8	P3	
9	P2	
10	P10	
11	P0	
12	PH 3/2	Output phase 3 inverted
13	PH3/1	Output phase 3 normal (active low)
14	PH2/2	Output phase 2 inverted
15	V_{SS}	Ground
16	PH2/1	Output phase 2 normal (active low)
17	PH1/2	Output phase 1 inverted
18	PH1/1	Output phase 1 normal (active low)
19	INHIBIT	Inhibit (active high) sets all phase outputs to high
20	STATUS	Output of status flipflop
21	CLEAR STATUS	Resets status flipflop
22	SET STATUS	Sets status flipflop
23	RES	Chip reset
24	$\overline{WR}$	Input for $\overline{WR}$ pulse from microcontroller
25	ALE	Input for ALE clock from microcontroller
26	CS	Chip select
27	SYNC	Input for trigger pulse from microcontroller
28	CLK OUT	Output crystal frequency for microcontroller

Block Diagram



Functional Description

The following description deals with the combination of the SAB 8051 microcontroller and the SLE 4520 PWM and a program developed by Siemens. Other hardware combinations are possible as well.

An on-chip oscillator directly feeds the programmable prescaler and has a buffered output for the connected microcontroller. The interface to the microcontroller has a width of 8 bits.

Data from the SAB 8051 microcontroller to the SLE 4520 PWM are transferred via the data bus P0 using the control signals $\overline{ALE}$ and $\overline{WR}$. In the PWM component three 8-bit registers for the three phases and two 4-bit registers for dead time and divider ratio respectively as well as an address decoder latch to buffer the relevant addresses are connected to the internal data bus of the SLE 4520 **(see block diagram)**.

Addresses are as follows:

Address	Register
00	8-bit register for phase 1
01	8-bit register for phase 2
02	8-bit register for phase 3
03	dead time control register
04	divider control register

The last two registers have to be written only once when being initialized. In the case of a controller output the above-mentioned 3-bit address is latched and decoded with the falling edge of the ALE clock. With the rising edge of the $\overline{WR}$ signal data are loaded from the bus into the registers of the pulse-width modulator.

The required divider ratio for the production of low switching frequencies at a simultaneously high operating frequency of the microcontroller is set by the divider control register. The divider control register is best loaded with an adequate value in the starting routine.

Allocation of value and divider ratio is shown in table 1:

Table 1

Allocation of value in the divider register to the divider ratio by which the SLE 4520 operating frequency is selected

Value	Divider ratio Counter	Divider ratio Delay clock
0	1:4	1:4
1	1:6	1:6
2	1:8	1:4
3	1:12	1:6
4	1:16	1:4
5	1:24	1:6
6	1:32	1:4
7	1:48	1:6

After the ratio has been determined, the length of the switching frequency cycle should be selected in such a way that the maximum pulse width is just reached. This means that with a PWM counter clock of, e.g. 1 MHz (oscillator frequency of 12 MHz, divider ratio 1:12) and a table value of 127 (7 bits) the counter reaches zero after 128 µs (switching frequency cycle 128 µs).

Table 2 gives a number of useful allocations of counter frequency and switching frequency for the SAB 8051 (12 MHz clock).

Table 2

Allocation of counter frequency and switching frequency of SAB 8051

Divider ratio	Counter frequency	Operating time Timer 0	Switching frequency	Resolution
1:6	2 MHz	64 µs	15.6 kHz	7 bit
1:6	2 MHz	128 µs	7.8 kHz	8 bit
1:12	1 MHz	128 µs	7.8 kHz	7 bit
1:12	1 MHz	256 µs	3.9 kHz	8 bit
1:24	500 kHz	256 µs	3.9 kHz	7 bit
1:24	500 kHz	2 x 256 µs	1.95 kHz	8 bit
1:48	250 kHz	2 x 256 µs	1.95 kHz	7 bit
1:48	250 kHz	4 x 256 µs	975 Hz	8 bit

Converting a data word into a pulse width

Pulse generation in the three processing channels is done by a presettable 8-bit down-counter and a zero detector (NOR gate) which is connected to the eight counter outputs. With the transfer pulse from the microcontroller (width 1 instruction cycle), whose repetition rate determines the length of the switching frequency, the presettable counter is loaded with the contents of the appropriate register and 0 appears at the zero detector's output (provided the register does not contain 00H).

This 0 digit enables the counter and starts it running down. When zero is reached the pulse ends and the counter is stopped until the next transfer pulse arrives. The crystal frequency multiplied by the divider ratio serves as clock frequency for the PWM counter.

Functional Description

Dead-time control register and dead-time setting in order to avoid overlapping switching operations

The dead time between the drive pulses for the two transistors of a half-bridge must consider the storage times of the bipolar driver and the power transistors, otherwise dangerous overlapping switching operations might occur. In the pulse-width modulator the dead time is obtained by linking the pulse-width modulated signal source with a delay signal. The delay is obtained by passing the source signal through a 15-bit shift register with 15 outputs.

The shift pulse is either $\frac{f_{CRYSTAL}}{6}$ or $\frac{f_{CRYSTAL}}{4}$, depending on the values in the divider control register.

By writing a value between 0 and 0FH into the appropriate control register 16 dead times are presettable (incl. zero dead time)

The dead time depends on the crystal frequency and the preset divider ratio. Programmable dead times for a 12-MHz crystal frequency are shown in **table 3.**

Table 3

Dead times presettable in the dead time control register using divider ratios of 1:4 and 1:6

Word in dead time memory	Divider ratio 1:4 dead time (µs)	Divider ratio 1:6 dead time (µs)
0	0	0
1	0.33	0.5
2	0.66	1
3	1.0	1.5
4	1.33	2
5	1.66	2.5
6	2.0	3
7	2.33	3.5
8	2.66	4
9	3.0	4.5
10	3.33	5
11	3.66	5.5
12	4.0	6
13	4.33	6.5
14	4.66	7
15	5.0	7.5

9

Functional Description

The interface to the power circuit is provided by outputs PH1/1 to PH3/2

Without dead time PH1/2 is inverted to PH1/1, PH2/2 to PH2/1 and PH3/2 to PH3/1. The active switching state is Low.

With a programmed dead time the negative edges of the output signal are shifted to the right by the dead time.

The outputs are capable of directly driving TTL devices or optocouplers for voltage isolation of drive block and power circuit with a current up to 20 mA.

Static or dynamic interlocking of outputs is possible

Within the duration of the inhibit signal (pin 19) all six outputs can be set to high level. In case the outputs are connected to optocouplers the light emitting diodes are currentless and all six individual transistors of the power circuit are blocked. This option is particularly necessary when switching on the drive block, as proper pulses at the pulse-width modulator output are only available after the oscillator output has been built up and the initilization routine has been executed.

As the SAB 8051 sets the port outputs to high when switched on, only one port pin of the microcontroller has to be connected to inhibit. At the end of the initialization routine this port pin is set to low.

Another way of inhibiting the outputs (hold function) is to apply a high pulse to the "Set" input (pin 22) of the status flipflop. This inhibit state is indicated by the "Status" output (pin 20) and can be used to indicate or inform the microcontroller (active high; used, for example, in the event of power failure, short circuit, overtemperature etc.).

The status flipflop is cleared by a high pulse at the "Clear Status" input (pin 21).

Features

- Generation of three pairs of pulse-width modulated rectangular pulses (phase angle between one phase and the next is, for example, 120°) to drive six individual transistors of an inverter power block.
- Programmable dead time to reliably drive both power switches of a half-bridge from

  0 to 15 x $\frac{6}{f_{crystal}}$ or 15 x $\frac{4}{f_{crystal}}$ in 15 steps.

  It is the negative edge which is in each case delayed because the output signal is active low.
- Programmable divider in the pulse-width modulator to obtain low switching frequencies (for output stages with thyristors, GTOs, and bipolar transistors) and to simultaneously operate the microcontroller at higher crystal frequencies.
- Direct drive of an optocoupler interface to isolate control and load circuits ($I_{sink} = 20$ mA maximum).
- All six outputs of the SLE 4520 are set to high level either dynamically by an inhibit signal (INHIBIT) or statically by an R-S flipflop (SET STATUS). Thus blocking of all six individual transistors of the power circuit is possible.
- DC braking by selecting different, fixed duty cycles in the three output pairs.
- Direction of rotation is software-reversed by changing between two phases.
- Sine-wave frequency range about 0 to > 2600 Hz.
- Switching frequency range < 1 to > 20 kHz.
- 8-bit resolution of the desired sine-wave function with a switching frequency of $\frac{f_{crystal}}{6 \times 2^8}$

  or 7 bits with a switching frequency of $\frac{f_{crystal}}{6 \times 2^7}$ ($f_{crystal}$ = 12 MHz and resolution = 7 bits result in a 15.6 kHz switching frequency).
- Smallest increment of the pulse-width is 333 ns with $f_{crystal}$ = 12 MHz and divider ratio 1:4.
- Changing the switching frequency cycle in 1-µs steps allows the transition from one sine-wave frequency stage to the next quasi continuously (virtually analog).
- Evaluating the bit pattern at one port of the microcontroller enables many (256) different speed-control programs to be selected.
- Low current consumption of the pulse-width modulator due to ACMOS technology.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	typ.	max.	Unit
Supply voltage	V_{DD}	−0.3		6	V
Input voltage	V_I	−0.3		V_{DD} +0.3	V
Storage temperature	T_{stg}	−50		125	°C
Total power dissipation	P_{tot}			500	mW
Power dissipation per output	P_Q			50	mW

Operating Range

Supply voltage	V_{CC}	4.5	5	5.5	V
Supply current (outputs not connected)	I_{DD}			15	mA
Operating frequency	f_{CLK}			12	MHz
Ambient temperature	T_A	−40		85	°C

DC Characteristics

$T_A = 25\,°C$

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
All Input Signals Except XTAL2						
H-input voltage	V_{IH}	2.2		V_{DD}	V	
L-input voltage	V_{IL}	0		0.8	V	
Input capacitance	C_I			10	pF	
Input current	I_{IL}			1	µA	
Input Signal XTAL2 for External Clock						
H-input voltage	V_{IH}	4.0			V	
L-input voltage	V_{IL}	0		0.3	V	
Input capacitance	C_I			10	pF	
Input current	I_{IL}			1	µA	
Output Signals STATUS, CLK OUT						
H-output voltage	V_{QH}	V_{DD}−0.8			V	$I_Q = 0.5$ mA
L-output voltage	V_{QL}			0.4	V	$I_Q = 1.6$ mA
Output Signals PH 1/1, PH 1/2, PH 2/2, PH 3/1, PH 3/2						
L-output voltage	V_{QL}			1	V	$I_Q = 20$ mA
H-output voltage	V_{QH}	V_{DD}−0.8 V			V	$I_Q = 1$ mA

9

AC Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{LHLL}	100		ns
Address setup to ALE	t_{AVLL}	30		ns
Address hold after ALE	t_{LLAX}	30		ns
WRN pulse width	t_{WLWH}	200		ns
WRN high to ALE high	t_{WHLH}	50		ns
Data setup after WRN low	t_{DVWL}		20	ns
ALE low to WRN low	t_{LLWL}	100		ns
Data hold after WRN[1)]	t_{WHQX}	30		ns
Oscillator period	t_{OSC}	83		ns
High time	t_{OSCH}	35		ns
Low time	t_{OSCL}	35		ns
SYNC pulse width	t_{YHYL}	200		ns
INHIBIT low to output enable	t_{ILOE}		100	ns
Delay between SYNC high to output active	t_{YHOA}	4 t_{OSC}	97 t_{OSC} +20	ns
Chip select setup to ALE low	t_{CHLL}	20		ns
Chip select hold after WRN high	t_{WHCL}	30		ns
Reset pulse width	t_{RHRL}	12 t_{OSC}		ns
Set Status pulse width	t_{SHSL}	200		ns
Clear Status pulse width	t_{CHCL}	200		ns
INHIBIT high to output disable	t_{IHOD}		100	ns
Set Status high to output disable	t_{SHOD}		100	ns
Clear Status high to output enable	t_{CHOD}		100	ns
Set Status pulse length	t_{SHTH}	100		ns
Clear Status pulse length	t_{CHTL}	100		ns
Inhibit pulse length	t_{IHIL}	100		ns

1) If t_{WLWH} is less than 2 t_{OSC} +20 ns, then t_{WHQX} is 50 ns

Pulse Diagrams