APPLICATION NOTES

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3-PHASE POWER CONVERTER FOR INDUCTION MOTORS

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A newly developed integrated pulse-width modulator and fast switching power FETs are the key components in a converter design which allows the good control characteristics of DC motors to be achieved with the more versatile 3-phase motor.

The most widely used three-phase motor is the squirrel cage type. Its features are well known. Having no commutator or brushes, it gives a long service life and runs very quietly. As there is no brush arcing, RFI suppression is not required. Because of the three-phase rotating field the motor has high starting and pull-out torque, is overload-proof and takes very little space. The rotational speed is determined solely by the operating frequency and the number of pole pairs in a given type. In rated operation, slip speed is negligible in view of the operating frequency. A three-phase power source is necessary to operate the motor. Line frequencies being low, like 50 Hz, allow only low motor speeds.

Advantages of converter-fed three-phase motors

Converters are designed to generate a three-phase AC voltage from a DC source. If the three-phase voltage is variable in frequency and amplitude and supplies a three-phase motor the above-mentioned operating characteristics of the motor will be extended considerably. Speed is controllable over a wide range corresponding to the frequency variations. A drive capable of handling 0 to 600 Hz has been built and is described here. Used with a two-pole motor this frequency would allow 36,000 rpm. The motor is controllable by its freely selectable rated frequency, in other words, upon starting, the slip frequency is low and thus the multiple starting current can be reduced to the rated value. Furthermore, it is possible to produce a defined excess starting torque or to generate a torque at standstill, e.g. to keep a robot's arm suspended in a fixed position. Reversing the direction of rotation is likewise facilitated. This is usually achieved by reversing the connections of two motor windings. In converter operation only the control pulses are interchanged by software instructions. Almost unlimited control applications are possible if the control logic of the converter is made part of the whole electronic drive system and programmed sequences or measured values are used to control the motor.

These advantages apply to both synchronous and induction motors. The converter-fed three-phase motor is ideal for drives which require

- long operating times,
- high speed,
- variable rpm,
- frequent reversing cycles,
- low-noise, maintenance-free operation.

Typical applications of variable-frequency AC inverters are: pumps, fans, machine tools, robots, spinning machines, vehicles and washing machines.

The three-phase voltage supplied from the converter to the motor is not sinusoidal

Figure 1 shows the principle of the converter design, which is based on the Type SLE4520 3-phase generator. Line AC voltage is rectified by a bridge rectifier and smoothed by a reservoir capacitor. The smoothed DC voltage is called the intermediate circuit voltage.

The three terminals of the three-phase motor are connected to the outputs of the power inverter (in Fig. 1 six SIPMOS transistors). The desired motor

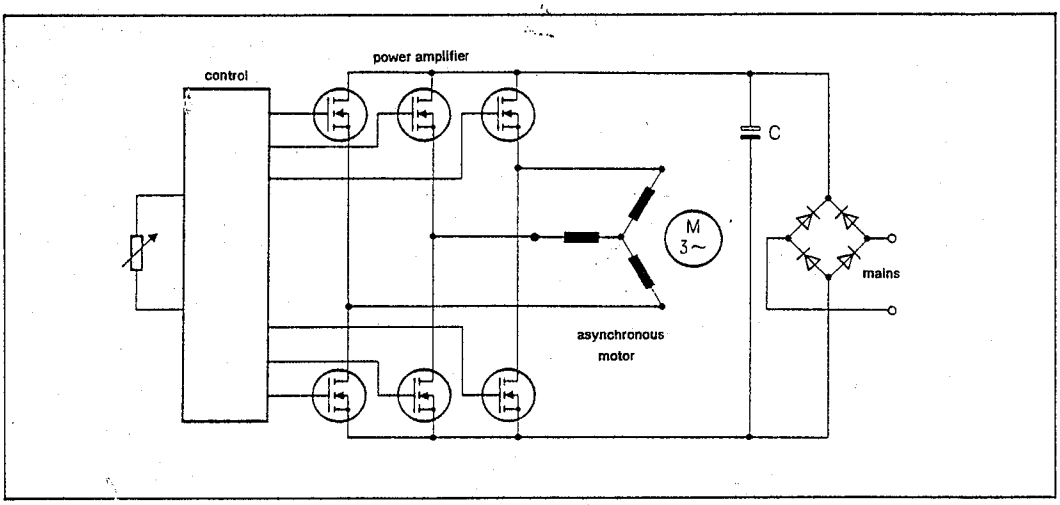

Fig. 1 Main components of a power converter for 3-phase motors.

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frequency is generated in the control block consisting of microcontroller and PWM. Usually, frequency and associated voltage—and thus motor speed—may be selected over a wide range by means of an adjuster. A sinusoidal voltage would increase the power dissipation in the converter to an excessive level. The overall efficiency would be unacceptable. Therefore the undershoot method is applied here. The pulsed voltage applied to each motor winding switches it off at short intervals. On and off times of the pulse sequence are controlled in a way that the average value of all on-cycles represents a sine-wave shape (Fig. 3). This process is called pulsewidth modulation. Since the motor inductance acts as an energy store, current depends on the pulse width of the voltage pulses. Figures 2 and 3 illustrate the process. Figure 2 shows the current flow in a load with a pulse-width modulated supply voltage. It can be seen that the current approaches the ideal sine waveform with increasing number of pulses (synthesis points) used to build up a sine wave. But the pulse-width also determines the current amplitude. Decreasing all pulsewidths in the positive sinusoidal region reduces the amplitude of the synthesized sine-wave voltage by the same factor. With the same load applied less sinusoidal current flows (Fig. 2). A 1:1 duty cycle of the clock frequency for all pulses results in zero current.

The minimum clock frequency depends on the motor inductance. The clock frequency required rises with reduction of inductance. Consequently small motors and high rotational speeds permit high clock frequencies while large motors and low rotational speeds mean low clock frequencies. The selected clock frequency may, however, exceed the required minimum. One synthesis point of a sine-wave consists of several uniform pulses. Often the clock frequency is chosen much higher than necessary to avoid excessive noise (beyond the limit of audibility). The emitted noise primarily depends on the current characteristic. The closer a current curve approaches the ideal sine waveform, the less noise is generated. Too high a clock frequency would certainly restrict the pulse-time variations for an optimum sinusoidal shape.

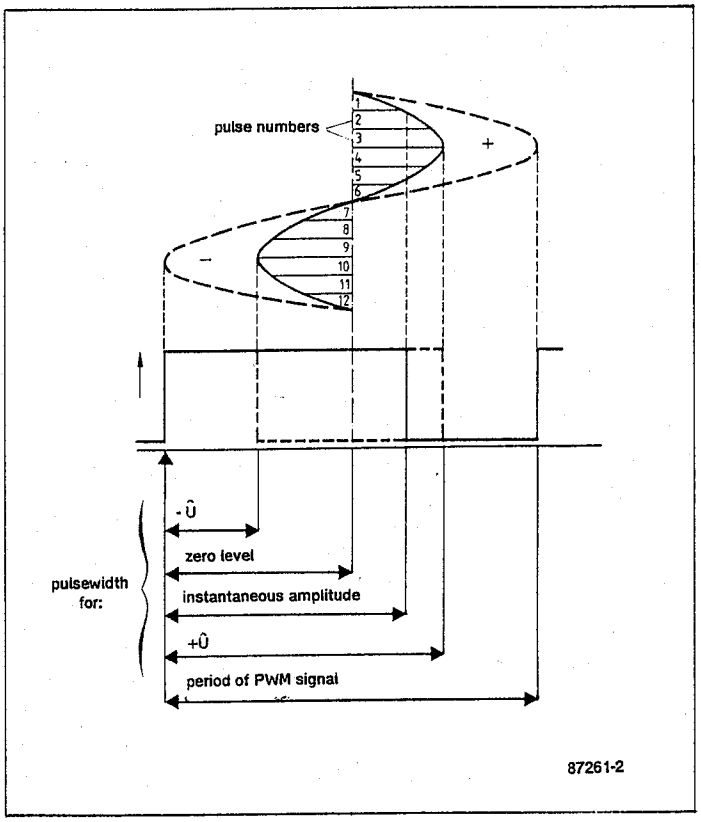

Fig. 2 Principle of pulse-width modulating a sine-wave voltage.

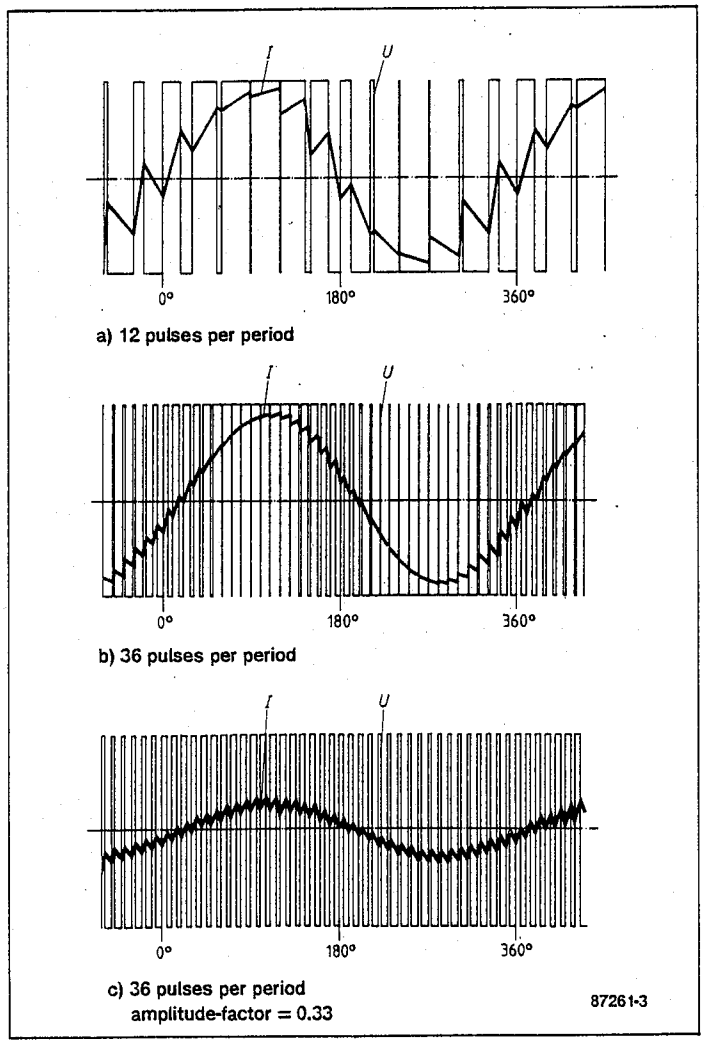

Fig. 3 Illustrating the principle of synthesizing a voltage waveform with the aid of pulse-width modulation. The sine-wave shape of the current waveform is improved by the number of synthesis points (3a; 3b). Current approximation is also possible when the amplitude factor is lower than 1 (3c).

Pulse-width modulation

The principle of pulse-width modulation is shown in Fig. 3. A microcontroller with timer and down counter is needed to modulate pulse widths. Another minimum requirement is a register to pre-load the initial count value and a predivider to adjust the counter frequency in steps. As a register and a counter are required in each phase, they are integrated in the new SLE4520 pulse-width modulator together with some additional functions. Functional description: the initial count value is loaded via the register from the microcontroller to the down counter. The down counter runs down to zero using the predivided CLK frequency (count clock). In this cycle a negative signal is available at the output (Fig. 4). A time signal is generated simultaneously in the timer of the microcontroller. After this interval has lapsed, a transfer pulse (synchronization pulse) is passed to the down counter to start another count down from the initial value from the register. If, meanwhile, the microcontroller has written a new value into the register, the pulse width generated at the output is modified. To obtain a proper pulse-width modulation the down count period has to be equal to or below the transfer pulse sequence initiated by the timer.

The timer determines the clock or switching frequency and the down counter cycle decides the pulse width. Pulse-width modulation for a sine wave is shown in Fig. 2. The sine wave is divided into a number of synthesis points. To each point an amplitude is allocated which corresponds to a particular pulse width. With a pulse width of 50% the average voltage is zero (see Fig. 3), with 100%, the maximum positive voltage and with 0%, the maximum negative voltage is obtained. The switching frequency (e.g. 15 kHz) is usually kept constant to generate a particular sine-wave frequency whereas the pulse width is varied from one synthesis point to another. Values are compiled in a table

within the microcontroller. A continually changing frequency is obtained by appropriately reducing or extending the switching frequency period, or, in other words, the timer interval.

As already mentioned, the sine-wave current to be generated is approximated by a number of synthesis points. Each point corresponds to at least one cycle of the switching frequency. The number of synthesis points for each full sine-wave cycle must be a multiple of six as otherwise a 120° phase displacement cannot be achieved for three-phase operation.

For the sinusodial frequency the following formula applies:

$$f_T = \frac{f_s}{SN}$$

where

f_T = synthesized sine-wave frequency (motor frequency),
f_S = switching frequency,
S = number of synthesis points,
N = number of equal pulses per synthesis point.

The switching frequency is determined by the timer interval in the microcontroller. The timer frequency of the microcontroller used here is 1 MHz. A maximum of 256 μs time interval results for the 8-bit timer corresponding to a 3.9-kHz switching frequency. For higher switching frequencies the timer is counted to below 8 bits with time steps of 1 μs being achieved. For a desired frequency of 20 kHz, for example, 50 steps = 50 μs have to be programmed. The maximum synthesized sine-wave frequency is obtained at a high switching frequency with six synthesis points per period (roughly) and one pulse per point:

$$f = \frac{15.625\ \text{kHz}}{6 \times 1} = 2604\ \text{Hz}$$

There are hardly any objections to generating extremely low sine-wave frequencies as the number of synthesis points and pulses per point may be almost unlimited, e.g.

$$f = \frac{3906.25\ \text{Hz}}{240 \times 100} = 0.16\ \text{Hz}$$

If a generated sine-wave frequency is to be varied, minor a major frequency changes may be performed by reducing or increasing the number of synthesis points or pulses per point with a given switching frequency.

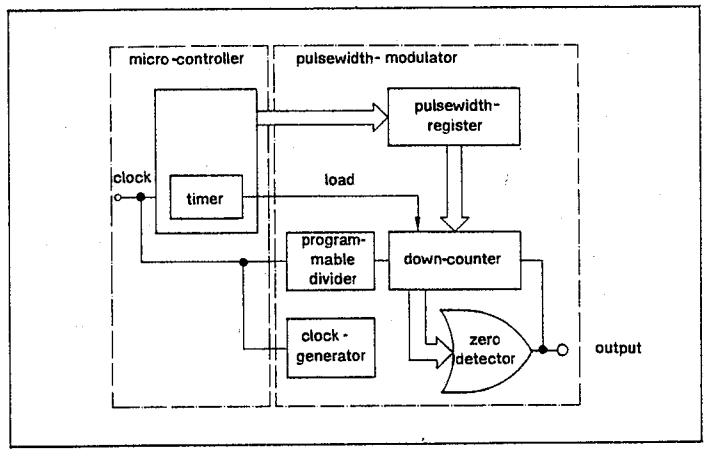

Fig. 4 General organization of a pulse-width modulator with "intelligent" control.

The SLE4520

The SLE4520 pulse-width modulator is a control device which reads the data provided by the microcontroller and converts them into pulse-width modulated clock pulses for three phases driving the power half-bridges via intermediary stages. The SLE4520 is compatible with all kinds of microcontrollers and suitable for all types of three-phase motors because of its large variety of selectable clock frequencies and pulse widths. Fig. 5 shows the block diagram of the SLE 4520 PWM. The IC is operated at the crystal frequency of an on-chip oscillator which may also clock the microcontroller. The operating frequency (or count frequency) is generated via a programmable divider. The available divisors 4, 6, 8, 12, 16, 24, 32 or 48 and the dead time delay are archieved by loading a number into the divider control register and into the appropriate dead-time register. Dead time is a delay required in case the halfbridge transistors exhibit excessive switching delays. Here the delay has to be compensated by decreasing the number of control pulses. The SLE4520 has two outputs for each phase to control individually the upper and lower transistors in the halfbridge. Output pulses may be delayed by a programmable dead time to prevent simultaneous switching of the halfbridge transistors, thus eliminating the risk of a short-circuit. This is particularly important for bipolar switching transistors but also if the power transistors have to be driven via a voltage isolating optocoupler susceptible to delays.

In the SLE4520 pulse-width modulator up to 16 dead time intervals can be generated from 0 to 15 × 4 (or 6)/f_{CLK} in steps of 4 (or 6)/f_{CLK}. At zero dead time both output pulses of one phase are in inverse to each other without any delay. Data are transferred to the pulse-width modulator by writing into phase registers 1, 2 and 3 via the 8-bit data bus P0 and the address decoder latch. At one output the 3-bit address is decoded and latched at the falling edge of the ALE clock until the data are available at the bus together with the $\overline{WR}$ signal.

The transfer pulse for the register is produced by an AND-logic operation from the $\overline{WR}$-signal and the address stored. The pulse-width modulated signal is generated by a zero decoder and a presetable 8-bit down counter which can be stopped via an enable input. The transfer pulse (one instruction cycle) of the processor determining the switching frequency loads the register contents into the presetable counter and a "1" appears at the 8-bit OR gate output. This 1 digit enables the counter and causes it running down. Upon reaching zero the pulse ends and the counter is

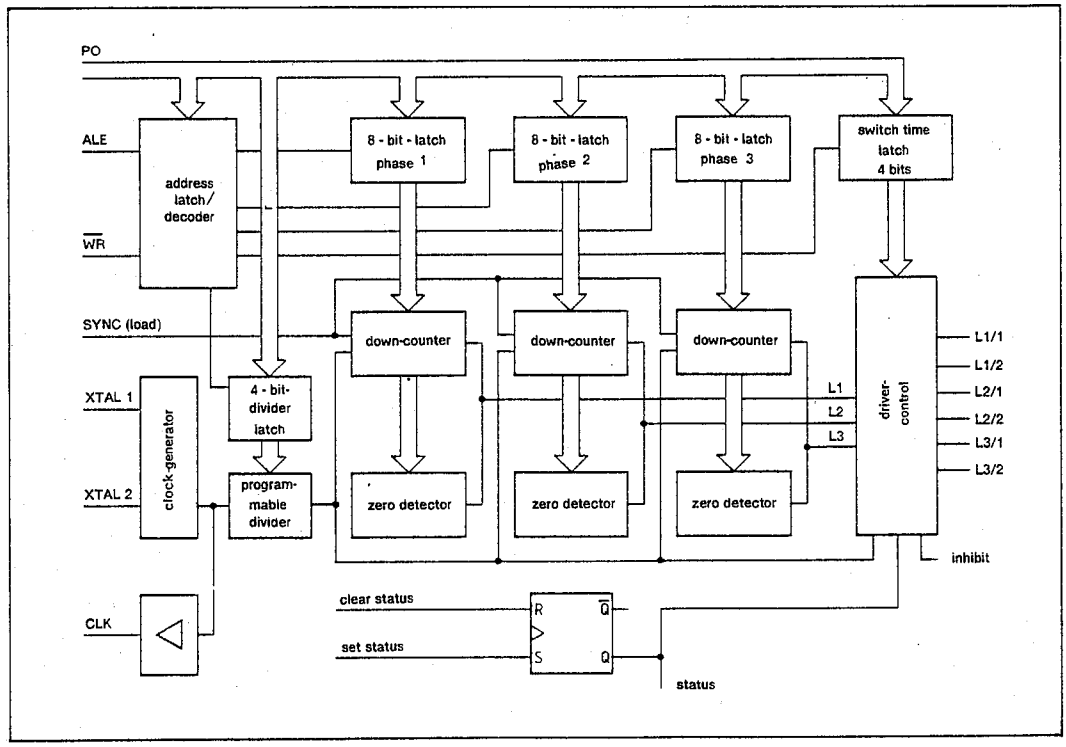

Fig. 5 Internal organization of the Type SLE4520 PWM controller for 3-phase systems.

Table 1

Value	divider ratio counter	divider ratio delay clock
0	1:4	1:4
1	1:6	1:6
2	1:8	1:4
3	1:12	1:6
4	1:16	1:4
5	1:24	1:6
6	1:32	1:4
7	1:48	1:6

Table 1 Allocation of value in the divider register to the divider ratio by which the SLE4520 operating frequency is selected.

Table 2

Word in dead time memory	Divider ratio 1:4 dead time (μs)	Divider ratio 1:6 dead time (μs)
0	0	0
1	0.33	0.5
2	0.66	1
3	1.0	1.5
4	1.33	2
5	1.66	2.5
6	2.0	3
7	2.33	3.5
8	2.66	4
9	3.0	4.5
10	3.33	5
11	3.66	5.5
12	4.0	6
13	4.33	6.5
14	4.66	7
15	5.0	7.5

Table 2 Dead time presettable in the relevant register using divider ratios of 1:4 and 1:6.

Table 3

3-bit address	latch
00	8-bit latch for PH1
01	8-bit latch for PH2
02	8-bit latch for PH3
03	dead time latch
04	divider latch

Table 3 Addressable latches in the SLE4520.

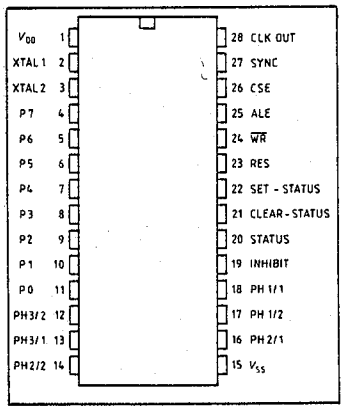

Fig. 6 Pinning of the SLE4520.

stopped until the next transfer pulse arrives.

The SLE4520 has a locking circuit to inhibit all outputs via one inhibit line. This feature is very useful, e.g. if uncontrolled pulses must be withheld from the power stages over the entire settling time of the microcontroller. Furthermore, all output stages and thus the motor can be switched off immediately in critical operating phases caused by overload, over-temperature and external hazardous situations. Via a cut-off flip-flop this locking state is either maintained or cleared. The control output is likewise suitable for indication or feedback to the processor.

To produce low switching frequencies with a simultaneously high microcontroller operating frequency the divider control register is loaded in the initial routine with an appropriate number. Allocation of value and divider ratio is shown in Table 1.

The switching cycle (determined by the initial value in the auto-reload register of the μC) should be selected after the ratio is fixed so as to barely reach the maximum pulse width. This means that with a PWM counter operating clock of, say, 1 MHz (oscillator frequency of 12 MHz, divider ratio 1:12) and a table value of 127 (7 bits) the counter reaches zero after 128 μs.

Table 2 gives a number of useful allocations of counter and switching frequencies for the SAB 8051 (12 MHz clock).

Pulse generation in the three processing channels is done by a presettable 8-bit downcounter and a zero detector (OR gate) which is connected to the eight counter outputs. With the transfer pulse from the microcontroller (width is one instruction cycle) the repetition rate of which determines the switching frequency, the presettable counter is loaded with the contents of the appropriate register and a 1 appears at the zero detector's output (provided the register does not contain 00H). This 1 digit enables the counter and starts it running down. When zero is reached the pulse ends and the counter is stopped until the next transfer pulse arrives. The quartz frequency multiplied by the divider ratio clocks the PWM counter.

In the pulse-width modulator the dead time is obtained by linking the pulse-width modulated source signal and its delayed signal. The delay is obtained by passing the source signal through a 15-bit shift register with 15 outputs. The shift pulse is either $f_{quartz}/6$ or $f_{quartz}/4$, depending on the contents of the divider control register.

To select the delay and the dead time, only one output of the shift register has to be addressed and then switched through to the logic circuit. This is provided by three 1:16 multiplexers. 15 dead times are presettable (incl. zero dead time) by writing a value between 0 and $0F_H$ into the appropriate control register.

Dead time depends on the quartz frequency and the preset divider ratio (1:4 or 1:6). For a 12-MHz quartz frequency the programmable dead times are given in Table 3.

Without dead time PH 1/2 is inverted to PH 1/1, PH 2/2 to PH 2/1 and PH 3/2 to PH 3/1. The active switching state is low: With a programmed dead time the negative edges of the output signal are shifted to the right by the dead time. The outputs are capable of directly driving TTL devices or optocouplers for voltage isolation of drive blocks and power circuits with currents up to 20 mA.

The SLE4520 is a CMOS device, and non-used inputs should, therefore, be connected to ground or the positive supply rail. Finally, Table 4 shows the relation between counter frequency and switching frequency for a SAB8051 microcontroller operating at 12 MHz.

TW

Source:
Siemens Components XXI (1986) Nos. 1 and 2.

Table 4

Divider ratio	Counter frequency	Operating time Timer 0	Switching frequency	Resolution
1:6	2 MHz	64 μs	15.6 kHz	7 bit
1:6	2 MHz	128 μs	7.8 kHz	8 bit
1:12	1 MHz	128 μs	7.8 kHz	7 bit
1:12	1 MHz	256 μs	3.9 kHz	8 bit
1:24	500 kHz	256 μs	3.9 kHz	7 bit
1:24	500 kHz	2 × 256 μs	1.95 kHz	8 bit
1:48	250 kHz	2 × 256 μs	1.95 kHz	7 bit
1:48	250 kHz	4 × 256 μs	975 Hz	8 bit

Table 4 Allocation of the counter frequency and the switching frequency of the SAB8051 microcontroller.

Pin	Description	
1	V_{DD}	+ 5-V connection
2	XTAL1	quartz connection
3	XTAL2	quartz connection
4	P7	
5	P6	
6	P5	
7	P4	input pins to be
8	P3	connected to data bus
9	P2	
10	P1	
11	P0	
12	PH 3/2	output phase 3 inverted
13	PH 3/1	output phase 3 normal (active low)
14	PH 2/2	output phase 2 inverted
15	Vss	ground connection
16	PH 2/1	output phase 2 normal (active low)
17	PH 1/2	output phase 1 inverted
18	PH 1/1	output phase 1 normal (active low)
19	INHIBIT	inhibit (active low) sets all phase outputs to H
20	STATUS	status of status flipflop
21	CLEAR STATUS	resets status flipflop
22	SET STATUS	sets status flipflop
23	RES	chip reset
24	WR	input for WR pulse from microcontroller
25	ALE	input for ALE clock from microcontroller
26	CSE	chip select
27	SYNC	input for carry pulse from microcontroller
28	CLK OUT	output quartz frequency for microcontroller