SIEMENS

Application Note

Pulse Width Modulator IC SLE 4520

With the new pulse width modulator (PWM) SLE 4520, it is possible to convert an 8-bit data word into a rectangular signal of corresponding width.

Three independently operating channels with memory, programmable counter and zero detectors are used for this purpose. In combination with a microcontroller (e.g. SAB 8051) and suitable software, pulses can easily be generated to drive three-phase frequency converters with an almost unlimited range of waveforms (sinusoidal, triangular) and any phase relationship. The device can also be used for inverters.

An oscillator with clock output, a programmable prescaler to adapt the switching frequency to the requirements of the output stage, an interlocking stage with status flipflop and the ability to program dead times are features that recommend the SLE 4520 for use in frequency converters to drive three-phase induction motors.

The following report displays the technical possibilities of this design idea, explains the functional operation and discusses the new component's interfaces. Further the use and handling of the new component from both hardware and software sides is shown and the functional operation in combination with the microcontroller SAB 8051 is explained.

1. Principle of function

Speed control of three-phase motors is easily done when such motors are supplied with a three-phase voltage the voltage/frequency ratio of which is kept nearly constant with variable frequency. To generate this three-phase voltage a frequency converter is required to rectify and filter the ac supply voltage and subsequently re-convert it into an ac voltage of different frequency by a drive circuit and three power half bridges **(Fig. 1)**. To avoid high losses the output stages operate in a switched mode and are driven by rectangular pulses which increase or decrease in width, depending on the waveform of the sinusoidal function. To produce such pulses with a repetition frequency (switching frequency) up to the limit of the audible range, a drive circuit has proved to be advantageous, which in the simplest case consists of the microcontroller SAB 8051 and the pulse width modulator SLE 4520.

2. Technical feasibility of the system configuration consisting of SAB 8051/SLE 4520 combination

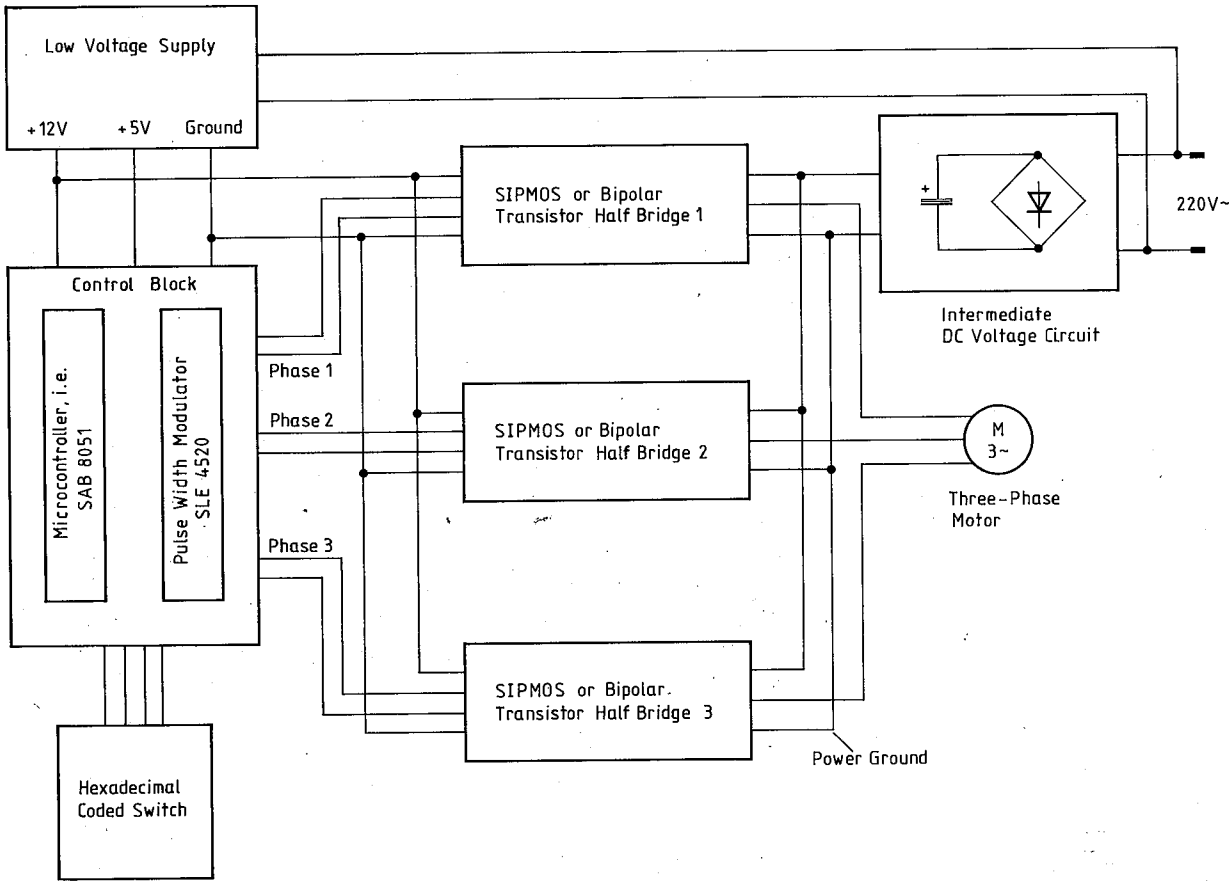
- Generation of three pairs of pulse-width modulated rectangular pulses (phase angle between one phase and the next is, for example, 120°) to drive six individual transistors of an inverter power stage.
- Programmable dead time to safely drive both power switches of a half bridge from 0 to $15 \cdot \frac{6}{f_{crystal}}$ or $15 \cdot \frac{4}{f_{crystal}}$ in 15 steps. The negative edge is always delayed because the output signal is active LOW.
- Programmable divider in the pulse width modulator to obtain low switching frequencies (bipolar transistor output stages) and at the same time to operate the microcontroller at higher crystal frequencies.
- Direct drive of an optocoupler interface to isolate control and load circuits (I_{sink} = 20 mA maximum).
- All six outputs of the SLE 4520 are set to HIGH level either dynamically by an inhibit signal (INHIBIT) or statically by an R-S flipflop (SET STATUS). Thus blocking of all six individual transistors of the power circuit is possible.
- DC braking is possible by selecting different fixed duty cycles on the three output pairs.
- Direction of rotation is reversed by software by exchanging two phases.
- Sine-wave frequency range between approx. 0 Hz and 2600 Hz.
- Switching frequency range between 1 kHz and 20 kHz.
- Resolution of desired sine-wave function:

  8 bits with a switching frequency of $\frac{f_{crystal}}{6 \cdot 2^8}$ or

  7 bits with a switching frequency of $\frac{f_{crystal}}{6 \cdot 2^7}$

  Example: With a resolution of 7 bits and a crystal frequency of $f_{crystal}$ = 12 MHz a switching frequency of 15.6 kHz results.

Fig. 1 Block diagram of a three-phase converter



- The smallest change in the pulse width is 333 ns with $f_{crystal}$ = 12 MHz and divider ratio 1:4.
- Changing the switching frequency cycle in 1-μs steps allows the transition from one sine-wave frequency stage to the next quasi continuously (virtually analog).
- Evaluating the bit pattern at one port of the microcontroller SAB 8051 enables many (256) different speed control programs to be selected.
- Output frequency amplitudes are allocated by filing a corresponding table in the program (table size = number of steps × 3) or by linking a table to the output values of an A/D converter.
- Low current consumption of the pulse width modulator because of ACMOS technology.

3. Description of the functional blocks of the pulse width modulator (PWM) SLE 4520

After listing the technical possibilities the substantial functional blocks of the PWM **(Fig. 2)** are described, based on a combination with the microcontroller SAB 8051 and an in-house developed program. However, in principle other hardware and software combinations can be used as well.

3.1 On-chip oscillator

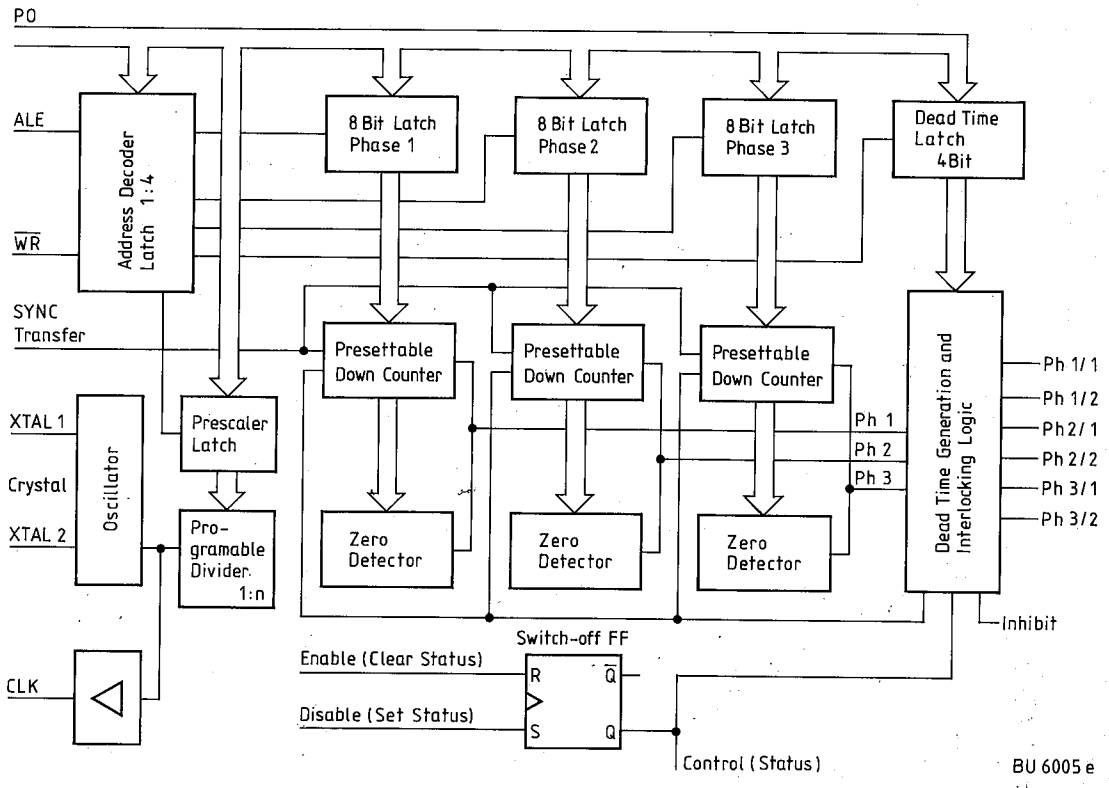
As oscillations from the crystal of the microcontroller do not permit further processing by digital circuits, an oscillator is integrated on the PWM. This feeds the programmable prescaler and has a buffered output for the connected microcontroller. Additional capacitors at the crystal terminals become unnecessary.

3.2 Interface to the microcontroller

Data from the SAB 8051 microcontroller to the SLE 4520 pulse width modulator are transferred via the data bus P0 using control signals ALE and WR. Three 8-bit registers for the three phases and two 4-bit registers to preset dead time and prescaler ratios, as well as an address decoder latch to buffer particular addresses, are connected to the data bus of the SLE 4520.

Transmission of a value is initiated by the instruction MOVX @R0, A (SAB 8051) with the external address being loaded into the R0 register and the data value to be transferred in the accumulator.

Fig. 2 Block diagram of pulse width modulator SLE 4520



Allocations are as follows:

Address (3 bits)	Register
00	8-bit register for phase 1
01	8-bit register for phase 2
02	8-bit register for phase 3
03	dead time control register
04	divider control register

The last two registers have to be written only once when initialized. In the case of a controller output the above mentioned 3-bit address is latched and decoded with the falling edge of the ALE clock. With the rising edge of the $\overline{WR}$ signal data are loaded from the bus into the registers of the pulse width modulator.

3.3 Divider control register

The desired divider ratio is set with the divider control register. Hence, the divider control register is loaded in the initial routine with an appropriate value to produce low switching frequencies with a simultaneously high microcontroller operating frequency. Allocation of the value in the divider register, with which the operating frequency of the SLE 4520 is selected, is shown in **Table 1**.

Table 1 Allocation of value and divider ratio

Value	Divider ratio down counter	Divider ratio delay clock
0	1:4	1:4
1	1:6	1:6
2	1:8	1:4
3	1:12	1:6
4	1:16	1:4
5	1:24	1:6
6	1:32	1:4
7	1:48	1:6

The switching cycle (run time of the timer 0, determined by the initial value in the auto-reload registers TH0 of the microcontroller) should be selected after the divider ratio for the down counter is fixed so as to barely reach the maximum pulse width. This means that with a PWM counter operating clock of, say, 1 MHz (oscillator frequency of 12 MHz, divider ratio 1:12) and a table value of 127 (7 bits) the counter reaches zero after 128 μs. Reload register TH0 for timer 0 in the microcontroller has to be written in this case with 80 H (switching frequency cycle 128 μs).

Table 2 gives the useful allocation of counter and switching frequencies for the SAB 8051 (12 MHz crystal).

Fig. 3 Control stage of the converter using SAB 8031 microcontroller and external EPROM

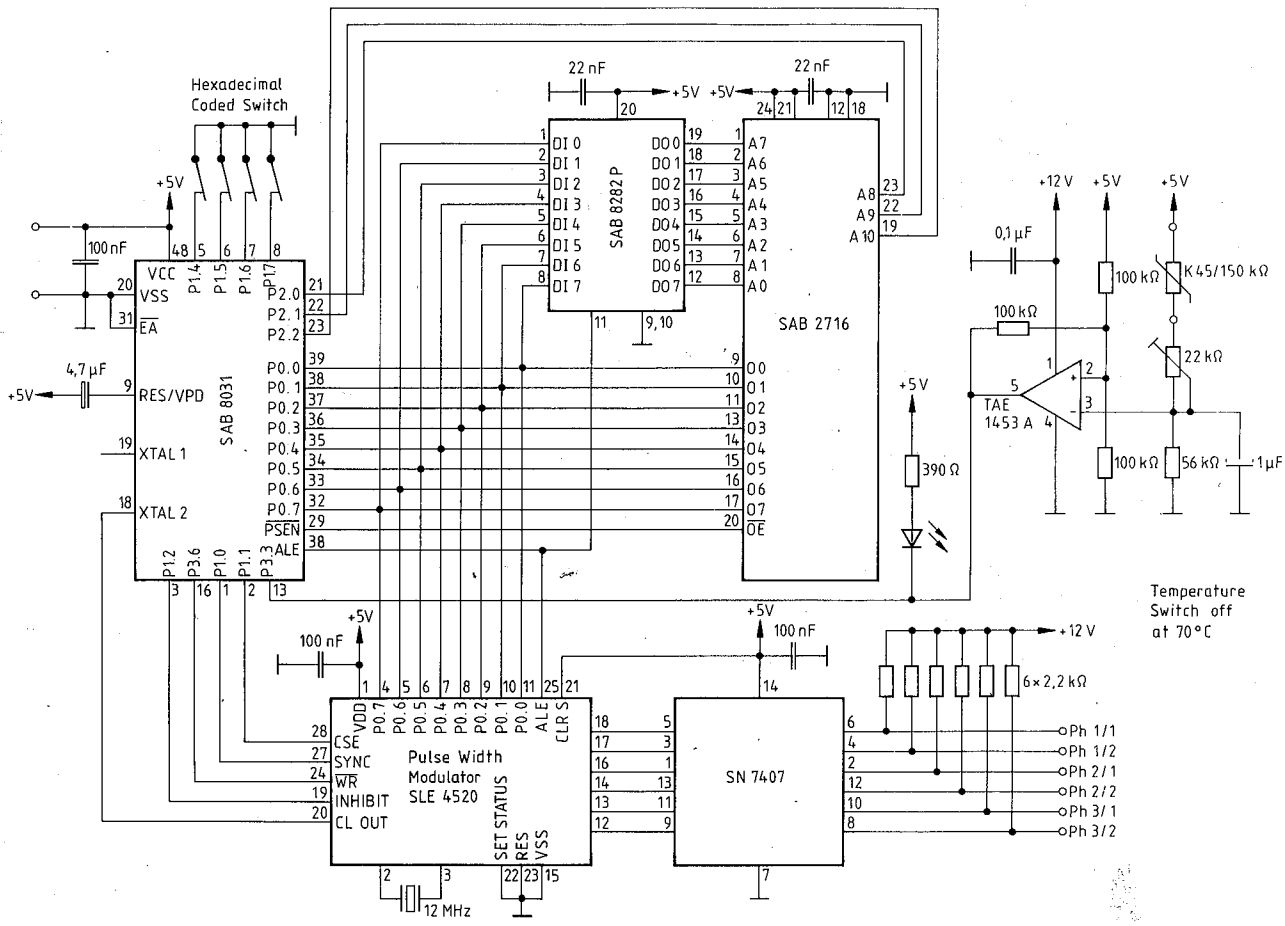


Table 2 Allocation of counter and switching frequency of SAB 8051

Divider ratio down counter	Counter frequency	Run time Timer 0	Switching frequency	Resolution
1:6	2 MHz	64 μs	15.6 kHz	7-bit
1:6	2 MHz	128 μs	7.8 kHz	8-bit
1:12	1 MHz	128 μs	7.8 kHz	7-bit
1:12	1 MHz	256 μs	3.9 kHz	8-bit
1:24	500 kHz	256 μs	3.9 kHz	7-bit
1:24	500 kHz	2×256 μs	1.95 kHz	8-bit
1:48	250 kHz	2×256 μs	1.95 kHz	7-bit
1:48	250 kHz	4×256 μs	975.0 Hz	8-bit

3.4 Conversion of data word into pulse width

Pulse generation in the three processing channels is done by a presettable 8-bit down counter and a zero detector (OR gate) which is connected to the eight counter outputs. With the transfer pulse from the microcontroller (width is one instruction cycle) the repetition rate of which determines the switching frequency, the presettable counter is loaded with the contents of the appropriate register and a 1 appears at the zero detector's output (provided the register does not contain 00H).

This 1 digit enables the counter to count down. When zero is reached the pulse ends and the counter is stopped until the next transfer pulse arrives. The crystal frequency multiplied by the divider ratio clocks the PWM down counter.

3.5 Dead time control register and dead time generation

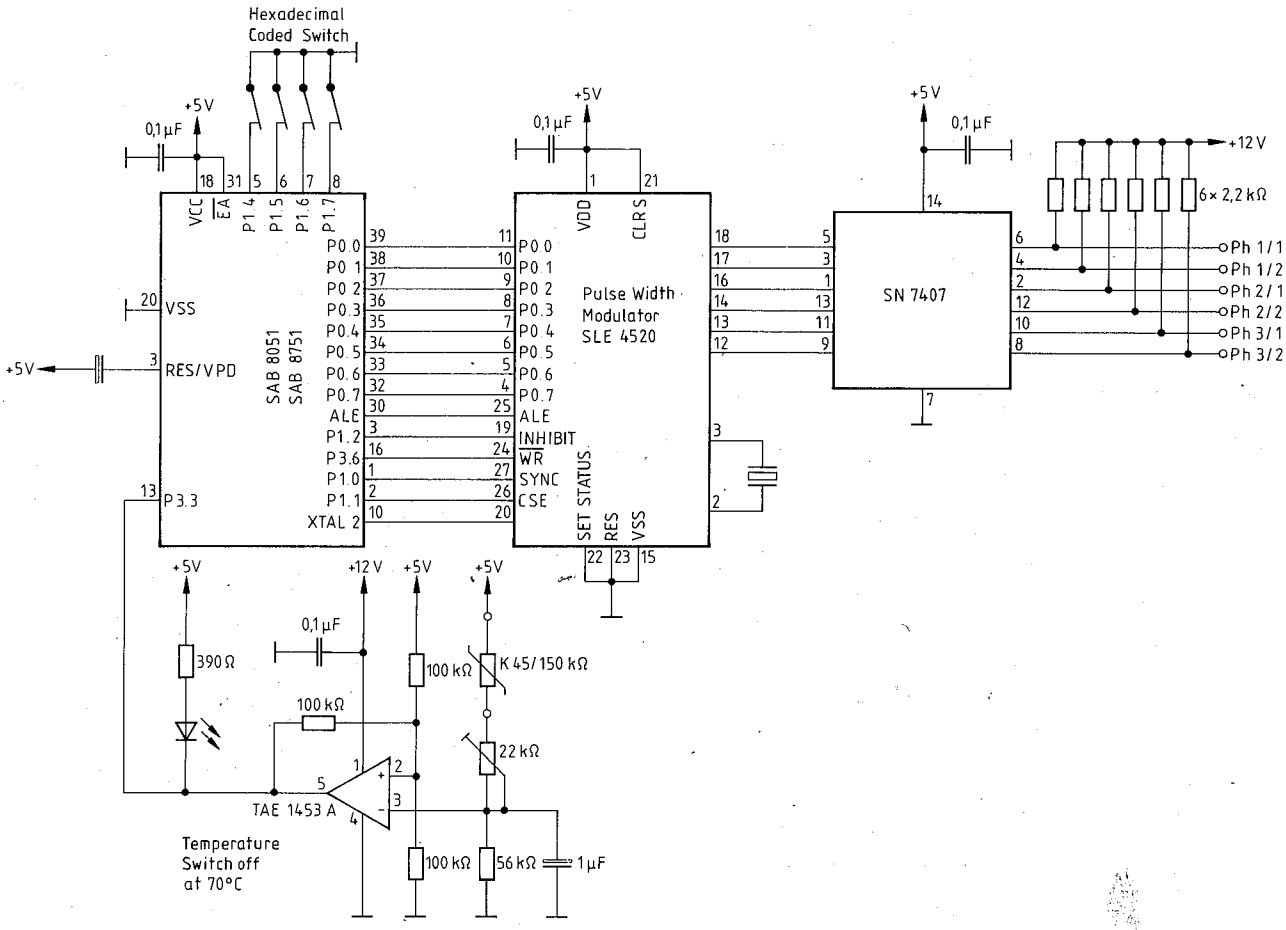
Each half bridge contains two transistors. The dead time is defined as the period of time between the conducting state of one transistor in a half bridge and the blocking state of the other transistor and vice versa.

The dead time between the drive pulses for the two transistors of a half bridge should take into account the storage times of the bipolar driver and power transistors to prevent dangerous overlapping of switching operations ("shoot-trough"). In the pulse width modulator, the dead time is obtained by linking the pulse-width-modulated source signal logically with a delayed signal. The delay is obtained by passing the source signal through a 15-bit shift register with 15 outputs. The shift pulse is either

$$\frac{f_{crystal}}{6} \text{ or } \frac{f_{crystal}}{4}$$

(depending on the contents of the divider control register, according to table 1).

Fig. 4 Application example of connection to a TTL driver



To select the delay and thus the dead time only one output of the shift register needs to be addressed and then switched through to the logic circuit. This is provided by three 1:16 multiplexers.

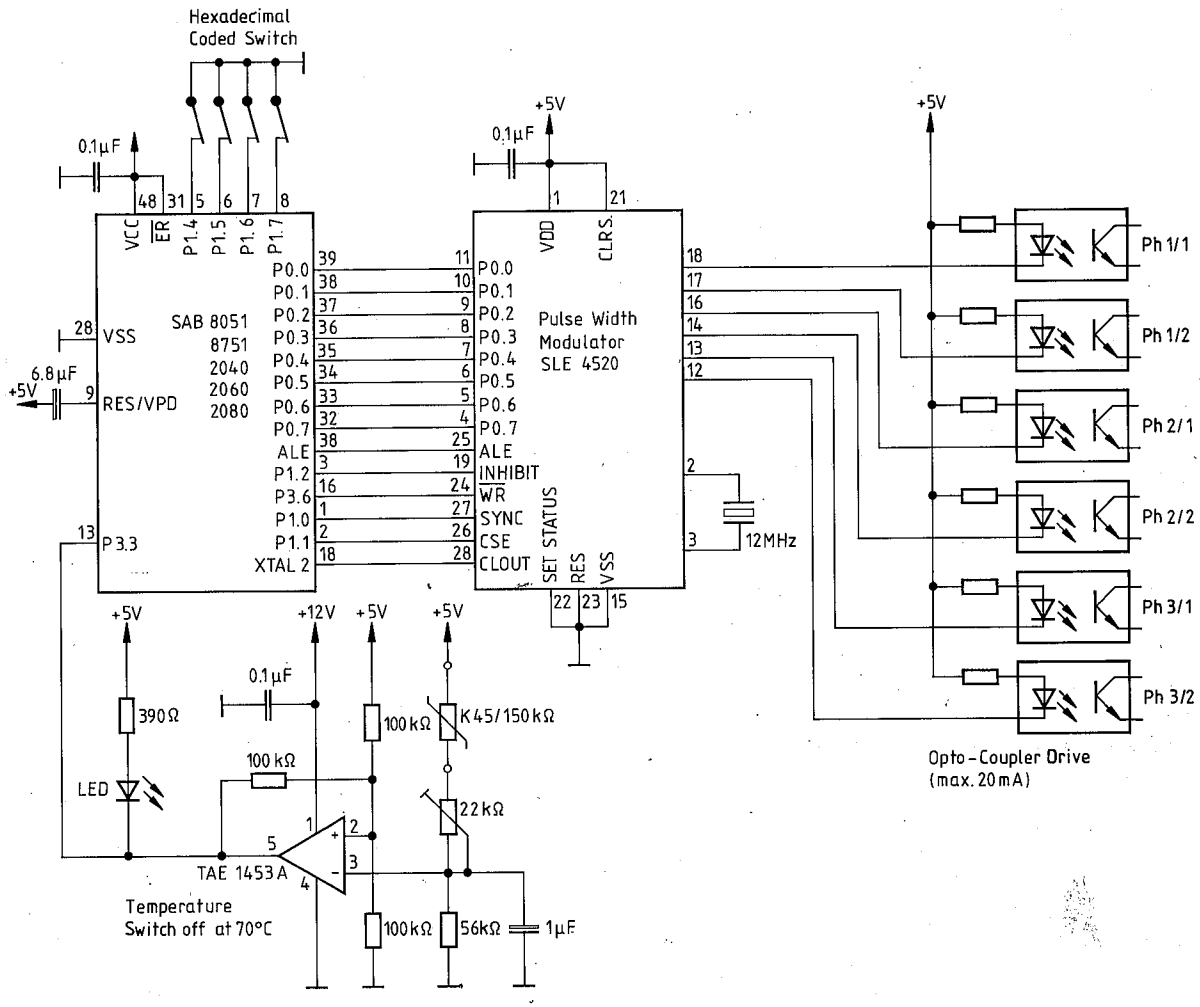
15 dead times are presettable (incl. zero dead time) by writing a value between 0 and 0FH into the appropriate control register.

The dead time depends on the crystal frequency and the preset divider ratio of the delay clock (1:4 od 1:6). For a 12-MHz crystal frequency the following dead times apply:

Table 3 Dead times set in the dead time control register with divider ratios of 1:4 and 1:6

Word in dead time memory	Dead time [µs] at divider ratio 1:4	1:6
0	0	0
1	0.33	0.5
2	0.66	1
3	1.0	1.5
4	1.33	2
5	1.66	2.5
6	2.0	3
7	2.33	3.5
8	2.66	4
9	3.0	4.5
10	3.33	5
11	3.66	5.5
12	4.0	6
13	4.33	6.5
14	4.66	7
15	5.0	7.5

Fig. 5 Connecting the pulse width modulator SLE 4520 to the microcontroller SAB 8051 or SAB 8751



3.6 Interface to the power stage

The interface to the power stage is provided by outputs Ph 1/1 to Ph 3/2. Without dead time Ph 1/2 is inverted to Ph 1/1, Ph 2/2 to Ph 2/1 and Ph 3/2 to Ph 3/1. The active switching state is LOW.

With a programmed dead time the negative edges of the output signal are shifted to the right by the period of the dead time.

The outputs are capable of directly driving TTL devices or optocouplers for voltage isolation of the drive block from the power stage with a current of up to 20 mA.

3.7 Interlocking of the outputs

All six outputs can be set to HIGH level during the inhibit signal (pin 19). Hence the light emitting diodes of the connected optocouplers are currentless and all six individual transistors of the power circuit are blocked. This option is particularly useful when switching on the drive block as clean pulses at the pulse width modulator output are available only after the start up of the oscillator and the initialization routine has been executed.

As the SAB 8051 sets the port outputs to HIGH on switching, only one pin of the microcontroller port needs to be connected to inhibit. At the end of the initialization routine this port pin is set to LOW.

Another way of inhibiting the outputs (hold function) is to apply a High pulse to the SET input (pin 22) of the status flipflop. This inhibit state is indicated by the "Status" output (pin 20) and can be used to indicate or inform the microcontroller (active High; used, for example, in the event of power failure, short circuit, excess temperature etc.). The status flipflop is cleared by a High pulse at the "Clear Status" input (pin 21).

4. Application examples

Figs. 3 through 5 show how the PWM SLE 4520 should be connected to the ROMless microcontroller SAB 8031, or the EPROM version SAB 8751 or to the mask-programmable version SAB 8051.

Unused inputs must be set to defined levels (HIGH or LOW), as the SLE 4520 is a CMOS device.

5. Initialization of the drive block (see listing 1)

The initialization routine is started with a jump instruction at the beginning of the program. Subsequently the vector addresses for the four interrupts are allocated and – if required – identified with the branch destination. During the initialization routine the applied registers are set to a starting value and the stack register and the operating mode of timer 0 and timer 1 are defined.

The number 12 H in the TMOD register indicates that the timer 1 will operate as a 16-bit timer and timer 0 as an 8-bit timer in the auto reload mode.

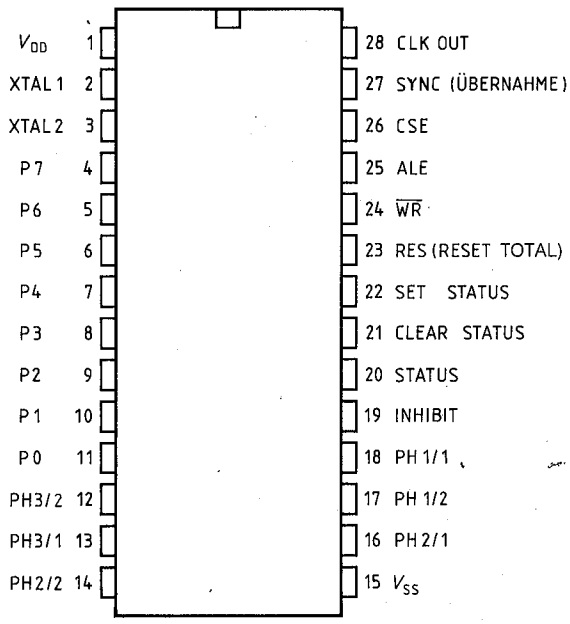
By writing 8EH into the IE register the interrupt sources timer 0, timer 1, and the external interrupt 1 are enabled individually or simultaneously. High priority is assigned to the interrupt of timer 0 and the external interrupt INT1 by setting PX1 and PT0 in the IP register. Subsequently, the registers in the PWM for the three phases, for the dead time and the divider ratios, for the down counter and the delay clock will be addressed and written.

After the DPT has been loaded with the initial value of the table address for amplitude 0, the registers 10 H and 11 H have received an initial value, and the debounce and reset flags are set, the subroutine "SABFR" (interrogation of switch) is implemented in order to determine and evaluate the switch status. The auto reload register TH0 for timer 0 is then loaded with the number which corresponds to the switching frequency cycle (0C0H = 64 μs). The low byte of timer 0, on the other hand, is loaded with a number for rapid overflow and the TCON register is written.

The number 55 H indicates that timer 0 and timer 1 will start and that an edge interrupt has been provided for the external interrupt INT1.

The last instruction enables the PWM, since in our example P1.2 has been connected to RES1.

Fig. 6 Pin configuration



7. Pin description

PIN	Description	Function
1	V_{DD}	+ 5 V connection
2	XTAL1	Crystal connection
3	XTAL2	Crystal connection
4	P7	Data bus connections (inputs)
5	P6	
6	P5	
7	P4	
8	P3	
9	P2	
10	P1	
11	P0	
12	PH3/2	Output phase 3 inverted
13	PH3/1	Output phase 3 normal (active low)
14	PH2/2	Output phase 2 inverted
15	V_{SS}	Ground connection
16	PH2/1	Output phase 2 normal (active low)
17	PH1/2	Output phase 1 inverted
18	PH1/1	Output phase 1 normal (active low)
19	INHIBIT	Inhibit (active high) sets all phase outputs to H
20	STATUS	Status of status flipflop
21	CLEAR STATUS	Resets status flipflop
22	SET STATUS	Sets status flipflop
23	$\overline{RES}$	Chip reset
24	$\overline{WR}$	Input for WR pulse from microcontroller
25	ALE	Input for ALE clock from microcontroller
26	CSE	Chip select
27	SYNC	Input for transfer pulse from microcontroller
28	CLK OUT	OUTPUT crystal frequency for microcontroller

6. Table access and output based on the SAB 8051 example (listing 2)

Two registers and the DPT register are required for a continuous output of the table values to the phase registers of the connected PWM.

The required command sequence is as follows:
MOV R0, # address phase register
MOV A, R4
MOVC A, @ A + DPTR
MOVX@R0, A

To generate the table address, the table value counter R4 is added as index to the table start address contained in the DPT register.

By incrementing R0 and R4 the above command sequence fetches and transfers the values for phase 1 through 3. It is therefore required that the values for phase 1 through 3 for a certain angle are listed in successive order in the table.

The table therefore lists triple the number of steps.

Listing 1

```
;Initialization

                CSEG    AT 0
                SJMP    INIT
                ORG     03H         ;START WITH EXT. INTERRUPT INT0
                ORG     0BH         ;START WITH TIMER 0 INTERRUPT
                AJMP    TINTO       ;TIMER 0 INTERRUPT ROUTINE
                ORG     013H        ;START WITH EXT. INTERRUPT INT1
                ORG     01BH        ;START WITH TIMER 1 INTERRUPT
                AJMP    TINT1               ;TIMER 1 INTERRUPT ROUTINE
                ORG     26H

INIT:   CLR     P1.0                ;FOR TEST PURPOSES
        CLR     A                   ;REGISTER INITIALIZATION
        MOV     20H,A               ;CLEAR FLAG 0 TO 7
        MOV     21H,A               ;CLEAR FLAG 8 TO 15
        MOV     R0,A                ;ADDRESS REGISTERS FOR THE 3 PHASES
        MOV     R1,A                ;LATCH FOR STARTING ADDRESS OF TABLE
        MOV     R2,A                ;       "       "       "       "
        MOV     R3,A                ;COMPARE REGISTER FOR BCD SWITCH
        MOV     R4,A                ;STEP COUNTER
        MOV     R5,A                ;
        MOV     R6,#01H             ;SET DEBOUNCE COUNTER FOR "DECIDE"
        MOV     R7,#01H             ;PREPARE COUNTER FOR PULSES PER STEP
        MOV     SP,#STACK_START
        MOV     TMOD,#00010010@     ;OPERATING MODE TIMER 0, TIMER 1
        ANL     IE,#01100000B       ;CLEAR PRIORITY INTERRUPT
        ORL     IE,#10001110B       ;ENABLE INTERRUPT FOR T0, T1, INT1
        ANL     IP,#11100000B       ;CLEAR INTERRUPT PRIORITY
        SETB    PX1                 ;HIGHEST PRIORITY FOR INT1
        SETB    PT0                 ;HIGH PRIORITY FOR TIMER 0
        MOV     A,#63D              ;PULSE DUTY FACTOR 1:1
        MOVX    @R0,A               ;WRITE PHASE REGISTER 1
        INC     R0                  ;INCREMENT EXT. ADDRESS
        MOVX    @R0,A               ;WRITE PHASE REGISTER 2
        INC     R0
        MOVX    @R0,A               ;PHASE REGISTER 3
        INC     R0                  ;ADDRESS DEAD TIME LATCH
        MOV     A,#DEAD TIME
        MOVX    @R0,A               ;WRITE DEAD TIME LATCH
        INC     R0                  ;ADDRESS DIVIDER LATCH
        MOV     A,#DIVIDER RATIO
        MOVX    @R0,A               ;WRITE DIVIDER LATCH
        MOV     DPL,#LOW TABLE0
        MOV     DPH,#HIGH TABLE0    ;AMPLITUDE 0
        MOV     11H,#10D            ;10 VALUES ARE PROCESSED
        MOV     10H,#03D            ;ARBITRARY STARTING VALUE
        SETB    DEBOUNCE FLAG
        SETB    RESET FLAG          ;BIT FOR DECIDING CALL OR INT.
        ACALL   SABFR               ;SWITCH INTERROGATION
        MOV     TH0,#0COH           ;SWITCHING FREQUENCY PERIOD =64 µS
        MOV     TL0,#0FCH           ;FOR ACCELERATED T0 OVERFLOW
        MOV     TCON,#01010101B     ;EDGE INTERRUPT FOR INT1, T0, T1 START
        CLR     P1.2                ;ENABLE PWM
        END
```

Listing 2

Output routine for phases 1 to 3 with change in direction

New values for amplitude, sinusoidal frequency, number of steps/period pulses/steps are transferred at the end of a period in the "NLOAD" section.

```
;Interrupt                                    service  routine
                        RSEG                 ;OUTPUT SEGMENT
TINT0:      SETB        P1.0                 ;PULSE FOR EXT. HARDWARE
            CLR         P1.0                 ;END OF PULSE
            PUSH        PSW                  ;SAVE PSW OF MAIN PROGRAM
            PUSH        ACC                  ;AS WELL AS ACCU
            CLR         IE.7                 ;INHIBIT INTERRUPT
            DJNZ        R7, OVER             ;WHEN COUNTER =0 OUTPUT, OTHERWISE OVER
            MOV         R7,10H               ;TRANSFER CONTENTS OF 10 TO REG. R7
            JB          Rwech_flag,RWECH              ;WITH FLAG=1 CHANGE IN DIRECTION
;------- OUTPUT OF 3-PHASE VALUE ----------------------------------------------------------------
            MOV         R0,#0H               ;SET ADDRESS COUNTER FOR EXT. REG. TO ZERO
            MOV         A,R4                 ;LOAD TABLE INDEX INTO ACCU
            MOVC        A,@A+DPTR            ;FETCH SUPPORT VALUE PHASE 1 FROM TABLE
            MOVX        @R0,A                ;OUTPUT SUPPORT VALUE TO PH.-REG. 1
            INC         R0                   ;INCREMENT ADDRESS COUNTER FOR 2ND PHASE
            INC         R4                   ;INCREMENT TABLE INDEX
            MOV         A,R4                 ;FETCH TABLE INDEX
            MOVC        A,@A+DPTR            ;FETCH SUPPORT VALUE PHASE 2 FROM TABLE
            MOVX        @R0,A                ;OUTPUT SUPPORT VALUE TO PH.-REG. 2
            INC         R0                   ;INCREMENT ADDRESS COUNTER FOR 3RD PHASE
            INC         R4                   ;INCREMENT TABLE INDEX
            MOV         A,R4                 ;FETCH TABLE INDEX
            MOVC        A,@A+DPTR            ;FETCH SUPPORT VALUE PHASE 3 FROM TABLE
            MOVX        @R0,A                ;OUTPUT SUPPORT VALUE PH.-REG. 3
            NOP                              ;TIME COMPENSATION FOR OTHER DIRECTION
            NOP
;----------------------------------------------------------------------------------------------
ABFR:       INC         R4                   ;INCREMENT TABLE INDEX
            MOV         A,R4                 ;FETCH TABLE INDEX
            CJNE        A,11H,OVER           ;HAVE ALL STEPS BEEN PROCESSED?
;----------------------------------------------------------------------------------------------
NLOAD:      DEC         09H                  ;TIME COUNTER-1
            JNB         Ueber flag,AWERT              ;NO NEW VALUE WHEN FLAG = 0
            MOV         10H,12H              ;AFTER SWITCH HAS BEEN QUERIED
            MOV         11H,13H              ;VALUE IS TRANSFERRED IN ZERO CROSSOVER
            MOV         TH0,14H              ;TRANSFER OF NEW SWITCHING FREQUENCY
            MOV         DPL,R2               ;TRANSFER OF TABLE
            MOV         DPH,R1               ;START ADDRESS
            CLR         Ueber_flag           ;CLEAR TRANSFER FLAG
            JNB         Aender_flag,FORT              ;FLAG FOR CHANGE IN DIRECTION
            SETB        Rwech_flag                    ;SET DIRECTIONAL FLAG
            SJMP        AWERT
FORT:       CLR         Rwech_flag
AWERT:      MOV         R4,#00H              ;SET STEP COUNTER TO ZERO
OVER:       SETB        IE.7                 ;ENABLE INTERRUPT
            POP         ACC                  ;TRANSFER ACCU
            POP         PSW                  ;AND PSW
            RETI
;------- PROGRAM SECTION FOR DIRECTION ----------------------------------------------------------
RWECH:      MOV         R0,#2H               ;SET ADDRESS COUNTER EXT. REGISTER TO 2
            MOV         A,R4                 ;TABLE INDEX
            MOVC        A,@A+DPTR
            MOVX        @R0,A                ;OUTPUT OF 1ST SUPPORT VALUE TO PH.-REG. 3
            DEC         R0
            INC         R4
            MOV         A,R4
            MOVC        A,@A+DPTR
            MOVX        @R0,A                ;OUTPUT OF 2ND SUPPORT VALUE TO PH.-REG. 2
            DEC         R0
            INC         R4
            MOV         A,R4
            MOVC        A,@A+DPTR
            MOVX        @R0,A                ;OUTPUT OF 3RD SUPPORT VALUE TO PH.-REG. 1
            SJMP        ABFR                 ;QUERY NUMBER OF STEPS
            END
```

To Listing 2:

Definition of the registers and flags listed in the output routine:

R0 = Address counter for phase registers 1, 2 and 3
R1 = Latch for starting address of table (high byte)
R2 = Latch for starting address of table (low byte)
R4 = Index counter for addressing the respective table value
R7 = Counter for determining pulses/steps
10H = Reload register for R7
11H = Contains actual number of table values
12H = Latch for 10 H
13H = Latch for 11 H
14H = Latch for TH0
(12H, 13H, 14H: after switch evaluation and value assignment)
TH0 = Reload register for timer 0 in auto reload mode
bit 32.0 = Direction flag
bit 32.2 = Transfer flag
bit 32.3 = Debounce flag (for switch query)
bit 32.5 = Flag for changing direction
bit IE.7 = Inhibit flag for all interrupts

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