SGS-THOMSON MICROELECTRONICS

ST6210B-ST6215B
ST6220B-ST6225B

8-BIT HCMOS MCUs WITH A/D CONVERTER

PRELIMINARY DATA

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait, Stop Modes
- 5 different interrupt vectors
- Look-up table capability in ROM
- User ROM: 1828 bytes (ST6210B, 15B) 3876 bytes (ST6220B, 25B)
- Data ROM: User selectable size (in program ROM)
- Data RAM: 64 bytes
- ROM readout Protection
- PDIP20, PSO20 (ST6210B, 20B) packages
- PDIP28, PSO28 (ST6215B, 25B) packages
- 12/20 fully software programmable I/O as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull outputs
  - Analog Inputs
- 4 I/O lines can sink up to 20mA for direct LED or TRIAC driving
- 8 bit counter with a 7-bit programmable prescaler
- Digital Watchdog and Oscillator Safe Guard
- 8 bit A/D Converter with up to 8 (ST6210B, 20B) and up to 16 (ST6215B, 25B) analog inputs
- On-chip clock oscillator driven by Quartz Crystal, Ceramic resonator or RC network
- Power-on Reset
- One external not maskable interrupt
- 9 powerful addressing modes
- The development tool of the ST621xB, 2xB microcontrollers consists of the ST626x-EMU emulation and development system connected via an RS232 serial line to an MS-DOS PC

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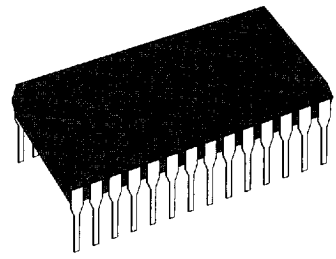
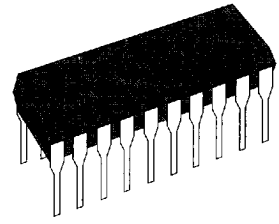
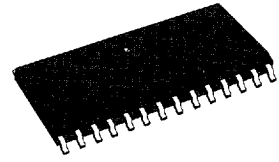


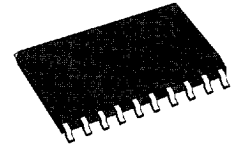
PDIP28



PDIP20



PSO28



PSO20

(Ordering Information at the end of the datasheet)

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September 1994

Figure 1. ST6210B, ST6220B Pin Configuration

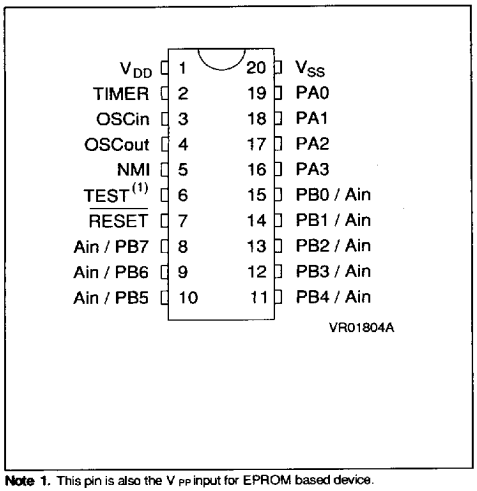
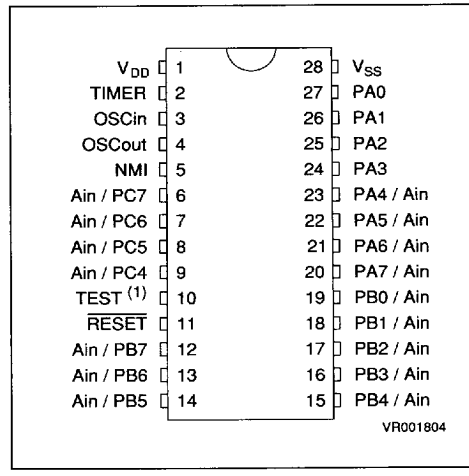
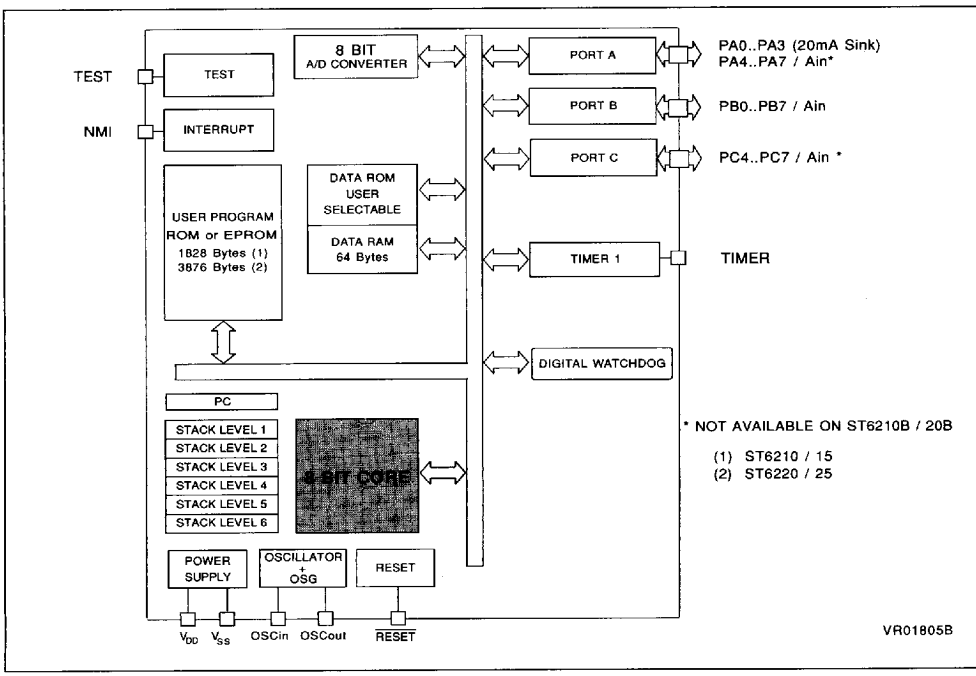


Figure 2. ST6215B, ST6225B Pin Configuration



Note 1. This pin is also the V_{PP} input for EPROM based device.

Figure 3. Block Diagram



GENERAL DESCRIPTION

The ST6210B, ST6215B, ST6220B and ST6225B microcontrollers are members of the 8-bit HCMOS ST62xx family, a series of devices oriented to low-medium complexity applications. All ST62xx members are based on a building block approach: a common core is surrounded by a combination of on-chip peripherals (macrocells).

The macrocells of the ST6210B, 15B, 20B and 25B are: the Timer peripheral that includes an 8-bit counter with a 7-bit software programmable prescaler, the 8-bit A/D Converter with up to 8 (ST6210B, 20B) and up to 16 (ST6215B, 25B) analog inputs (A/D inputs are alternate functions of I/O pins), the Digital Watchdog (DWD).

The ST621xB, 2xB are upward compatible with the ST621x, 2x. They in addition feature enhanced RC oscillator, Oscillator Safe Guard, Readout Protection against Piracy and a new External STOP Mode Control option to enlarge the range of power consumption/safety trade-offs.

These devices are well suited for automotive, appliance and industrial applications. The ST62E20B and ST62E25B EPROM versions are available for prototypes and low-volume production; also OTP versions are available. The only difference between these devices are program memory size and I/O pin number, following the table below.

DEVICE SUMMARY

Device	ROM (Bytes)	I/O Pins
ST6210B	2K	12
ST6215B	2K	20
ST6220B	4K	12
ST6225B	4K	20

PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU using these two pins. V_{DD} is power and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected with the on-chip oscillator circuit. When the QUARTZ/CERAMIC RESONATOR mask option is selected, a quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins. When the RC OSCILLATOR mask option is selected, a resistor must be connected between the pin OSCout and the ground. The OSCin pin is the input pin, the OSCout pin is the output pin.

$\overline{\text{RESET}}$. The active low $\overline{\text{RESET}}$ pin is used to restart the microcontroller to the beginning of its program.

TEST. The TEST must be held at V_{SS} for normal operation (an internal pull-down resistor selects normal operating mode if TEST pin is not connected).

NMI. The NMI pin provides the capability for asynchronous interrupt applying an external not maskable interrupt to the MCU. The NMI is falling edge sensitive.
On ST6210B, 15B, 20B, 25B the user can select as ROM mask option the availability of an on-chip pull-up at NMI pin.

TIMER. This is the timer I/O pin. In input mode it is connected to the prescaler and acts as external timer clock or as control gate for the internal timer clock. In the output mode the timer pin outputs the data bit when a time-out occurs.
On ST6210B, 15B, 20B, 25B the user can select as ROM mask option the availability of an on-chip pull-up at TIMER pin.

PA0-PA3,PA4-PA7. These 8 lines are organized as one I/O port (A). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs. PA0-PA3 can also sink 20mA for direct LED driving while PA4-PA7 can be programmed as analog inputs for the A/D converter.,
Note. PA4-PA7 are not available on ST6210B, ST6220B.

PB0-PB7. These 8 lines are organized as one I/O port (B). When the External STOP Mode Control option is disabled, each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter. When the External STOP Mode Control option is enabled, PB0 output Mode is forced as open-drain (push-pull output is not possible). The other lines are unchanged.

PC4-PC7. These 4 lines are organized as one I/O port (C). When the External STOP Mode Control option is disabled, each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs and as analog inputs for the A/D converter. When the External STOP Mode Control is enabled PC7output Mode is forced as open-drain (push-pull output is not possible) . The other lines are unchanged.
Note. PC4-PC7 are not available on ST6210B, ST6220B.

ST62xx CORE

The core of the ST62xx Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control busses. The in-core communication is arranged as shown in Figure 5; the controller being externally linked to both the reset and the oscillator, while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes through the control registers.

Registers

The ST62xx Family core has six registers and three pairs of flags available to the programmer. They are shown in Figure 4 and are explained in the following paragraphs.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator is addressed in the data space as RAM location at address FFh. Accordingly the ST62xx instruction set can use the accumulator as any other register of the data space.

Indirect Registers (X, Y). These two indirect registers are used as pointers to the memory locations in the data space. They are used in the register-indirect addressing mode. These registers can be

Figure 4. ST62xx Core Programming Model

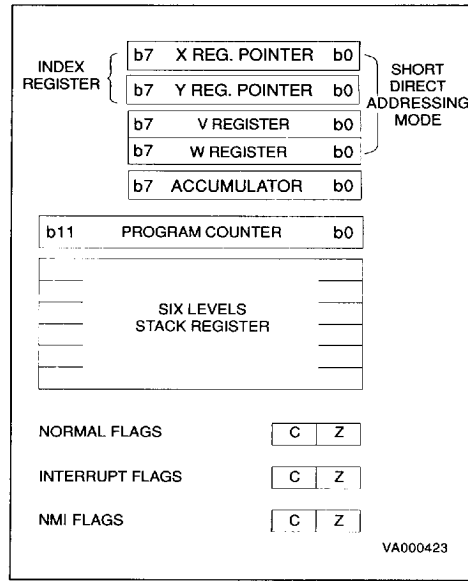
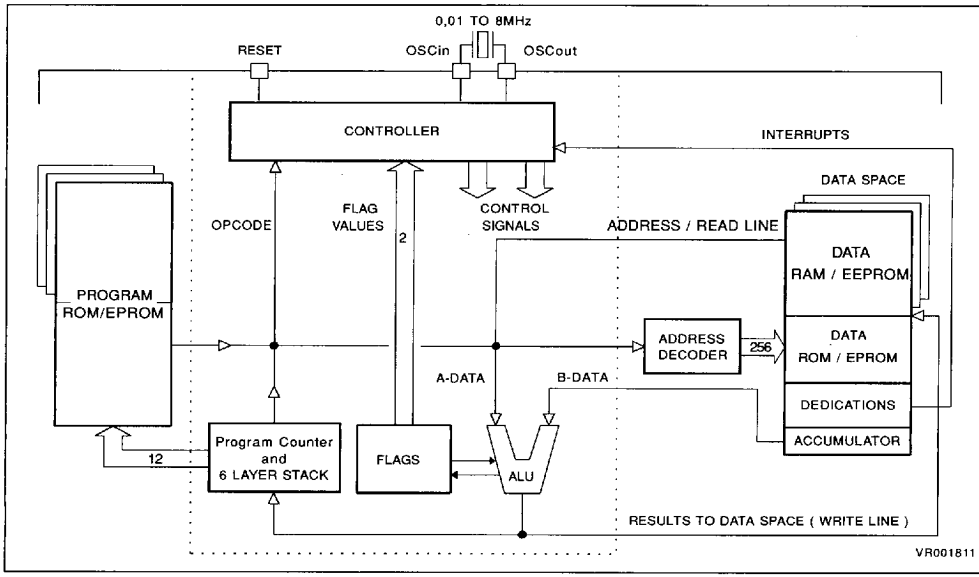


Figure 5. ST62xx Core Block Diagram



ST62xx CORE (Continued)

addressed in the data space as RAM locations at addresses 80h (X) and 81h (Y). They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST62xx instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save one byte in short direct addressing mode. These registers can be addressed in the data space as RAM locations at addresses 82h (V) and 83h (W). They can also be accessed with the direct and bit direct addressing modes. Accordingly, the ST62xx instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or an address of operand. The 12-bit length allows the direct addressing of 4096 bytes in the program space. Nevertheless, if the program space contains more than 4096 locations, the further program space can be addressed by using the Program Bank Switch register. The PC value is incremented, after it is read the address of the current instruction. To execute relative jumps the PC and the offset are shifted through the ALU, where they will be added, and the result is shifted back into the PC. The program counter can be changed in the following ways:

- JP (Jump) instruction . . . PC= Jump address
- CALL instruction . . . . PC= Call address
- Relative Branch Instructions. PC= PC ± offset
- Interrupt . . . . . PC=Interrupt vector
- Reset . . . . . PC= Reset vector
- RET & RETI instructions . PC= Pop (stack)
- Normal instruction . . . . PC= PC + 1

Flags (C, Z)

The ST62xx core includes three pairs of flags that correspond to 3 different modes: normal mode, interrupt mode and Non-Maskable-Interrupt-mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during normal operation, one pair is used during the interrupt mode (CI, ZI) and one is used during the not-maskable interrupt mode (CNMI, ZNMI).

The ST62xx core uses the pair of flags that correspond to the actual mode: as soon as an interrupt (resp. a Non-Maskable-Interrupt) is generated, the ST62xx core uses the interrupt flags (resp. the NMI flags) instead of the normal flags. When the RETI instruction is executed, the normal flags (resp. the interrupt flags) are restored if the MCU was in the normal mode (resp. in the interrupt mode) before the interrupt. It should be observed that each flag set can only be addressed in its own routine (Not-maskable interrupt, normal interrupt or main routine). The flags are not cleared during the context switching and so remain in the state they were at the exit of the last routine switching.

The Carry flag is set when a carry or a borrow occurs during arithmetic operations, otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction, and participates in the rotate left instruction.

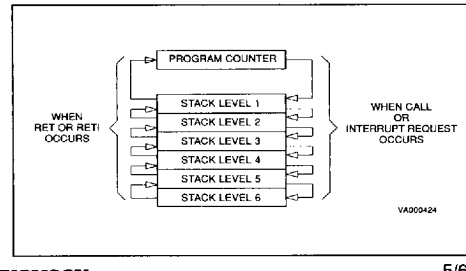
The Zero flag is set if the result of the last arithmetic or logical operation was equal to zero, otherwise it is cleared.

The switching between the three sets of flags is automatically performed when an NMI, an interrupt or a RETI instructions occurs. As the NMI mode is automatically selected after the reset of the MCU, the ST62xx core uses at first the NMI flags.

Stack

The ST62xx core includes true LIFO hardware stack that eliminates the need for a stack pointer. The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level is shifted into the next level while the content of the PC is shifted into the first level (the value of the sixth level will be lost). When a subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is popped back into the previous level. These two operating modes are described in Figure 6. Since the accumulator, as all other data space registers, is not stored in this stack the handling of these registers should be performed inside the subroutine. The stack pointer will remain in its deepest position if more than 6 calls or interrupts are executed, so that the last return address will be lost. It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

Figure 6. Stack Operation



MEMORY SPACES

The MCU operates in three different memory spaces: program space, data space, and stack space. A description of these spaces is shown in the following figures.

Program Space

The program space is physically implemented in the ROM memory and includes all the instructions that are to be executed, as well as the data required for the immediate addressing mode instructions, the reserved test area and the user vectors. It is addressed by the 12-bit Program Counter register (PC register) and so the ST62xx core can directly address up to 4K bytes of Program Space. ST62 devices with more than 4K ROM use ROM banked program memory (not available on ST6210B, 15B, 20B, 25B).

Rom Protection

The ST621xB, 2xB program space can be protected against external reading of the ROM contents when the READOUT PROTECTION mask option is selected. If this option is selected, the user can blow a dedicated fuse on the silicon by applying a high voltage at V_{PP} (see detailed information in the "Electrical Specification").

Note:

Once the fuse is blown, it is no longer possible, even for SGS-THOMSON, to gain access to the ROM contents. Returned parts with blown fuse can therefore not be accepted.

Table 1. ST6210B, 15B Program ROM Memory

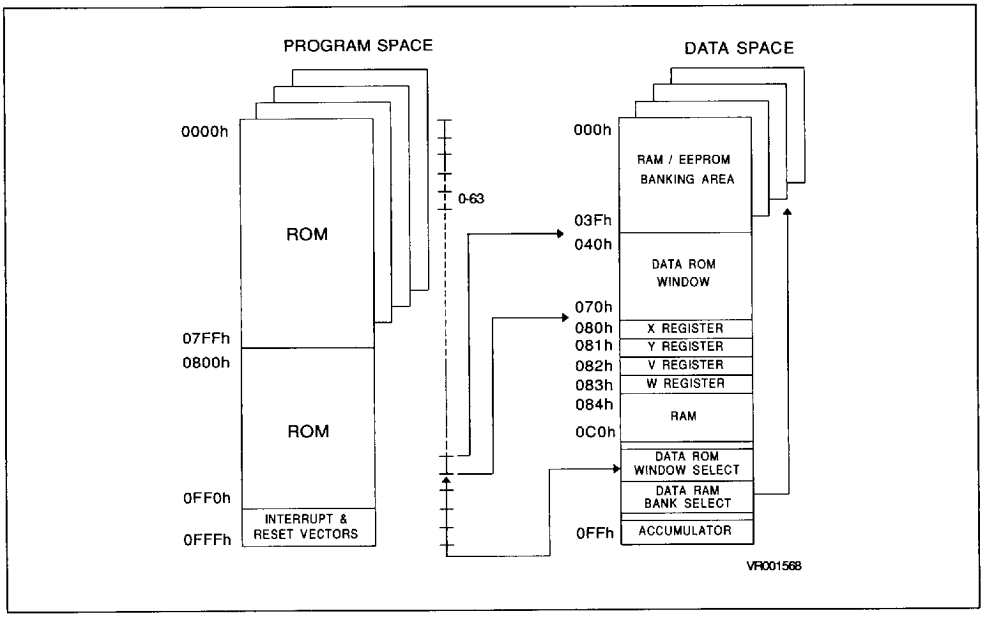
Device Address	Description
0000h-07FFh	Not implemented
0800h-087Fh	Reserved
0880h-0F9Fh	User Program ROM 1828 Bytes
0FA0h-0FEFh	Reserved
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved
0FFCh-0FFDh	NMI Vector
0FFEh-0FFFh	User Reset Vector

Table 2. ST6220B, 25B Program ROM Memory

Device Address	Description
0000h-007Fh	Reserved
0080h-0F9Fh	User Program ROM 3872 Bytes
0FA0h-0FEFh	Reserved
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved
0FFCh-0FFDh	NMI Vector
0FFEh-0FFFh	User Reset Vector

MEMORY SPACES (Continued)

Figure 7. Memory Addressing Description Diagram



MEMORY SPACES (Continued)

Data Space

The instruction set of the ST62xx core operates on a specific space, named Data Space, that contains all the data necessary for the processing of the program. The Data Space allows the addressing of RAM, ST62xx core/peripheral registers, and read-only data such as constants and look-up tables.

Data ROM. All the read-only data is physically implemented in the ROM memory in which the Program Space is also implemented. The ROM memory contains consequently the program to be executed, the constants and the look-up tables needed for the program.

The locations of Data Space in which the different constants and look-up tables are addressed by the ST62xx core can be considered as being a 64-byte window through which it is possible to access to the read-only data stored in the ROM memory.

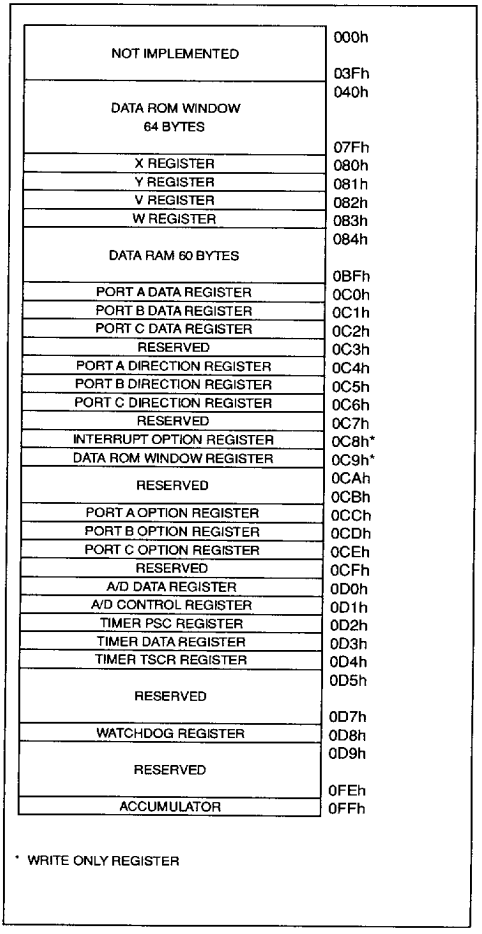
Data RAM. In the ST6210B, ST6215B, ST6220B and ST6225B products the data space includes 60 bytes of RAM, the accumulator (A), the indirect registers (X), (Y), the short direct registers (V), (W), the I/O port registers, the peripheral data and control registers, the interrupt option register and the Data ROM Window register (DRW register).

As the data space is less than 256 bytes the ST62xx core can directly address this area and the Data Bank Switch register (DRBR) has not been implemented.

Stack Space

The stack space consists of six 12 bit registers that are used for stacking subroutine and interrupt return addresses plus the current program counter register.

Figure 8. ST6210B,15B,20B,25B Data Memory Space



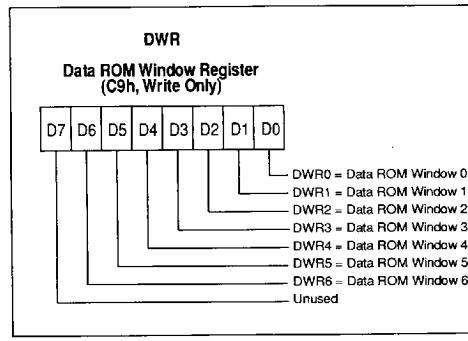
MEMORY SPACES (Continued)

Data Window register (DWR)

The Data ROM window is located from address 040h to address 7Fh in the Data space. It allows the direct reading of 64 consecutive bytes located anywhere in the ROM memory between the addresses 0000h and 1FFFh (if implemented on the particular device). All the bytes of the ROM memory can therefore be used to store either instructions or read-only data. Indeed, the window can be moved by step of 64 bytes along the ROM memory in writing the appropriate code in the Write-only Data Window register (DWR register, location C9h).

The DWR register can be addressed like a RAM location in the Data Space at the address C9h, nevertheless it is a write only register that cannot be accessed with single-bit operations. This register is used to move the 64-byte read-only data window (from the 40h address to 7Fh address of the Data Space) up and down the ROM memory of the MCU in steps of 64 bytes. The effective address of the byte to be read as a data in the ROM memory is obtained by the concatenation of the 6 least significant bits of the register address given in the instruction (as least significant bits) and the content of the DWR register (as most significant bits, see Figure 8). So when addressing location 40h of dataspace, and 0 is loaded in the DWR register, the phisycal addressed location in ROM is 00h. The DWR register is not cleared at reset, therefore it must be written to before the first access to the Data ROM window area.

Figure 10. Data ROM Window Register



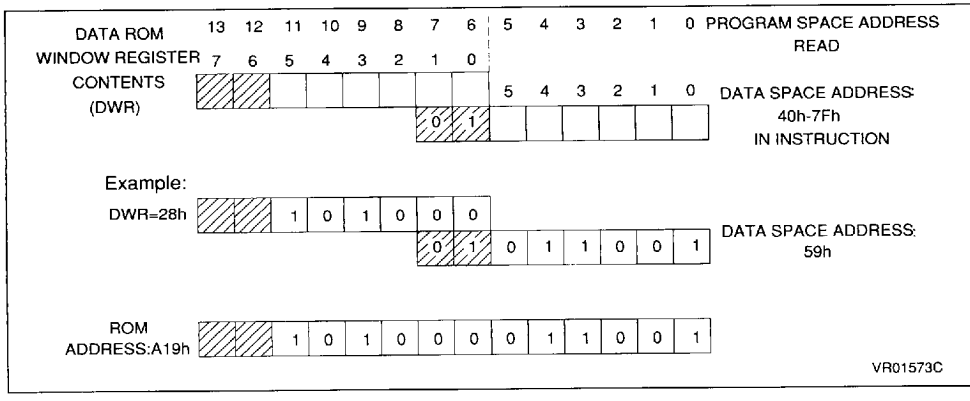
D7. This bit is not used.

DWR6-DWR0. These are the Data ROM Window bits that correspond to the upper bits of the data ROM space.

This register is undefined on reset. Neither read nor single bit instructions may be used to address this register.

Note: Care is required when handling the DWR register as it is write only. For this reason, it is not allowed to change the DWR contents while executing interrupt service routine, as the service routine cannot save and then restore its previous content. If it is impossible to avoid the writing of this register in the interrupt service routine, an image of this register must be saved in a RAM location, and each time the program writes to the DWR it must write also to the image register. The image register must be written first, so if an interrupt occurs between the two instructions the DWR is not affected.

Figure 9. Data ROM Window Memory Addressing



TEST MODE

For normal operation the TEST pin must be held low when reset is active. An on-chip 100kΩ pull-down resistor is internally connected to the TEST pin.

INTERRUPT

The ST62xx core can manage 4 different maskable interrupt sources, plus one non-maskable interrupt source (top priority level interrupt). Each source is associated with a particular interrupt vector that contains a Jump instruction to the related interrupt service routine. Each vector is located in the Program Space at a particular address (see Table 1). When a source provides an interrupt request, and the request processing is also enabled by the ST62xx core, then the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction). Finally, the PC is loaded with the address of the Jump instruction and the interrupt routine is processed.

The ST6210B, ST6215B, ST6220B and ST6225B microcontrollers have six different interrupt sources associated to different interrupt vectors as it is described in table below.

Table 3. Interrupt Vector/Source Relationship

Interrupt Source	Associated Vector	Vector Address
NMI pin	Interrupt vector #0 (NMI)	(FFCh, FFDh)
Port A pins	Interrupt vector #1	(FF6h, FF7h)
Port B pins	Interrupt vector #2	(FF4h, FF5h)
Port C pins	Interrupt vector #2	(FF4h, FF5h)
TIMER peripheral	Interrupt vector #3	(FF2h, FF3h)
ADC peripheral	Interrupt vector #4	(FF0h, FF1h)

Interrupt Vectors Description

- The ST62xx core includes 5 different interrupt vectors in order to branch to 5 different interrupt routines in the static page of the Program Space.
- The interrupt vector associated with the non-maskable interrupt source is named interrupt vector #0. It is located at addresses FFCh,FFDh in the Program Space. On ST6210B, ST6215B, ST6220B and ST6225B this vector is associated with the external falling edge sensitive interrupt pin (NMI).
- The interrupt vector located at addresses FF6h, FF7h is named interrupt vector #1. It is associated with Port A pins and can be programmed by software either in the falling edge detection mode or in the low level sensitive detection mode according to the code loaded in the Interrupt Option Register (IOR).
- The interrupt vector located at addresses FF4h, FF5h is named interrupt vector #2. It is associated with Port B and C pins and can be programmed by software either in the falling edge detection mode or in the positive edge detection mode according to the code loaded in the Interrupt Option Register (IOR).
- The two interrupt vectors located respectively at addresses FF2h, FF3h and addresses FF0h, FF1h are respectively named interrupt vector #3 and #4. Vector #3 is associated to the TIMER peripheral and vector #4 to the A/D converter peripheral.

All the on-chip peripherals have an interrupt request flag bit (TMZ for timer, EOC for A/D), that is set to one when the device generates an interrupt request and a mask bit (ETI for timer, EAI for A/D) that must be set to one to allow the transfer of the flag bit to the core.

Interrupt Priority

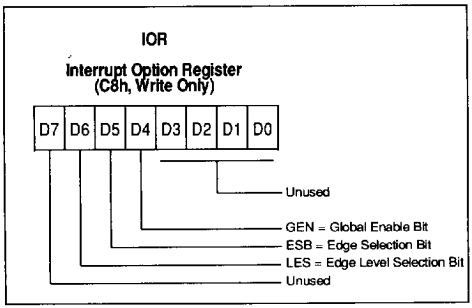
The non-maskable interrupt request has the highest priority and can interrupt any other interrupt routines at any time, nevertheless the four other interrupts can not interrupt each other. If more than one interrupt request are pending, they are processed by the ST62xx core according to their priority level: vector #1 has the higher priority while vector #4 the lower.
The priority of each interrupt source is fixed.

INTERRUPT (Continued)

Interrupt Option Register

The Interrupt Option Register (IOR register, location C8h) is used to enable/disable the individual interrupt sources and to select the operating mode of the external interrupt inputs. This register can be addressed in the Data Space as RAM location at the address C8h, nevertheless it is a write-only register that cannot be accessed with single-bit operations. The operating modes of the external interrupt inputs associated to interrupt vectors #1 and #2 are selected through bits 5 and 6 of the IOR register.

Figure 11. Interrupt Option Register



D7. D3-D0 These bits are not used.

LES. Level/Edge Selection Bit. When this bit is set to one, the interrupt #1 (Port A) is low level sensitive, when cleared to zero the negative edge sensitive interrupt is selected.

ESB. Edge Selection Bit. When this bit is set to one, the interrupt #2 (Ports B & C) is positive edge sensitive, when cleared to zero the negative edge sensitive interrupt is selected.

GEN. Global Enable Interrupt. When this bit is set to one, all the interrupts are enabled. When this bit is cleared to zero all the interrupts (excluding NMI) are disabled.

This register is cleared on reset.

Table 4. Interrupt Option Register Description

GEN	SET	Enable all interrupts
	CLEARED	Disable all interrupts
ESB	SET	Rising edge mode on interrupt input #2
	CLEARED	Falling edge mode on interrupt input #2
LES	SET	Level-sensitive mode on interrupt input #1
	CLEARED	Falling edge mode on interrupt input #1
OTHERS	NOT USED	

External Interrupts Operating Modes

The NMI interrupt is associated to the external interrupt pin of the ST6210B, ST6215B, ST6220B and ST6225B devices. This pin is falling edge sensitive and the interrupt pin signal is latched by a flip-flop which is automatically reset by the core at the beginning of the non-maskable interrupt service routine. A Schmitt trigger is present on NMI pin.

The two interrupt sources associated with the falling/rising edge mode of the external interrupt pins (Ports A-vector #1, Ports B and C-vector #2) are connected to two internal latches. Each latch is set when a falling/rising edge occurs during the processing of the first one, will be processed as soon as the first one has been finished (if there is not a higher priority interrupt request). If more than one interrupt occurs during the processing of the first one, these other interrupt requests will be lost.

The storage of the interrupt requests is not available in the level sensitive detection mode. To be taken into account, the low level must be present on the interrupt pin when the core samples the line after the execution of the instructions.

During the end of each instruction the core tests the interrupt lines and if there is an interrupt request the next instruction is not executed and the related interrupt routine is executed.

Note

On ST6210B,15B and ST6220B,25B the user can select the availability of an on-chip pull-up at NMI pin as ROM mask option (see option list at the end of the datasheet).

When GEN bit is low, the NMI interrupt is active but cannot cause a wake up from STOP/WAIT modes.

INTERRUPT (Continued)

Interrupt Procedure. The interrupt procedure is very similar to a call procedure, indeed the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event, the user does not know about the context and the time at which it occurred. As a result the user should save all the data space registers which will be used inside the interrupt routines. There are separate sets of processor flags for normal, interrupt and non-maskable interrupt modes which are automatically switched and so these do not need to be saved.

The following list summarizes the interrupt procedure:

ST62xx actions

– Interrupt detection
– The flags C and Z of the main routine are exchanged with the flags C and Z of the interrupt routine (or the NMI flags)
– The value of the PC is stored in the first level of the stack
– The normal interrupt lines are inhibited (NMI still active)
– First internal latch is cleared
– The related interrupt vector is loaded in the PC.

User actions

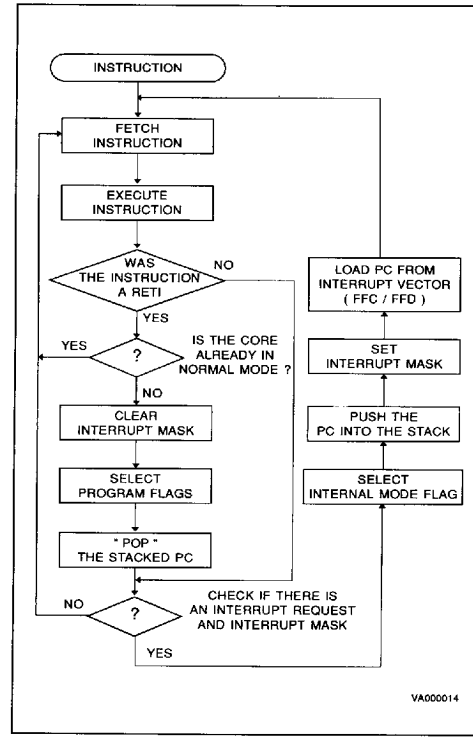
– User selected registers are saved inside the interrupt service routine (normally on a software stack)
– The source of the interrupt is found by polling (if more than one source is associated to the same vector) the interrupt flag of the source.
– Interrupt servicing
– Return from interrupt (RETI)

ST62xx actions

– Automatically the ST62xx core switches back to the normal flags (or the interrupt flags) and pops the previous PC value from the stack

The interrupt routine begins usually by the identification of the device that has generated the interrupt request (by polling). The user should save the registers which are used inside the interrupt routine (that holds relevant data) into a software stack. After the RETI instruction execution, the core carries out the previous actions and the main routine can continue.

Figure 12. Interrupt Processing Flow-Chart

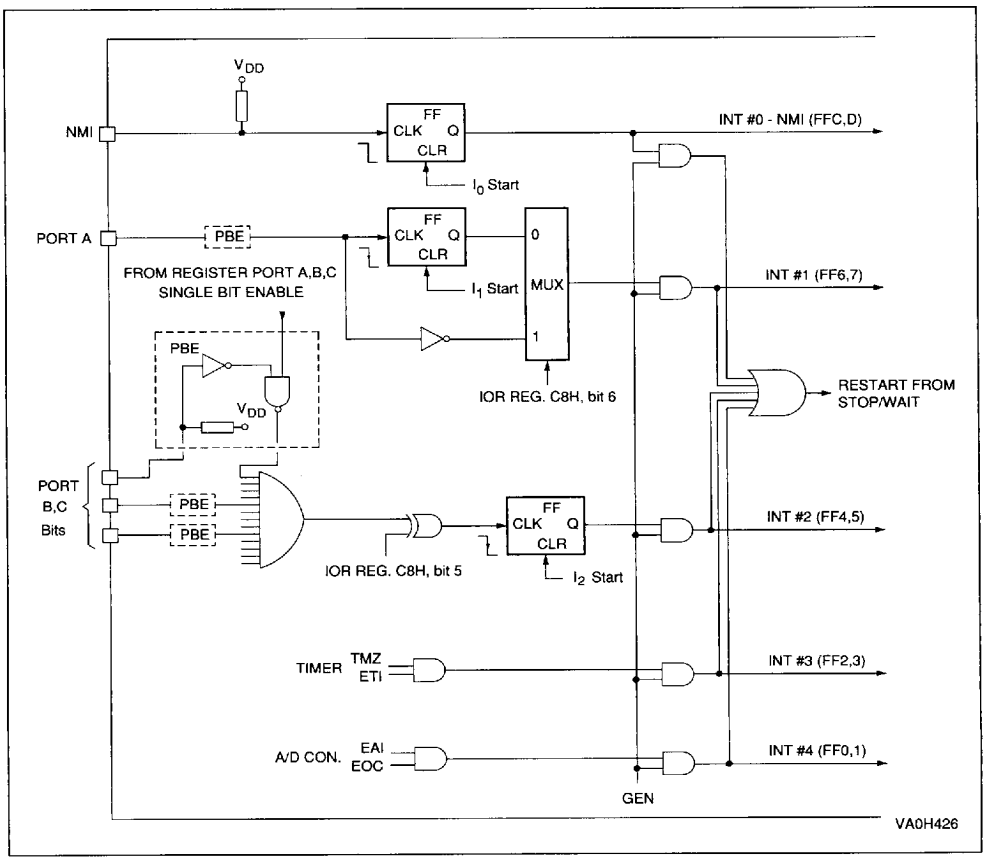


INTERRUPT (Continued)

Table 5. Interrupt Requests and Mask Bits

Peripheral	Register	Address Register	Mask bit	Masked Interrupt Source	Interrupt vector
GENERAL	IOR	C8h	GEN	All Interrupts, excluding NMI	
TIMER	TSCR	D4h	ETI	TMZ: TIMER Overflow	Vector 3
A/D Converter	ADCR	D1h	EAI	EOC: End of Conversion	Vector 4
Port PAn	ORPA-DRPA	C4h-CCh	ORPAn-DRPAn	PAn pin	Vector 1
Port PBn	ORPB-DRPB	C5h-CDh	ORPBn-DRPBn	PBn pin	Vector 2
Port PCn	ORPC-DRPC	C6h-CEh	ORPCn-DRPCn	PCn pin	Vector 2

Figure 13. Interrupt Circuit Diagram



RESET

The ST6210B, 15B, 20B, 25B can be reset in three ways: by the external reset input (RESET) tied low, by power-on reset and by the digital Watchdog peripheral.

RESET Input

The $\overline{\text{RESET}}$ pin can be connected to a device of the application board in order to restart the MCU during its operation. The activation of the $\overline{\text{RESET}}$ pin may occur in the RUN, WAIT or STOP mode. This input has to be used to reset the MCU internal state and provide a correct start-up procedure. The pin is active low and has a Schmitt trigger input. The internal reset signal is generated by adding a delay to the external signal. Therefore even short pulses at the $\overline{\text{RESET}}$ are accepted, provided V_{DD} has finished its rising phase and the oscillator is running correctly (normal RUN or WAIT modes). The MCU is kept in the Reset state as long as the $\overline{\text{RESET}}$ pin is held low.

If the $\overline{\text{RESET}}$ activation occurs in the RUN or WAIT mode, the processing of the program is stopped (in RUN mode only), the Input/Outputs are placed in input with pull-up resistors, the Low Frequency Auxiliary Oscillator (LFAO) is stopped and the main Oscillator is restarted. When the level on the RESET pin becomes high, the initialization sequence is executed just after the internal delay.

If a $\overline{\text{RESET}}$ pin activation occurs in the STOP mode, the oscillator starts and all the inputs/outputs are configured in input with pull-up resistors. When the level of the $\overline{\text{RESET}}$ pin becomes high, the initialization sequence is started just after the internal delay.

Power-on Reset

The function of the POR consists in waking up the MCU during the power-on sequence. At the beginning of this sequence, the MCU is configured in the Reset state: every Input/Output port is configured in input with pull-up resistor and no instruction is executed. When the power supply voltage becomes sufficient, the oscillator starts to operate, nevertheless an internal delay is generated to allow the oscillator to be completely stabilized before the execution of the first instruction. The initialization sequence is executed just after the internal delay.

The internal delay is generated by an on-chip counter. The internal reset is released 2048 cycles of the internal frequency after the external reset is released.

Note:

When the OSG is enabled, the first pulses to the on-chip counter generating the internal delay are coming from the Low Frequency Auxilliary Oscillator (LFAO), until the Main Oscillator starts running.

To have a correct start-up, the user should take care that the internal reset is not released before the V_{DD} level is sufficient to allow MCU operation at the chosen frequency (see Recommended Operating Conditions).

A proper reset signal for slow rising V_{DD} can be generally provided by an external RC network connected at pin $\overline{\text{RESET}}$.

RESET (Continued)

Watchdog Reset

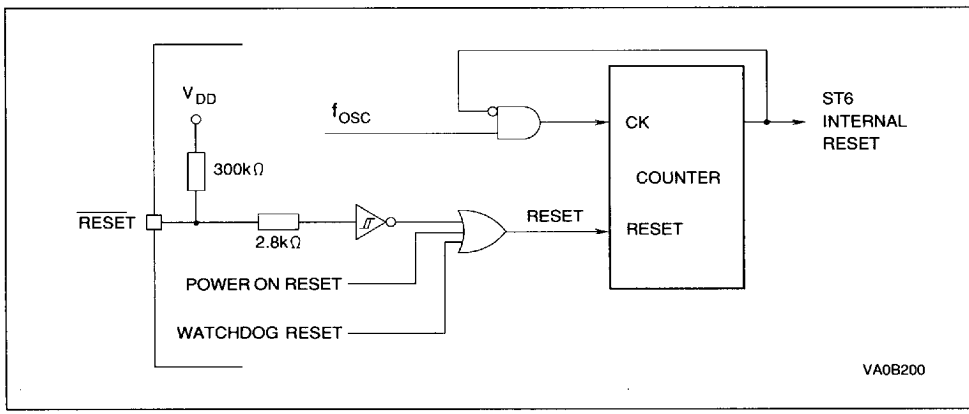
The ST621xB, 2xB provide an on-chip watchdog function in order to provide a graceful recovery from a software upset. If the watchdog register is not refreshed, preventing the end-of-count being reached, the internal reset is activated. This, in particular, resets the watchdog. The MCU restarts as with normal reset from RESET pin including the internal delay.

Application Notes

An external resistor between V_{DD} and reset pin is not required because an internal pull-up device is provided.

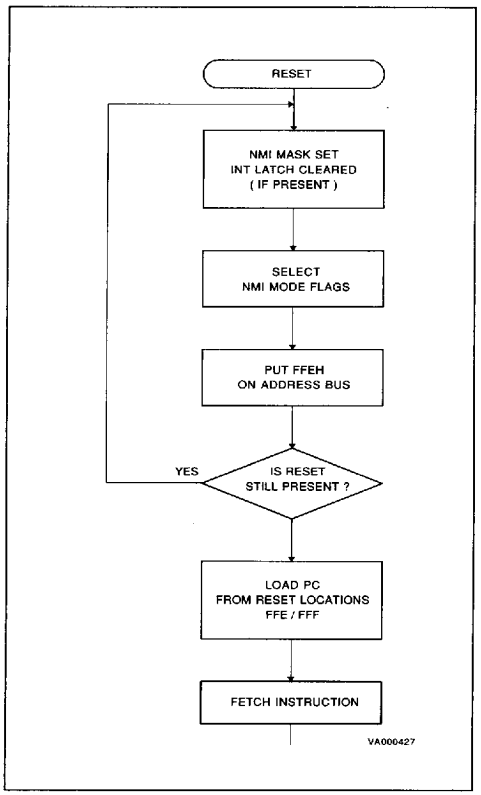
The POR device operates in a dynamic manner in the way that it brings about the initialization of the MCU when it detects a dynamic rising edge of the V_{DD} voltage. The typical detected threshold is about 2 volts, but the actual value of the detected threshold depends on the way in which the V_{DD} voltage rises up. The POR device *DOES NOT* allow the supervision of a static or slowly rising or falling edge of the V_{DD} voltage.

Figure 14. Reset Circuit



RESET (Continued)

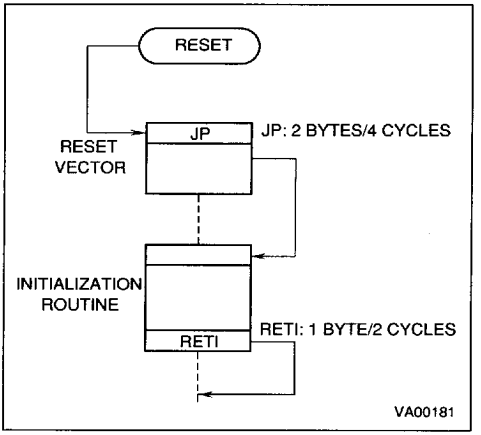
Figure 15. Reset and Interrupt Processing Flow-Chart



MCU Initialization Sequence

When a reset occurs the stack is reset to the program counter, the PC is loaded with the address of the reset vector (located in the program ROM at addresses FFEh & FFFh). A jump instruction to the beginning of the program has to be written into these locations. After a reset a NMI is automatically activated so that the core is in non-maskable interrupt mode to prevent false or ghost interrupts during the restart phase. Therefore the restart routine should be terminated by a RETI instruction to switch to normal mode and enable interrupts. If no pending interrupt is present at the end of the reset routine the ST62xx will continue with the instruction after the RETI; otherwise the pending interrupt will be serviced.

Figure 16. Restart Initialization Program Flow-Chart



RESET (Continued)

Table 6. Reset Value

Register	Address	Value	Comment
Port Data Registers	0C0h to 0C2h		
Port Direction Register	0C4h to 0C6h		I/O are Input with pull-up
Port Option Register	0CCh to 0CEh	00h	I/O are Input with pull-up
Interrupt Option Register	0C8h		Interrupt disabled
Timer Status/Control	0D4h		Timer disabled
X, Y, V, W, Register	080h to 083h		
Accumulator	0FFh		
Data RAM	084h to 0BFh	Undefined	As written if programmed
Data ROM Window Register	0C9h		
A/D Result Register	0D0h		
Timer Counter Register	0D3h	FFh	
Timer Prescaler Register	0D2h	7Fh	Max count loaded
Watchdog Counter Register	0D8h	FEh	
A/D Control Register	0D1h	40h	A/D in Standby, main oscillator ON

WAIT & STOP MODES

The WAIT and STOP modes have been implemented in the ST62xx core in order to reduce the consumption of the product when the latter has no instruction to execute. These two modes are described in the following paragraphs.

In addition, the Low Frequency Auxiliary Oscillator (LFAO) can be used instead of the main oscillator to reduce power consumption in RUN and WAIT mode.

WAIT Mode

The MCU goes into the WAIT mode as soon as the WAIT instruction is executed. The microcontroller can also be considered as being in a "software frozen" state where the core stops processing the instructions of the routine, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage, but where the peripherals are still working.

The WAIT mode can be used when the user wants to reduce the consumption of the MCU when it is idle, while not losing count of time or monitoring of external events. The active oscillator (main oscillator or LFAO) is not stopped in order to provide a clock signal to the peripherals. The Timer counting may be enabled as well as the Timer interrupt before entering the WAIT mode; this allows the WAIT mode to be left when Timer interrupt occurs. The above explanation related to the timers applies also to the A/D converter.

If the power consumption has to be further reduced, the Low Frequency Auxiliary Oscillator (LFAO) can be used (provided the main oscillator has a frequency higher than the LFAO). It must be switched on before entering the WAIT mode.

If the exit from the WAIT mode is performed with a general RESET (either from the activation of the external pin or by watchdog reset) the MCU enters a normal reset procedure as described in the RESET chapter. If an interrupt is generated during WAIT mode the MCU behavior depends on the state of the ST62xx core before the initialization of the WAIT sequence, but also of the kind of the interrupt request that is generated. This case is described in the following paragraphs. In any case, the ST62xx core does not generate any delay after the occurrence of the interrupt because the oscillator clock is still available.

STOP Mode

If the Watchdog is disabled the STOP mode is available. When in STOP mode the MCU is placed in the lowest power consumption mode. In this operating mode the microcontroller can be considered as being "frozen", no instruction is executed, the oscillator is stopped, the contents of the RAM locations and peripheral registers are saved as long as the power supply voltage is higher than the RAM retention voltage, and the ST62xx core waits for the occurrence of an external interrupt request or Reset activation to output from the STOP state.

If the exit from the STOP mode is performed with a general RESET (by the activation of the external pin) the MCU will enter a normal reset procedure as described in the RESET chapter. The case of an interrupt depends on the state of the ST62xx core before the initialization of the STOP sequence and also of the kind of the interrupt request that is generated.

WAIT & STOP MODES (Continued)

This case will be described in the following paragraphs. In any case, the ST62xx core generates a delay after the occurrence of the interrupt request in order to wait for the complete stabilization of the oscillator before the execution of the first instruction.

Exit from WAIT and STOP Modes

The following paragraphs describe the output procedure of the ST62xx core from WAIT and STOP modes when an interrupt occurs (not a RESET). It must be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) before the start of the WAIT or STOP sequence, but also of the type of the interrupt request that is generated.

In any case, interrupts do not affect the oscillator selection. When the LFAO is used, the user program must handle oscillator selection as soon as the RUN mode resumes.

Normal Mode. If the ST62xx core was in the main routine when the WAIT or STOP instruction has been executed, the ST62xx core outputs from the stop or wait mode as soon as any interrupt occurs; the related interrupt routine is executed and at the end of the interrupt service routine the instruction that follows the STOP or the WAIT instruction is executed if no other interrupts are pending.

Not Maskable Interrupt Mode. If the STOP or WAIT instruction has been executed during the execution of the non-maskable interrupt routine, the ST62xx core outputs from the stop or wait mode as soon as any interrupt occurs: the instruction that follows the STOP or the WAIT instruction is executed and the ST62xx core is still in the non-maskable interrupt mode even if another interrupt has been generated.

Normal Interrupt Mode. If the ST62xx core was in the interrupt mode before the initialization of the STOP or WAIT sequence, it outputs from the stop or wait mode as soon as any interrupt occurs. Nevertheless, two cases have to be considered:

- If the interrupt is a normal interrupt, the interrupt routine in which the wait or stop was entered will be completed with the execution of the instruction that follows the STOP or the WAIT and the ST6xx core is still in the interrupt mode. At the end of this routine pending interrupts will be serviced in accordance to their priority.
- If the interrupt is a non-maskable interrupt, the non-maskable routine is processed at first. Then the routine in which the wait or stop was entered will be completed with the execution of the instruction that follows the STOP or the WAIT and the ST6xx core remains in the normal interrupt mode.

Notes:

To reach the lowest power consumption during RUN or WAIT modes, the user software must take care of:

- configuring unused I/O as input without pull-up with well defined logic levels.
- placing the A/D converter in its power down mode by clearing the PDS bit in the A/D control register before entering the STOP instruction.
- stopping Timer external clock
- selecting the Low Frequency Auxiliary Oscillator (provided the main oscillator runs faster).

When the hardware activated watchdog is selected or the software watchdog enabled, the STOP instruction is deactivated and any attempt to execute the STOP instruction will cause an execution of a WAIT instruction.

If all the interrupt sources are disabled (including NMI if GEN is low), the restart of the MCU can only be done by a Reset activation. The WAIT and STOP instructions are not executed if an enabled interrupt request is pending.

ON-CHIP CLOCK OSCILLATOR

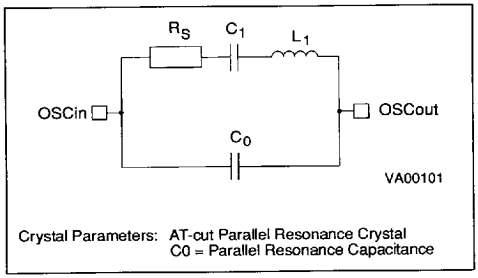
The ST6210B,15B, 20B, 25B provide a Main Oscillator which can be used with an external clock, with crystal or ceramic resonator, with a RC network. In addition, a Low Frequency Auxiliary Oscillator can be switched on for safety reason, to reduce power consumption or to have a fully integrated clock circuitry.

The internal frequency is divided by 12 to produce the Timer, the A/D converter and the Watchdog clock.

With a 8MHz external frequency, the fastest machine cycle is therefore 1.625µs.

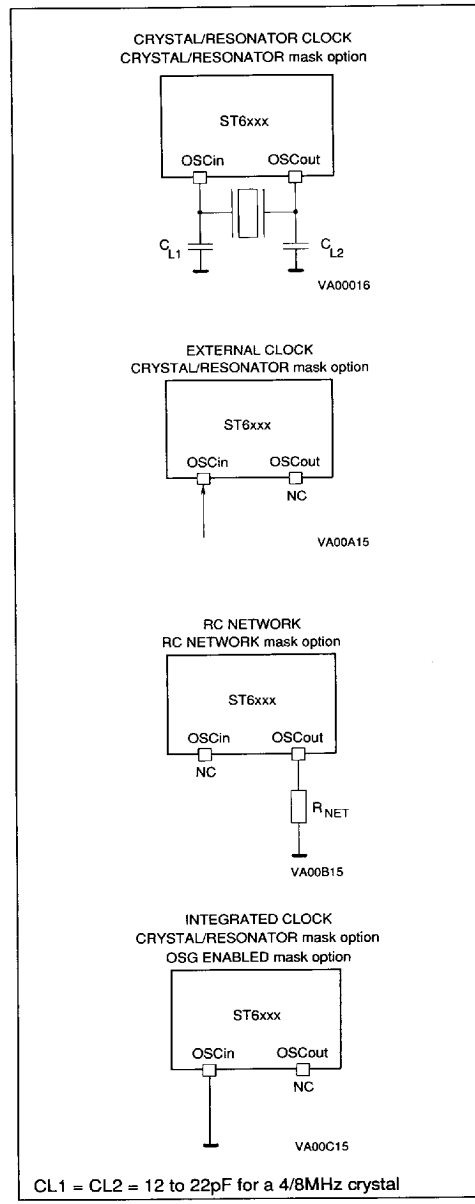
The machine cycle is the smallest unit needed to execute any operation (i.e. increment the program counter). An instruction may need two, four, or five machine cycles to be executed.

Figure 17. Crystal Parameters



Crystal Parameters: AT-cut Parallel Resonance Crystal
C0 = Parallel Resonance Capacitance

Figure 18. Oscillator Connection



CL1 = CL2 = 12 to 22pF for a 4/8MHz crystal

ON-CHIP CLOCK OSCILLATOR (Continued)

Main Oscillator

The oscillator is configured through mask option. When the CRYSTAL/RESONATOR option is selected, it must be used with a quartz crystal, a ceramic resonator or an external signal provided on pin OSCin. When the RC NETWORK option is selected, the system clock is generated by a RC network.

The oscillator can be turned off when the OSG ENABLED mask option is selected by setting OSCOFF bit of the ADC Control Register. The Low Frequency Auxiliary Oscillator is automatically started.

Turning on the main oscillator is achieved by a software reset of bit OSCOFF of the A/D Converter Control Register or by resetting the MCU. Restarting the main oscillator takes the oscillator start up time plus possibly the duration of the software instruction at f_{LFAO} low frequency.

Low Frequency Auxiliary Oscillator (LFA0)

The Low Frequency Auxiliary Oscillator has three main purposes. First, it can be used to reduce power consumption in non timing critical routines. Second, it enables to generate a fully integrated system clock, without any external components. Last, it acts as safety oscillator in case of the main oscillator fails.

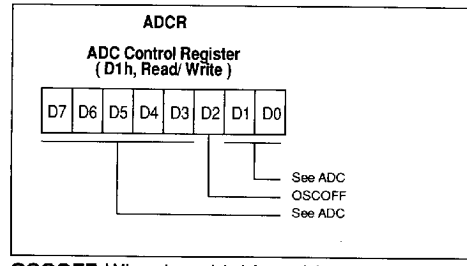
This oscillator is available when the OSG ENABLED mask option is selected. In this case, it automatically starts one of its periods after the first missing edge from the main oscillator, whatever the reason (main oscillator defective, no clock circuitry provided, main oscillator switched off ...).

User program, normally interrupts, WAIT and STOP instructions, is normally processed but at the reduced f_{LFAO} frequency. The A/D converter accuracy is decreased, as the internal frequency is below 1MHz.

At power on, the Low Frequency Auxiliary Oscillator starts faster than the Main Oscillator. It therefore feeds the on-chip counter generating the POR delay until the Main Oscillator runs.

The Low Frequency Auxiliary Oscillator is switched off as soon as the main oscillator starts.

Figure 19.OSCOFF Bit in ADC Control Register



OSCOFF. When low, this bit enables main oscillator to run. The main oscillator is switched off when OSCOFF is high.

Oscillator Safe Guard

The Oscillator Safe Guard (OSG) enables to drastically increase the safety of operation of ST62xx devices. It has three basic functions. It first filters spikes from the oscillator lines which would result in over frequency to the ST62 core. Second, it gives access to the Low Frequency Auxilliary Oscillator (LFAO), used to ensure minimum processing in case of failure of the main oscillator, to reduce power consumption or to provide a fixed frequency low cost oscillator. Last, it automatically limits the internal frequency to ensure correct operation in case the power supply drops.

The OSG is enabled or disabled through the OSG mask option. It can be seen as a filter whose cross over frequency is device dependent.

Spikes on the oscillator lines result in an increased internal frequency. Without the OSG, this may lead to an over frequency at the operating power supply. The OSG filters such spikes (see Figure 20). Anyway, enabling the OSG limits the maximum frequency to f_{osg}.

When the OSG is enabled, it gives access to the Low Frequency Auxiliary Oscillator. This oscillator starts operating after the first missing edge of the main oscillator (see Figure 21).

Over frequency at a given power supply is seen by the OSG as spikes. It therefore filters some periods in order that the internal frequency of the device is kept within both the range the particular device can stand (depending on Vdd) and below f_{osg} , the maximum authorised frequency with OSG enabled.

Notes:

The OSG should be used wherever possible as it provides maximum safety. Care must be taken as it increases power consumption and reduces the maximum authorised frequency down to f_{OSG}.

ON-CHIP CLOCK OSCILLATOR (Continued)

Figure 20. OSG Filtering Principle

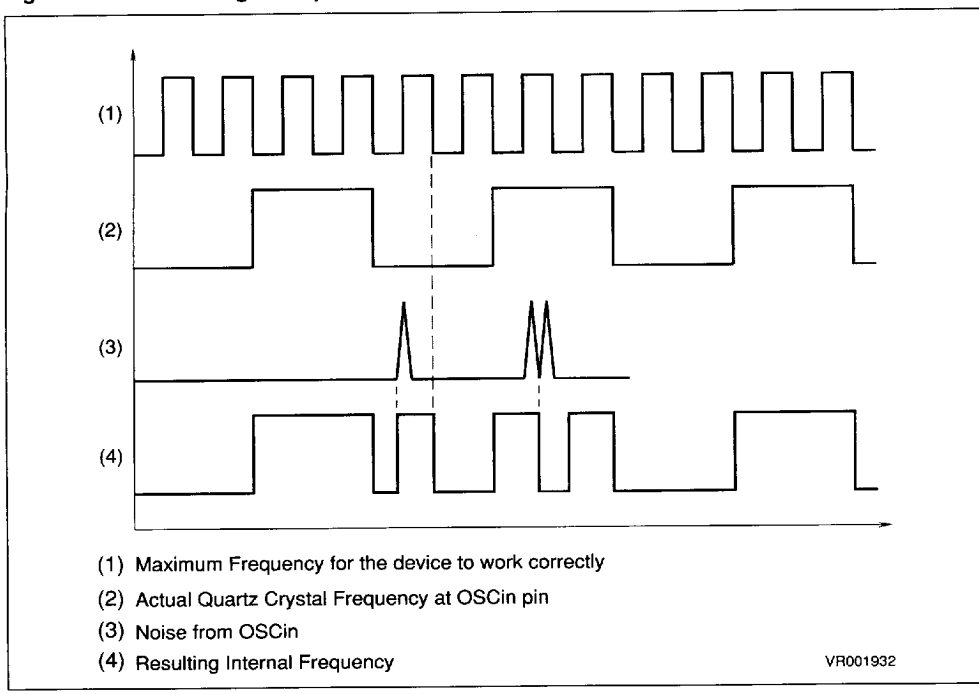
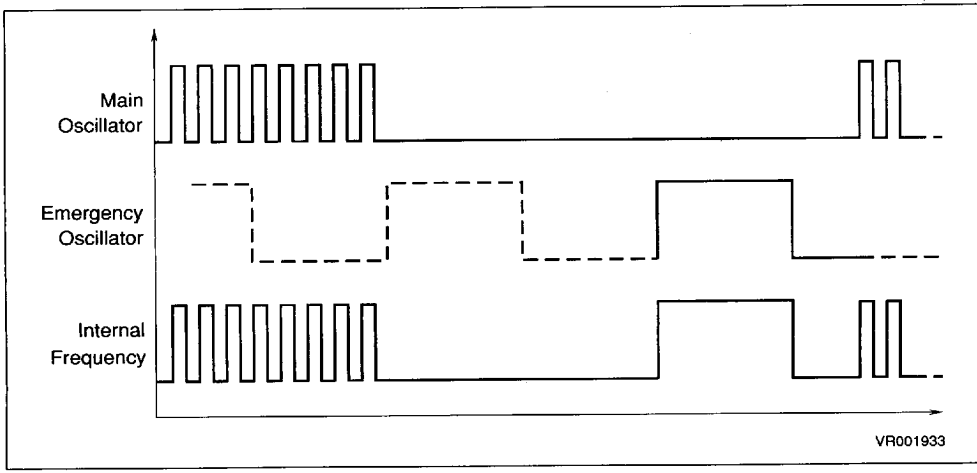
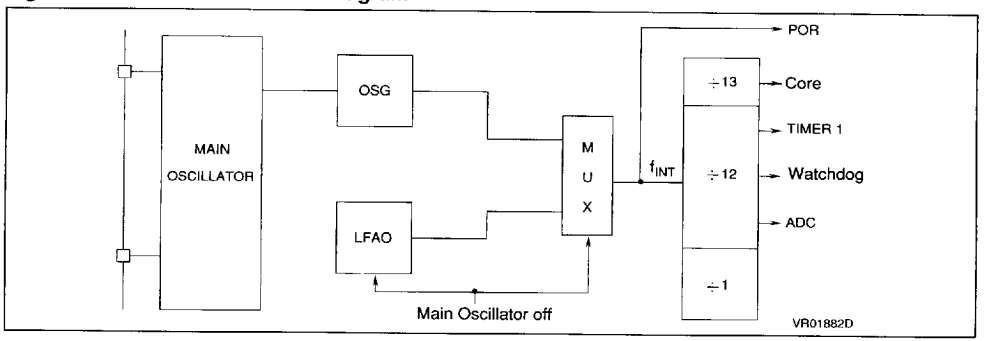


Figure 21. OSG Emergency Oscillator Principle

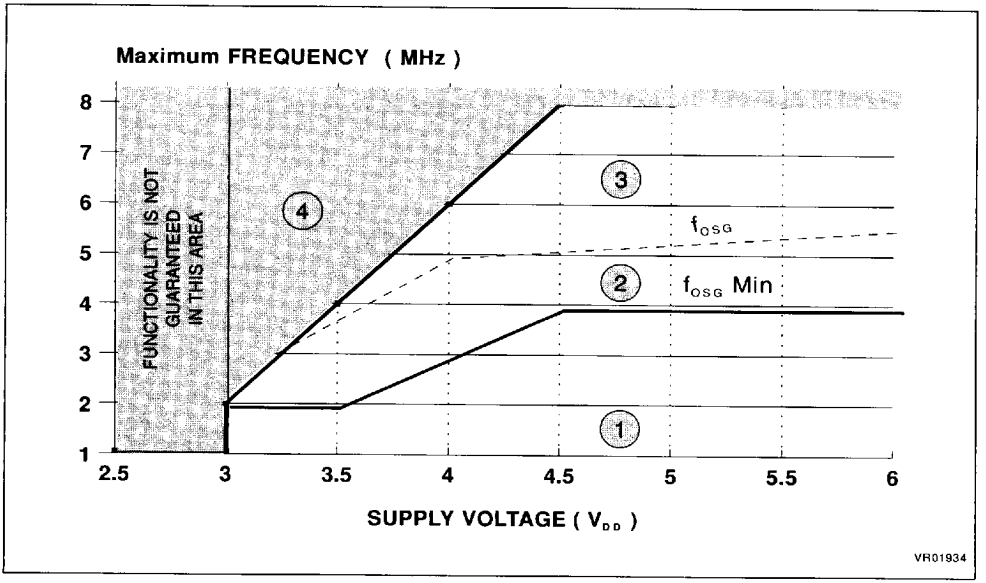


ON-CHIP CLOCK OSCILLATOR (Continued)

Figure 22. Clock Circuits Block Diagram



Maximum Operating Frequency (f_{MAX}) versus Supply Voltage (V_{DD})



① In this area, operation is guaranteed at the quartz crystal frequency.

② When the OSG is disabled, operation in this area is guaranteed at the quartz crystal frequency
When the OSG is enabled, operation in this area is guaranteed at a frequency of at least f_{OSG} min.

③ When the OSG is disabled, operation in this area is guaranteed at the quartz crystal frequency
When the OSG is enabled, access to this area is prevented. The internal frequency is kept at f_{OSG}.

④ When the OSG is disabled, operation in this area is not guaranteed
When the OSG is enabled, access to this area is prevented. The internal frequency is kept at f_{OSG}.

INPUT/OUTPUT PORTS

The ST6210B, ST6215B, ST6220B and ST6225B microcontroller have respectively 12 and 20 Input/Output lines that can be individually programmed either in the input mode or the output mode with the following software selectable options:

- Input without pull-up and without interrupt
- Input with pull-up and with interrupt
- Input with pull-up without interrupt
- Analog inputs (PA4-PA7, PB0-PB7, PC4-PC3)
- Push-pull output
- Standard Open drain output
- 20mA Open drain output

The lines are organized in three Ports (Port A, B and C).

Each port occupies 3 registers in the data space. Each bit of these registers is associated with a particular line (for instance, the bits 0 of the Port A Data, Direction and Option registers are associated with the PA0 line of Port A).

The three DATA registers (DRA, DRB, DRC), are used to read the voltage level values of the lines programmed in the input mode, or to write the logic value of the signal to be output on the lines configured in the output mode. The port data registers can be read to get the effective logic levels of the pins, but they can be also written by the user software, in conjunction with the related option registers, to select the different input mode options.

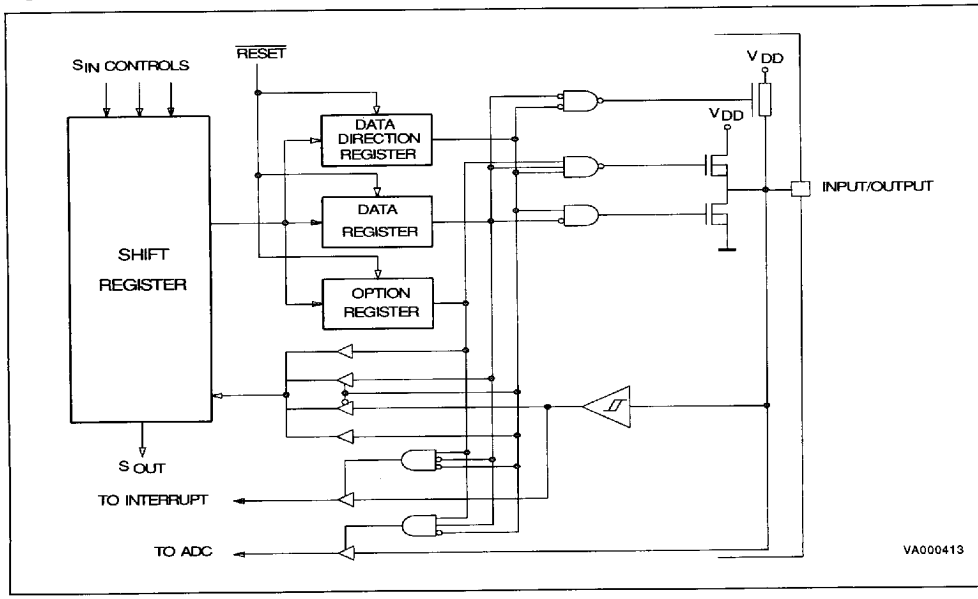
Single-bit operations on I/O registers are possible but care is necessary because reading in input mode is done from I/O pins while writing will directly affect the Port data register causing an undesired change of the input configuration.

The three Data Direction registers (DDRA, DDRB and DDRC) allow the selection of the data direction of each pin (input or output).

The three Option registers (ORA, ORB and ORC) are used to select the different port options available both in input and in output mode.

All the I/O registers can be read or written as any other RAM location of the data space, so no extra RAM cell is needed for port data storing and manipulation. During the initialization of the MCU, all the I/O registers are cleared and the input mode with pull-up/no-interrupt is selected on all the pins, thus avoiding pin conflicts.

Figure 23. I/O Port Block Diagram



INPUT/OUTPUT PORTS (Continued)

I/O Pin Programming

Each pin can be individually programmed as input or output with different input and output configurations, except PB0 and PC7 when the External STOP Mode Control option is selected.

This is achieved by writing the relevant bit in the data (DR), data direction register (DDR) and option registers (OR). Table 7 shows all the port configurations that can be selected by user software.

Input Option Description

Pull-up, High Impedance Option. All the input lines can be individually programmed with or without an internal pull-up according to the codes programmed in the OR and DR registers. If the pull-up option is not selected, the input pin is in the high-impedance state.

Interrupt Option. All the input lines can be individually connected by software to the interrupt lines of the ST62xx core according to the codes programmed in the OR and DR registers. The pins of Port A are AND-connected to the interrupt associated to the vector #1. The pins of Port B & C are AND-connected to the interrupt associated to the vector #2. The interrupt modes (falling edge sensitive, rising edge sensitive, low level sensitive) can be selected by software for each port by programming the IOR register.

Analog Input Option. The sixteen PA4-PA7, PB0-PB7, PC4-PC7 pins can be configured to be analog inputs according to the codes programmed in the OR and DR registers. These analog inputs are connected to the on-chip 8-bit Analog to Digital Converter. *ONLY ONE* pin should be programmed as analog input at a time, otherwise the selected inputs will be shorted.

Figure 24. I/O Port Option Registers

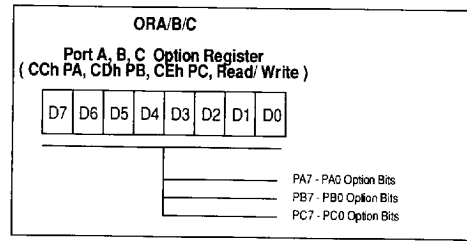


Figure 25. I/O Port Data Direction Registers

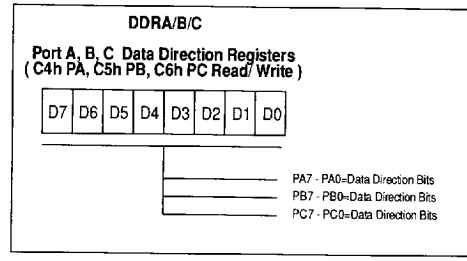
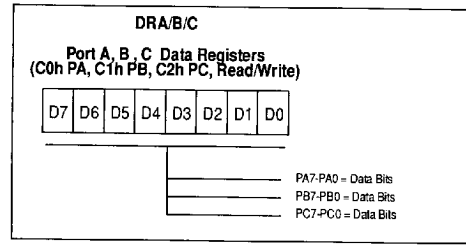


Figure 26. I/O Port Data Registers



Note: For complete coding explanation refer to Table 7

Table 7. I/O Port Options Selection

DDR	OR	DR	Mode	Option
0	0	0	Input	With pull-up, no interrupt (Reset state)
0	0	1	Input	No pull-up, no interrupt
0	1	0	Input	With pull-up, with interrupt
0	1	1	Input	No pull-up, no interrupt (PA0-PA3 pins)
			Input	Analog input (PA4-PA7, PB0-PB7, PC4-PC7 pins)
1	0	X	Output	20mA sink open-drain output (PA0-PA3 pins)
1	0	X	Output	Standard open-drain output (PA4-PA7, PB0-PB7, PC4-PC7 pins)
1	1	X	Output	20mA sink push-pull output (PA0-PA3 pins)

Notes: X. Means don't care.

INPUT/OUTPUT PORTS (Continued)

Note:

Switching the I/O ports from one state to another should be done in a way that no unwanted side effects can happen. The recommended safe transitions are shown below. All other transitions are risky and should be avoided during change of operation mode as it is most likely that there will be an unwanted side-effect such as interrupt generation or two pins shorted together by the analog input lines.

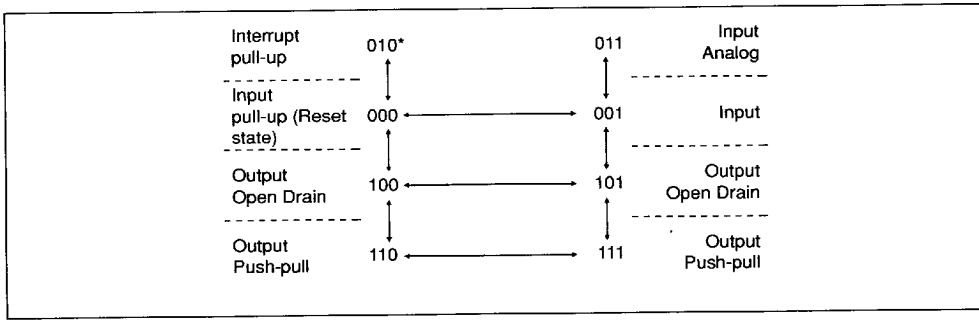
Single bit instructions (SET, RES, INC and DEC) should be used very carefully with Port A, B and C data registers because these instructions make an implicit read and write back of the whole addressed register byte. In port input mode however data register address reads from input pins, not from data register latches and data register information in input mode is used to set characteristics of the input pin (interrupt, pull-up, analog input), therefore these characteristics may be unintentionally reprogrammed depending on the state of input pins. As general rule is better to use single bit instructions on data register only when the whole port is in output mode. If input or mixed configuration is needed it is recommended to keep a copy of the data register in RAM. On this copy it is possible to use single bit instructions, then the copy register could be written into the port data register.

```
SET     bit, datacopy
LD      a, datacopy
LD      DRA, a
```

The WAIT and STOP instructions allow the ST62xx to be used in situations where low power consumption is needed. The lowest power consumption is achieved by configuring I/Os in input mode with well-defined logic levels.

The user has to take care not to switch outputs with heavy loads during the conversion of one of the analog inputs in order to avoid any disturbance in the measurement.

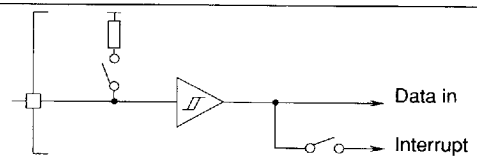
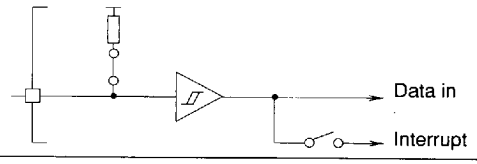
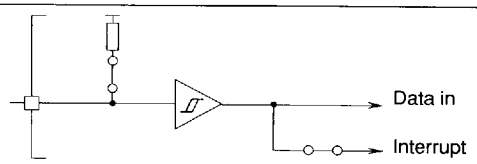
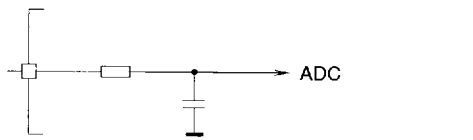
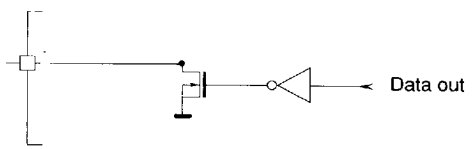
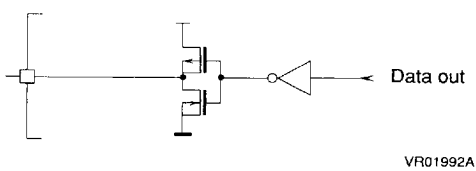
State Transition Diagram for Safe Transitions



Note *. xxx = DDR, OR, DR Bits respectively

INPUT/OUTPUT PORTS (Continued)

Table 8. I/O Port Options Selection

Mode	Available At[1]	Schematic
Input	PA0-PA7 PB0-PB7 PC4-PC7 TIMER	
Input with pull up	PA0-PA7 PB0-PB7 PC4-PC7 TIMER	
Input with pull up with interrupt	PA0-PA7 PB0-PB7 PC4-PC7	
Analog Input	PA4-PA7 PC4-PC7 PB0-PB7	
Open drain output 5mA Open drain output 20mA	PA4-PA7 PB0-PB7 PC4-PC7 PA0-PA3	
Push-pull output 5mA Push-pull output 20mA	PA4-PA7 PB0-PB7 PC4-PC7 PA0-PA3	

Note 1. Provided proper configuration.

TIMER

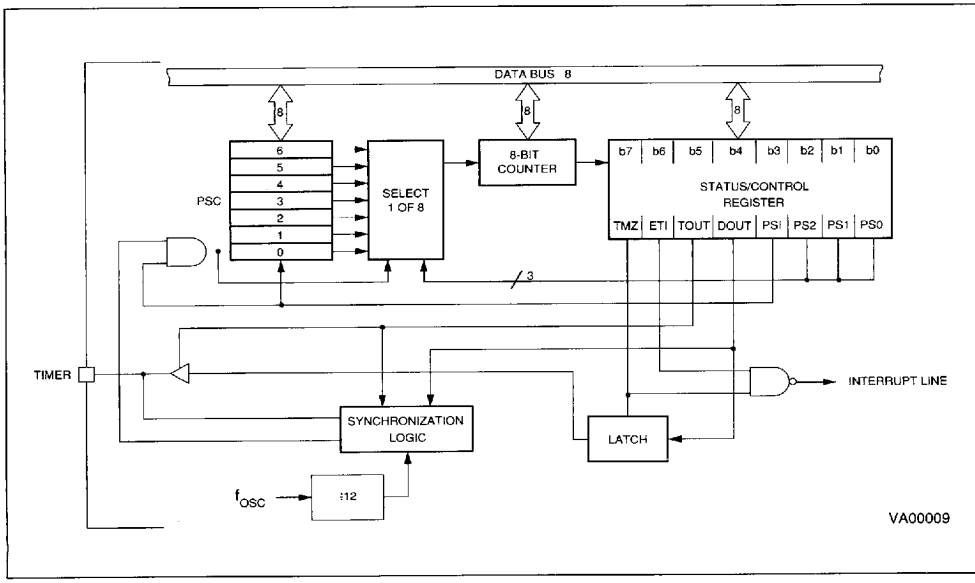
The ST6210B, ST6215B, ST6220B and ST6225B offer one on-chip Timer peripheral consisting of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of 2^{15}, and control logic that allows configuring the peripheral in three operating modes.

Figure 27 shows the Timer block diagram. This timer has the external TIMER pin available for the user. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as a RAM location at address D3h. The state of the 7-bit prescaler can be read in the PSC register at address D2h. The control logic device is managed in the TSCR register (D4h address) as described in the following paragraphs.

The 8-bit counter is decrement by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (Timer Zero)bit in the TSCR is set to one. If the ETI (Enable Timer Interrupt) bit in the TSCR is also set to one an interrupt request, associated to interrupt vector #3, is generated. The Timer interrupt can be used to exit the MCU from the WAIT mode.

The prescaler input can be the internal frequency divided by 12 or an external clock at TIMER pin. The prescaler decrements on the rising edge. Depending on the division factor programmed by PS2, PS1 and PS0 bits in the TSCR (see table 10), the clock input of the timer/counter register is multiplexed to different sources. On division factor 1, the clock input of the prescaler is also that of timer/counter; on factor 2, bit 0 of prescaler register is connected to the clock input of TCR. This bit changes its state with the half frequency of prescaler clock input. On factor 4, bit 1 of PSC is connected to clock input of TCR, and so on. The prescaler initialize bit PSI in the TSCR register must be set to one to allow the prescaler (and hence the counter) to start. If it is cleared to zero then all of the prescaler bits are set to one and the counter is inhibited from counting. The prescaler can be given any value between 0 and 7Fh by writing to address D2h, if bit PSI in the TSCR register is set to one. The tap of the prescaler is selected using the PS2/PS1/PS0 bits in the control register.
Figure 28 shows the Timer working principle.

Figure 27. Timer Block Diagram



TIMER (Continued)

Timer Operating Modes

There are three operating modes of the Timer peripheral. They are selected by the bits TOUT and DOUT (see TSCR register). These three modes correspond to the two clock frequencies that can be connected on the 7-bit prescaler (f_{INT}÷12 or TIMER pin signal) and to the output mode.

Gated Mode (TOUT = "0", DOUT = "1"). In this mode the prescaler is decremented by the Timer clock input (f_{INT} divided by 12) but ONLY when the signal at TIMER pin is held high (giving a pulse width measurement potential). This mode is selected by the TOUT bit in TSCR register cleared to "0" (i.e. as input) and DOUT bit set to "1".

Clock Input Mode (TOUT = "0", DOUT = "0"). In this mode the TIMER pin is an input and the prescaler is decremented on rising edge. The maximum input frequency that can be applied to the external pin in this mode is 1/4 of the internal frequency when the processor is running but can be higher when the WAIT mode is entered.

Output Mode (TOUT = "1", DOUT = data out). The TIMER pin is connected to the DOUT latch. Therefore the timer prescaler is clocked by the prescaler clock input (f_{INT}÷12).

The user can select the desired prescaler division ratio through the PS2, PS1, PS0 bits. When TCR count reaches 0, it sets the TMZ bit in the TSCR. The TMZ bit can be tested under program control to perform a timer function whenever it goes high. The low-to-high TMZ bit transition is used to latch the DOUT bit of the TSCR and pass it to TIMER pin. This operating mode allows external signal generation on the TIMER pin.

Table 9. Timer Operating Modes

TOUT	DOUT	Timer Pin	Timer Function
0	0	Input	Event Counter
0	1	Input	Input Gated
1	0	Output	Output "0"
1	1	Output	Output "1"

Timer Interrupt

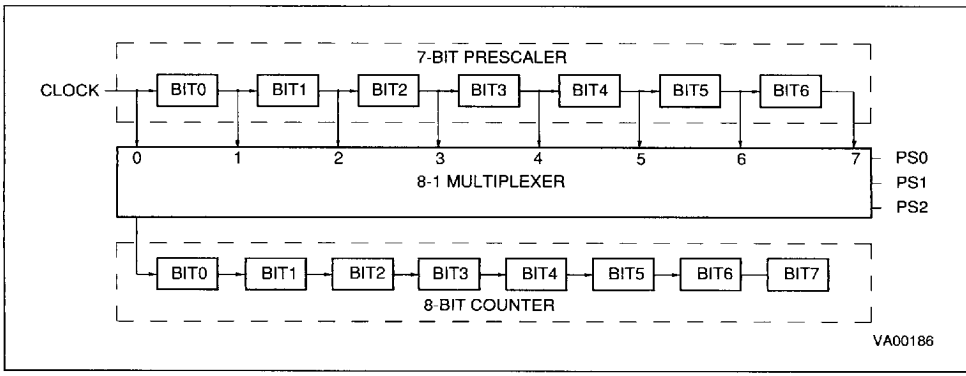
When the counter register decrements to zero and the software controlled ETI (Enable Timer Interrupt) bit is set to one then an interrupt request associated to interrupt vector #3 is generated. When the counter decrements to zero also the TMZ bit in the TSCR register is set to one.

Notes:

On ST6210B,15B, ST6220B, 25B the user can select the availability of an on-chip pull-up at TIMER pin as ROM mask option (see option list at the end of the datasheet).

TMZ is set when the counter reaches 00h ; however, it may be set by writing 00h in the TCR register or setting bit 7 of the TSCR register. TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine. After reset, the 8-bit counter register is loaded to FFh while the 7-bit prescaler is loaded to 7Fh , and the TSCR register is cleared which means that Timer is stopped (PSI="0") and the timer interrupt is disabled.

Figure 28. Timer Working Principle



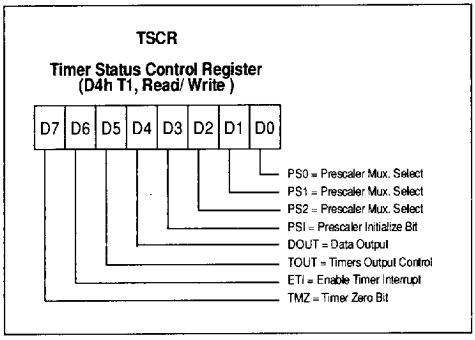
TIMER (Continued)

If the Timer is programmed in output mode, DOUT bit is transferred to the TIMER pin when TMZ is set to one (by software or due to counter decrement). When TMZ is high, the latch is transparent and DOUT is copied to the timer pin. When TMZ goes low, DOUT is latched.

A write to the TCR register will predominate over the 8-bit counter decrement to 00h function, i.e. if a write and a TCR register decrement to 00h occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00h again. The values of the TCR and the PSC registers can be read accurately at any time.

Timer Registers

Figure 29. Timer Status Control Register



TMZ. Low-to-high transition indicates that the timer count register has decrement to zero. This bit must be cleared by user software before starting with a new count.

ETI. This bit, when set, enables the timer interrupt request (vector #3). If ETI=0 the timer interrupt is disabled. If ETI=1 and TMZ=1 an interrupt request is generated.

TOUT. When low, this bit selects the input mode for the TIMER pin. When high the output mode is selected.

DOUT. Data sent to the timer output when TMZ is set high (output mode only). Input mode selection (input mode only).

PSI. Used to initialize the prescaler and inhibit its counting. When PSI="0" the prescaler is set to 7Fh and the counter is inhibited. When PSI="1" the prescaler is enabled to count downwards. As long as PSI="0" both counter and prescaler are not running.

PS2, PS1, PS0. These bits select the division ratio of the prescaler register.

Table 10. Prescaler Division Factors

PS2	PS1	PS0	Divided by
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Figure 31. Timer Counter Register

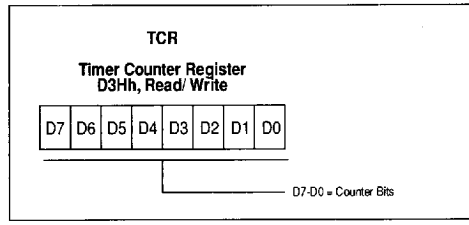
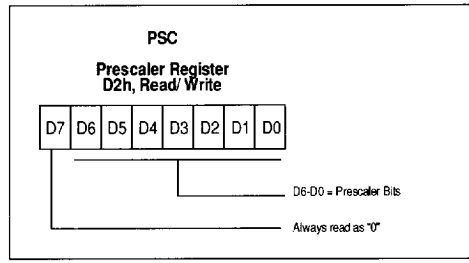


Figure 30. Prescaler Register



DIGITAL WATCHDOG

The digital Watchdog of the ST6210B/15B device consists of a down counter that can be used to provide a controlled recovery from a software upset.

The Watchdog generates a system reset when the counter passes 00h. User software can prevent the reset by reloading the counter. User software should therefore be written in such a way that the counter is regularly reloaded as long as the software runs correctly. In the case of software upset (e.g. infinite loop or power supply fail), user software should not reload the counter so it will pass 00h and reset the MCU.

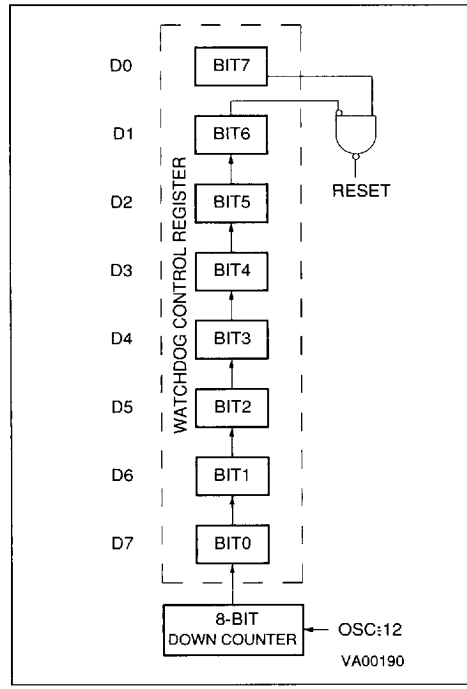
The Watchdog activation (hardware or software) is user selectable by mask option. If the hardware option is selected the Watchdog is automatically initialized after reset so that this function does not need to be activated by the user program.

The Watchdog uses one data space register (DWDR location D8h). The Watchdog register is set to FEh on reset and counts down when activated. The Watchdog time can be adjusted through the value reloaded into the DWDR register. Only the 6 MSbits are significant. This gives the possibility to generate a reset in a time between 3072 to 196608 clock cycles in 64 possible steps (with a clock frequency of 8MHz this means from 384µs to 24.576ms). The reset is prevented if the register is reloaded before bits 2-7 decrement from all zeros to all ones.

The WATCHDOG ACTIVATION can be software (it is launched by software) or hardware (it automatically starts counting down after reset). When the software activation is selected, the watchdog can be launched by setting to 1 bit 0 of the Digital Watchdog Register after bit SR of this register has been set to 1. Once activated, the watchdog cannot be stopped by software: a full external reset is mandatory.

The STOP instruction is inhibited as soon as the watchdog is active. A WAIT instruction is processed instead and the watchdog continues to countdown. The NMI pin allows, in addition to the interrupt generation, to control the execution of the STOP instruction. It is inhibited when NMI is low (a WAIT instruction is processed instead). When NMI is high, a STOP instruction freezes the watchdog counter before entering the STOP mode. When the micro exits from the STOP mode (for example, when an NMI interrupt is generated), the watchdog resumes activity.

Figure 32. Watchdog Working Principle



Note:

When the software activation is selected and the watchdog is not activated, the 7 MSbits of the counter can be used to perform timer functions. Care must be taken as the Watchdog bits are in reverse order.

Bit 1 of the Watchdog register (set to one at reset) can be used to generate a software reset if cleared to zero.

C. This is the Watchdog activation bit. If hardware option is selected, it is forced high and the user cannot change it (the Watchdog is always active). When the software option is selected, the Watchdog function is activated by setting C to 1. It can then be cleared only by a system reset and is not affected by the STOP Mode Control option. When C is kept low the counter can be used as a 7-bit timer.

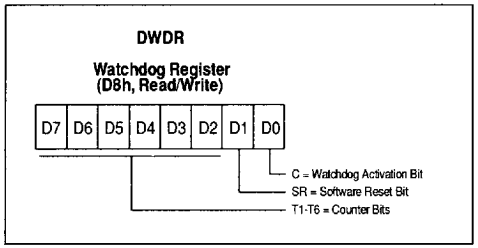
DIGITAL WATCHDOG (Continued)

When cleared to zero it allows the use of the counter as a 7-bit timer. This bit is cleared on reset.

SR. This bit is set to one during the reset and will generate a software reset if cleared to zero. When C = "0" (watchdog disabled) it is the MSB of the 7-bit timer.

T1-T6. These are the watchdog counter bits. It must be noted that D7 (T1) is the LSB of the counter and D2 (T6) is the MSB of the counter.

Figure 33. Digital Watchdog Register



Application Notes

The hardware activation option is very useful when the external circuitry may inject noises on the reset pin, where there is an unstable supply voltage, or RF influence or other similar phenomena. If the Watchdog software activation is selected and the Watchdog is not used during power-on reset external noise may cause the undesired activation of the Watchdog with a generation of an unexpected reset. To avoid this risk, two additional instructions, that check the state of the watchdog and eventually reset the chip are neededwithin the first 27 instructions, after the reset. These instructions are:

```
jrx 0, WD, #+3
ldi WD, 0FDH
```

These instructions should be executed at the very beginning of the customer program.

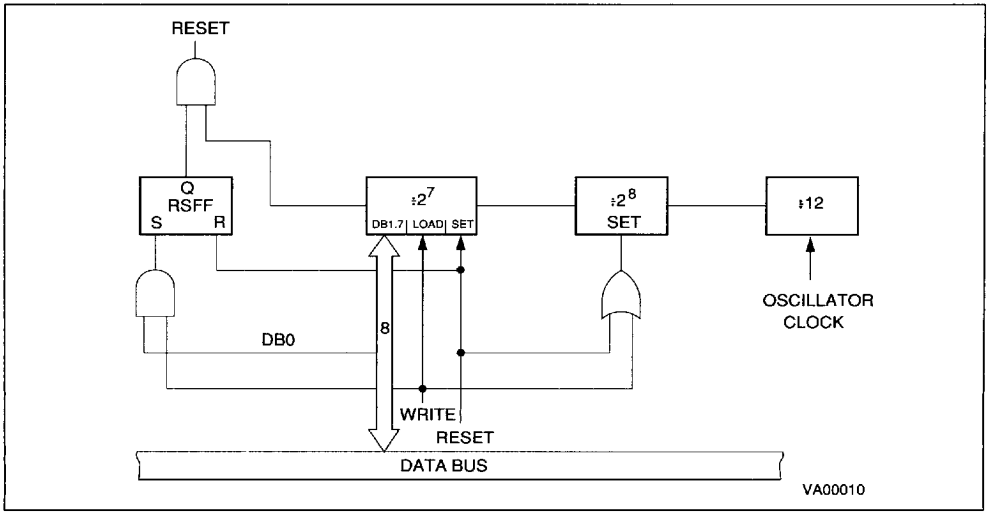
If the Watchdog is used (both hardware or software activated), during power-on reset the Watchdog register may be set to a low value, that could give a reset after 28 instructions earliest. To avoid undesired resets, the Watchdog must be set to the desired value within the first 27 instructions, the best is to put at the very beginning.

Alternatively the normal legal state can be checked with the following short routine:

```
ldi a, 0FEH
and a, WD
cpi a, 0FEH
jrz #+3
ldi WD, 0FDH
```

This sequence is recommended for security applications, where possible stack confusion error loops must be avoided and the Watchdog must only be refreshed after extensive checks.

Figure 34. Digital Watchdog Block Diagram



8-BIT A/D CONVERTER

The A/D converter of ST621xB,2xB devices is an 8-bit analog to digital converter with up to 8 (PB0-PB7 on ST6210B, ST6220B) and up to 16 (PA4-PA7, PB0-PB7, PC4-PC7 on ST6215B, ST6225B) analog inputs (as alternate functions of I/O lines) offering 8-bit resolution with a typical conversion time of 70ms (clock frequency of 8MHz).

The A/D peripheral converts the input voltage by a process of successive approximations using a clock frequency derived from the oscillator with a division factor of twelve. With an oscillator clock frequency less than 1.2MHz, the A/D converter accuracy is decreased.

The selection of the pin signal that has to be converted is done by configuring the related I/O line as analog input through the I/O ports option and data registers (refer to I/O ports description for additional information). Only one I/O line must be configured as analog input at a time. The user must avoid the situation in which more than one I/O pin is selected to be analog input to avoid malfunction of the ST62xx.

The ADC uses two registers in the data space: the ADC data conversion register which stores the conversion result and the ADC control register used to program the ADC functions.

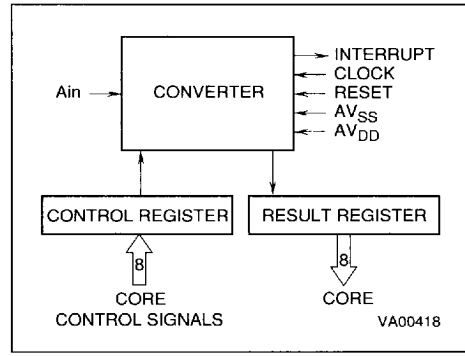
A conversion is started by writing a "1" to the Start bit (STA) in the ADC control register. This automatically clears (resets to "0") the End Of Conversion Bit (EOC). When a conversion has been finished this EOC bit is automatically set to "1" in order to flag that conversion is complete and that the data in the ADC data conversion register is valid. Each conversion has to be separately initiated by writing to the STA bit.

The STA bit is continually being scanned so that if the user sets it to "1" while a previous conversion is in progress then a new conversion is started before the previous one has been completed.The start bit (STA) is a write only bit, any attempt to read it will show a logical "0".

The A/D converter has a maskable interrupt associated to the end of conversion. This interrupt is associated to the interrupt vector #4 and occurs when the EOC bit is set, i.e. when a conversion is completed. The interrupt is masked using the EAI (interrupt mask) bit in the control register.

The power consumption of the device can be reduced by turning off the ADC peripheral. That is achieved when the PDS bit in the ADC control register is cleared to "0". If PDS="1", the A/D is supplied and enabled for conversion. This bit must be set at least one instruction before the beginning of the conversion to allow the stabilization of the

Figure 35. A/D Converter Block Diagram



A/D converter. This action is needed also before entering the WAIT instruction as the A/D comparator is not automatically disabled by the WAIT mode

During reset any conversion in progress is stopped, the control register is reset to 40h and the A/D interrupt is masked (EAI=0).

Notes:

The ST62xx A/D converter does not feature a sample and hold. The analog voltage to be measured should therefore be stable during the conversion time. Variation should not exceed±1/2 LSB for the best accuracy in measurement. A low pass filter can be used at the analog input pins to reduce input voltage variation during the conversion.

When selected as an analog channel, the input pin is internally connected to a capacitor Cad of typically 12pF. For maximum accuracy, this capacitor must be fully loaded at conversion start. In the worst case, conversion starts one instruction (6.5 µs) after the channel has been selected. In the worst case conditions, the impedance ASI of the analog voltage source is calculated using the following formula :

$$6.5\mu s = 9 \times Cad \times ASI$$

(capacitor loaded over 99.9%), ie 30 kΩ including 50% guardland. ASI can be higher if Cad has been loaded for a longer time by adding instructions before conversion start (adding more than 26 CPU cycles is meaningless).

Since the ADC is on the same chip as the microprocessor the user should not switch heavily loaded output signals during conversion if high precision is needed. This is because such switching will affect the supply voltages which are used for comparisons.

8-BIT A/D CONVERTER (Continued)

The accuracy of the conversion depends on the quality of the power supply voltages (V_{DD} and V_{SS}). The user must specially take care of applying regulated reference voltage on the V_{DD} and V_{SS} pins (the variation of the power supply voltage must be inferior to 5V/ms). This implies in particular that a suitable decoupling capacitor is used at V_{DD}.

The converter can resolve the input voltage with a resolution of:

$$\frac{V_{DD} - V_{SS}}{256}$$

The Input voltage (Ain) which has to be converted must be constant for 1µs before conversion and remain constant during the conversion.

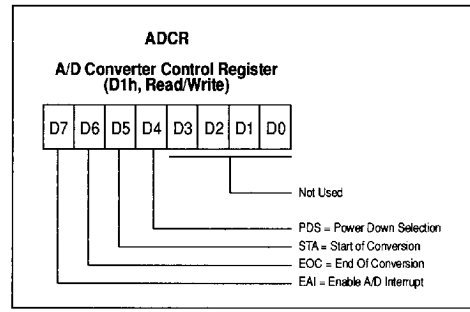
The resolution of the conversion can be improved if the power supply voltage (V_{DD}) of the microcontroller becomes lower.

In order to optimize the resolution of the conversion, the user can configure the microcontroller in the WAIT mode because this mode allows the minimization of the noise disturbances and the variations of the power supply voltages due to the switching of the outputs. Nevertheless, it must be take care of executing the WAIT instruction as soon as possible after the beginning of the conversion because the execution of the WAIT instruction may provide a small variation of the V_{DD} voltage (the negative effect of this variation is minimized at the beginning of the conversion because the latter is less sensitive than the end of the conversion when the less significant bits are determined).

The best configuration from a accuracy point of view is the WAIT mode with the Timer stopped. Indeed, only the ADC peripheral and the oscillator are still working. The MCU has to be wake-up from the WAIT mode by the interrupt of the ADC peripheral at the end of the conversion. It must be noticed that the wake-up of the microcontroller could be done also with the interrupt of the TIMER, but in this case, the Timer is working and some noise could disturb the converter in terms of accuracy.

EAI. If this bit is set to one the A/D interrupt (vector #4) is enabled, when EAI=0 the interrupt is disabled.

Figure 36. A/D Converter Control Register



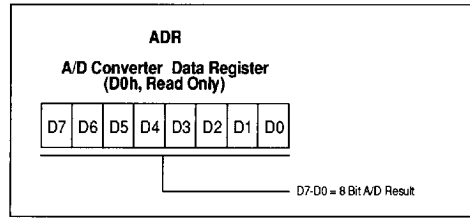
EOC. *Read Only*; This read only bit indicates when a conversion has been completed. This bit is automatically reset to zero when the STA bit is written. If the user is using the interrupt option then this bit can be used as an interrupt pending bit. Data in the data conversion register are valid only when this bit is set to one.

STA. *Write Only*; Writing a "1" in this bit will start a conversion on the selected channel and automatically reset to zero the EOC bit. If the bit is set again when a conversion is in progress, the present conversion is stopped and a new one will take place. This bit is write only, any attempt to read it will show a logical zero.

PDS. This bit activates the A/D converter if set to "1". Writing a zero into this bit will put the ADC in power down mode (idle mode).

D3-D0. Not used

Figure 37. A/D Converter Data Register



SOFTWARE DESCRIPTION

The ST62xx software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short to provide byte efficient programming capability. The ST62xx core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space. The carry bit is stored with the value of the bit when the SET or RES instruction is processed.

Addressing Modes

The ST62xx core has nine addressing modes which are described in the following paragraphs. The ST62xx core uses three different address spaces : Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains the Accumulator, the X,Y,V and W registers, peripheral and Input/Output registers, the RAM locations and Data ROM locations (for storage of tables and constants). Stack space contains six 12-bit RAM cells used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte that is processed by the instruction is stored in the location that follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data Space memory with a single two-byte instruction.

Short Direct. The core can address the four RAM registers X,Y,V,W (locations 80h, 81h, 82h, 83h) in the short-direct addressing mode . In this case, the instruction is only one byte and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note that 80h and 81h are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) that use the extended addressing mode are able to branch to any address of the 4K bytes Program space.

An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to +16 locations around the address of the relative instruction. If the condition is not true, the instruction that follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained in adding the three most significant bits that characterize the kind of the test, one bit that determines whether the branch is a forward (when it is 0) or backward (when it is 1) branch and the four less significant bits that give the span of the branch (0h to Fh) that must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct. In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 locations of Data space memory can be set or cleared.

Bit Test & Branch. The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range of -126 to +129. This displacement can be determined using a label, which is converted by the assembler.

Indirect. In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80h,81h). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

SOFTWARE DESCRIPTION (Continued)

Instruction Set

The ST62xx core has a set of 40 basic instructions. When these instructions are combined with nine addressing modes, 244 usable opcodes can be obtained. They can be divided into six different types:load/store, arithmetic/logic, conditional branch, control instructions, jump/call, bit manipulation. The following paragraphs describe the different types.

All the instructions within a given type are presented in individual tables.

Load & Store. These instructions use one,two or three bytes in relation with the addressing mode. One operand is the Accumulator for LOAD and the other operand is obtained from data memory using one of the addressing modes.

For Load Immediate one operand can be any of the 256 data space bytes while the other is always immediate data.

Table 12. Load & Store Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register
Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Arithmetic and Logic. These instructions are used to perform the arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while the other can be either a data space memory content or an immediate value in relation with the addressing mode. In CLR, DEC, INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator.

Table 13. Arithmetic & Logic Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	*
AND A, (Y)	Indirect	1	4	Δ	*
AND A, rr	Direct	2	4	Δ	*
ANDI A, #N	Immediate	2	4	Δ	*
CLR A	Short Direct	2	4	Δ	Δ
CLR r	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y. Indirect Register Pointers, V & W Short Direct Registers
#. Immediate data (stored in ROM memory)
rr. Data space register
Δ. Affected
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Conditional Branch. The branch instructions achieve a branch in the program when the selected condition is met.

Bit Manipulation Instructions. These instructions can handle any bit in data space memory. One group either sets or clears. The other group (see Conditional Branch) performs the bit test branch operations.

Control Instructions. The control instructions control the MCU operations during program execution.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutines call inside the whole program space.

Table 14. Conditional Branch Instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b. 3-bit address
e. 5 bit signed displacement in the range -15 to +16
ee. 8 bit signed displacement in the range -126 to +129
rr. Data space register
Δ. Affected
*. Not Affected

Table 15. Bit Manipulation Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b. 3-bit address;
rr. Data space register;
*. Not Affected

Table 16. Control Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1. This instruction is deactivated and a WAIT is automatically executed instead of a STOP if the watchdog function is selected.
Δ. Affected
*. Not Affected

Table 17. Jump & Call Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc.12-bit address;
*. Not Affected

SOFTWARE DESCRIPTION (Continued)

Opcode Map Summary. The following table contains an opcode map for the instructions used by ST6

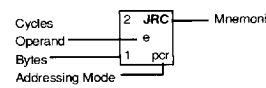
LOW / HI	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	LOW / HI
0 0000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b0,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b0,rr 2 b.d	2 JRZ e 1 pcr	4 LDI rr,nn 3 imm	2 JRC e 1 pcr	4 LD a,(y) 1 ind	0 0000
1 0001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b0,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC x 1 sd	2 JRC e 1 prc	4 LDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b0,rr 2 b.d	2 JRZ e 1 pcr	4 DEC x 1 sd	2 JRC e 1 pcr	4 LD a,rr 2 dir	1 0001
2 0010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b4,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 CP a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b4,rr 2 b.d	2 JRZ e 1 pcr	4 COM a 1 inh	2 JRC e 1 pcr	4 CP a,(y) 1 ind	2 0010
3 0011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b4,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,x 1 sd	2 JRC e 1 prc	4 CPI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b4,rr 2 b.d	2 JRZ e 1 pcr	4 LD x,a 1 sd	2 JRC e 1 pcr	4 CP a,rr 2 dir	3 0011
4 0100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b2,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 ADD a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b2,rr 2 b.d	2 JRZ e 1 pcr	2 RETI 1 inh	2 JRC e 1 pcr	4 ADD a,(y) 1 ind	4 0100
5 0101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b2,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC y 1 sd	2 JRC e 1 prc	4 ADDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b2,rr 2 b.d	2 JRZ e 1 pcr	4 DEC y 1 sd	2 JRC e 1 pcr	4 ADD a,rr 2 dir	5 0101
6 0110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b6,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 INC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b6,rr 2 b.d	2 JRZ e 1 pcr	2 STOP 1 inh	2 JRC e 1 pcr	4 INC (y) 1 ind	6 0110
7 0111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b6,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,y 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b6,rr 2 b.d	2 JRZ e 1 pcr	4 LD y,a 1 sd	2 JRC e 1 pcr	4 INC rr 2 dir	7 0111
8 1000	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b1,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 LD (x),a 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b1,rr 2 b.d	2 JRZ e 1 pcr	#	2 JRC e 1 pcr	4 LD (y),a 1 ind	8 1000
9 1001	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b1,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC v 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b1,rr 2 b.d	2 JRZ e 1 pcr	4 DEC v 1 sd	2 JRC e 1 pcr	4 LD rr,a 2 dir	9 1001
A 1010	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b5,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 AND a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b5,rr 2 b.d	2 JRZ e 1 pcr	4 RLC a 1 inh	2 JRC e 1 pcr	4 AND a,(y) 1 ind	A 1010
B 1011	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b5,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,v 1 sd	2 JRC e 1 prc	4 ANDI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b5,rr 2 b.d	2 JRZ e 1 pcr	4 LD v,a 1 sd	2 JRC e 1 pcr	4 AND a,rr 2 dir	B 1011
C 1100	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b3,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 SUB a,(x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b3,rr 2 b.d	2 JRZ e 1 pcr	2 RET 1 inh	2 JRC e 1 pcr	4 SUB a,(y) 1 ind	C 1100
D 1101	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b3,rr,ee 3 bt	2 JRZ e 1 pcr	4 INC w 1 sd	2 JRC e 1 prc	4 SUBI a,nn 2 imm	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b3,rr 2 b.d	2 JRZ e 1 pcr	4 DEC w 1 sd	2 JRC e 1 pcr	4 SUB a,rr 2 dir	D 1101
E 1110	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRR b7,rr,ee 3 bt	2 JRZ e 1 pcr	#	2 JRC e 1 prc	4 DEC (x) 1 ind	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 RES b7,rr 2 b.d	2 JRZ e 1 pcr	2 WAIT 1 inh	2 JRC e 1 pcr	4 DEC (y) 1 ind	E 1110
F 1111	2 JRNZ e 1 pcr	4 CALL abc 2 ext	2 JRNC e 1 pcr	5 JRS b7,rr,ee 3 bt	2 JRZ e 1 pcr	4 LD a,w 1 sd	2 JRC e 1 prc	#	2 JRNZ e 1 pcr	4 JP abc 2 ext	2 JRNC e 1 pcr	4 SET b7,rr 2 b.d	2 JRZ e 1 pcr	4 LD w,a 1 sd	2 JRC e 1 pcr	4 DEC rr 2 dir	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages.

For proper operation it is recommended that V_I and V_O must be higher than V_{SS} and smaller V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriated logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from :

$T_j = T_A + PD \times RthJA$

Where : T_A = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = $I_{DD} \times V_{DD}$ (chip internal power).

Pport = Port power dissipation (determinated by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	V_{SS} - 0.3 to V_{DD} + 0.3 (1)	V
V_O	Output Voltage	V_{SS} - 0.3 to V_{DD} + 0.3 (1)	V
I_O	Current Drain per Pin Excluding V_{DD}, V_{SS}	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, V_{DD} = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
IV_{DD}	Total Current into V_{DD} (source)	50 (2)	mA
IV_{SS}	Total Current out of V_{SS} (sink)	50 (2)	mA
Tj	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes :

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device . This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.
- (2) The total current through ports A and B combined may not exceed 50mA. The total current through port C may not exceed 50mA. If the application is designed with care and observing the limits stated above, total current may reach 100mA.

THERMAL CHARACTERISTIC

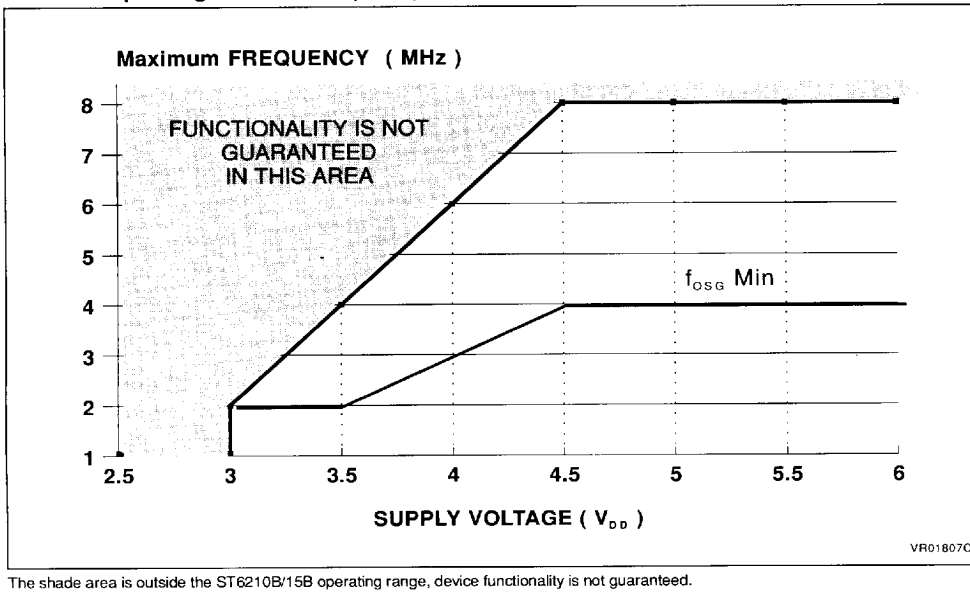
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP28			55	°C/W
		PDIP20			60	
		PSO28			75	
		PSO20			80	

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version 1 Suffix Version	-40 0		85 70	°C
V_{DD}	Operating Supply Voltage	f_{OSC}= 2MHz f_{INT} = 2MHz	3.0		6.0	V
		f_{OSC}= 4MHz f_{INT} = 4MHz	3.5		6.0	V
		f_{OSC} = 8MHz f_{INT} = 8MHz	4.5		6.0	V
f_{INT}	Internal Frequency (3)	V_{DD} = 3V; OSG disabled V_{DD}= 4.5V;OSG disabled	0 0		2.0 8.0	MHz MHz
I_{INJ+}	Pin Injection Current (positive) Digital Input (1) Analog Inputs(2)	V_{DD} = 4.5 to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input (1) Analog Inputs	V_{DD} = 4.5 to 5.5V			-5	mA

Notes :
1. A current of ± 5mA can be forced on each pin of the digital section without affecting the functional behaviour of the device. For a positive current injected into one pin, a part of this current (– 10%) can be expected to flow from the neighbouring pins.
2. If a total current of +1 mA is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 1mA, all the resulting conversions are shifted by +1 LSB. If a total positive current is flowing into the single analog channel or if the total current flowing into all the analog inputs is of 5mA, all the resulting conversions are shifted by +2 LSB.
3. An internal frequency above 1MHz is recommended for reliable A/D results.

Maximum Operating FREQUENCY (Fmax) Versus SUPPLY VOLTAGE (V_{DD})



The shade area is outside the ST6210B/15B operating range, device functionality is not guaranteed.

DC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage TIMER,NMI,RESET pins				V_{DD} x 0.3	V
V_{IH}	Input High Level Voltage TIMER,NMI,RESET pins		V_{DD} x 0.7			V
V_{Hys}	Hysteresis Voltage (4) All Inputs	V_{DD}= 5V V_{DD}= 3V		1 0.5		V
V_{OL}	Low Level Output Voltage TIMER pin	I_{OL} = + 5.0mA			0.2 x VDD	V
V_{OH}	High Level Output Voltage TIMER pin	I_{OH} = – 5.0mA	V_{DD} x 0.65			V
R_{PU}	Pull-up TIMER, NMI pins		50	100	200	kΩ
I_{IL} I_{IH}	Input Leakage Current(1) TIMER, NMI pins	V_{IN}= V_{SS} V_{IN}= V_{DD}		0.1	1.0	µA
I_{IL} I_{IH}	Input Leakage Current RESET pin	V_{IN}=V_{DD}; Watchdog Res. V_{IN}=V_{DD}; No Watch. Res. V_{IN}=V_{SS}; External Res.	 -8	 -16	1 10 -30	mA µA µA
I_{DD}	Supply Current in RESET Mode	V_{RESET}= V_{SS} f_{OSC}= 8MHz			3.5	mA
	Supply Current in RUN Mode (2)	V_{DD} = 5.0V f_{INT}=8MHz V_{DD} = 5.0V f_{INT}=f_{LFAO} V_{DD} = 3.0V f_{INT}=2MHz			3.5 TBD TBD	mA
	Supply Current in WAIT Mode (3)	V_{DD}= 5.0V f_{INT}=8MHz V_{DD} = 5.0V f_{INT}=f_{LFAO} V_{DD}= 3.0V f_{INT}=2MHz			1.50 TBD TBD	mA
	Supply Current in STOP Mode (3)	I_{LOAD}= 0mA V_{DD}= 5.0V			10	µA

Notes :
1. Only when pull-ups are not inserted
2. All peripherals running
3. A/D Converter in Stand-by
4. Hysteresis voltage between switching levels

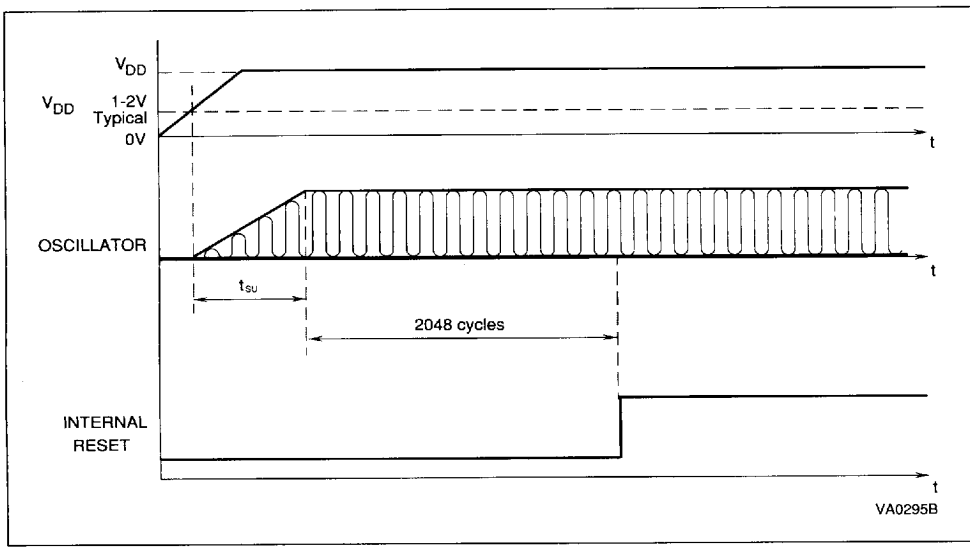
AC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

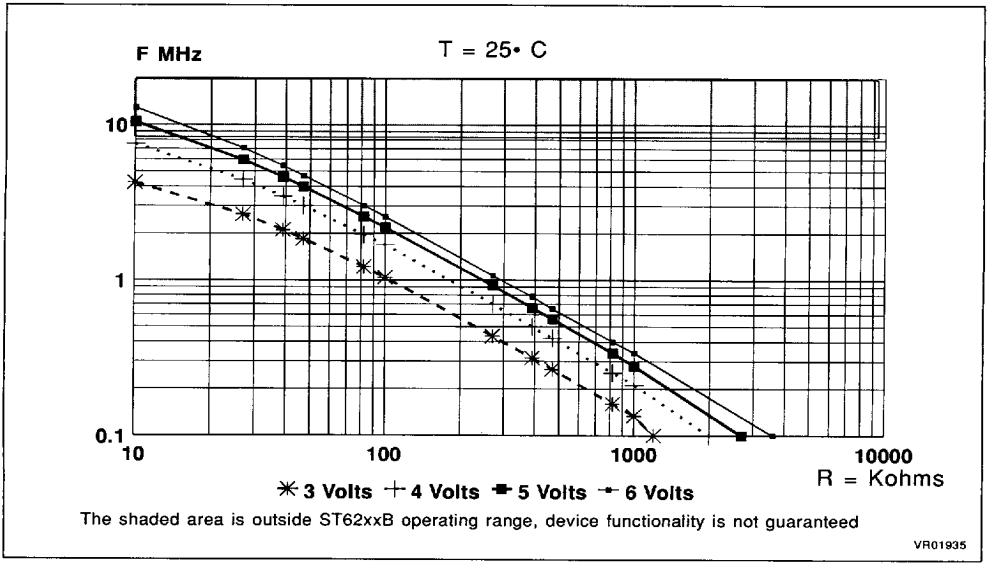
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
f_{OSC}	Oscillator Frequency	V_{DD} = 3.0V; OSG disabled V_{DD} = 4.5V; OSG disabled			2 8	MHz
f_{OSG}	Maximum internal frequency with OSG enabled	VDD = 3.0V V_{DD} = 4.5V	2 4			MHz
f_{LFAO}	Low Frequency Auxiliary Oscillator		200	400	800	kHz
t_{SU}	Oscillator Start-up Time at Power On (2)	Ceramic Resonator C_{L1} = C_{L2} = 22pF		5	100	ms
t_{SUS}	Oscillator STOP mode Recovery Time (2)	8MHz Ceramic Resonator CL1=C_{L2}=22pF		0.2	100	
		8MHz Quartz CL1=C_{L2}=22pF		10	100	
t_{REC}	Supply Recovery Time (1)		100			
T_{WR}	Minimum Pulse Width (V_{DD} = 5V) RESET pin NMI pin		 100 100			ns
C_{IN}	Input Capacitance	All Inputs Pins			10	pF
C_{OUT}	Output Capacitance	All Outputs Pins			10	pF

Note:
1. Period for which V_{DD} has to be connected at 0V to allow internal Reset function at next power-up.
2. See Figure 38. This value is highly dependent on the Ceramic Resonator or Quartz Crystal used in the application.

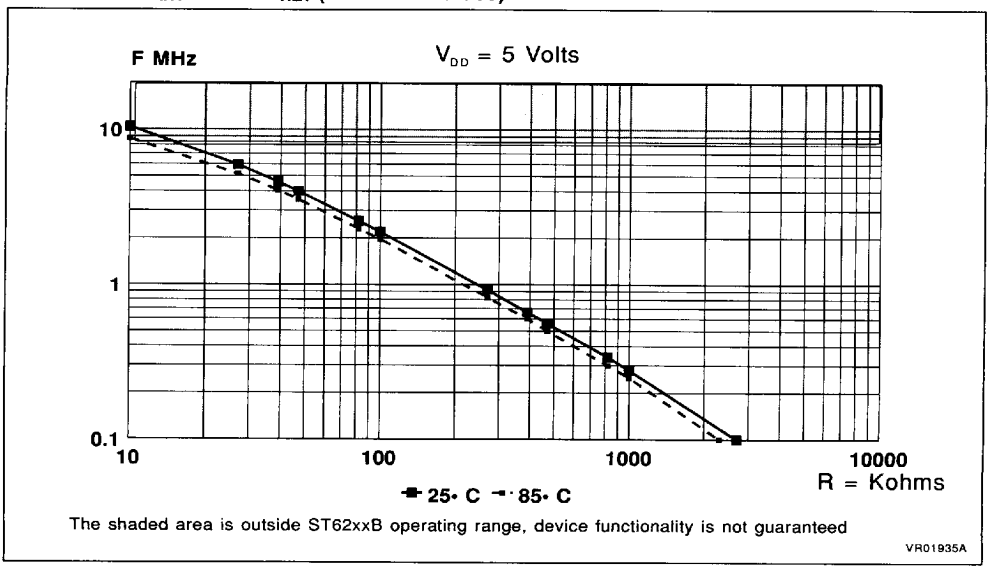
Figure 38.Power On Reset



RC Oscillator. f_{INT} versus R_{NET} (Indicative Values)



RC Oscillator. f_{INT} versus R_{NET} (Indicative Values)

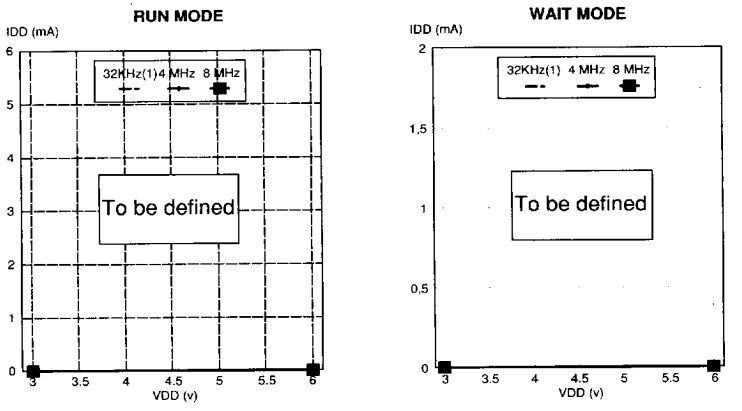


SGS-THOMSON MICROELECTRONICS

ELECTRICAL CHARACTERISTICS (Continued)

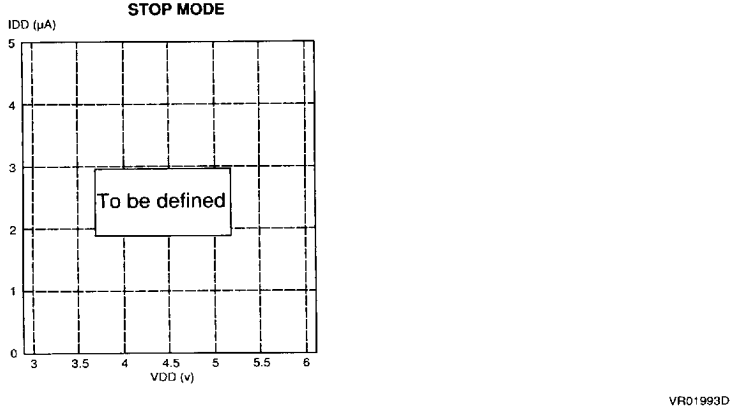
CURRENT CONSUMPTION

IDD Current Versus Supply Voltage
Typical Values(T_A : +85°C)



Note 1. Using the network described in the Application Note AN673

IDD Current Versus Supply Voltage
Typical Values(T_A : +85°C)



I/O PORT CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IL}	Input Low Level Voltage	I/O Pins			0.3x V_{DD}	V
V_{IH}	Input High Level Voltage	I/O Pins	0.7x V_{DD}			V
V_{OL}	Low Level Output Voltage	V_{DD}= 5.0V I_{OL}= 10µA , All I/O Pins I_{OL}= 5mA , Standard I/O I_{OL}= 10mA } PA0-PA3 I_{OL}= 20mA }			0.1 0.8 0.8 1.3	V
V_{OH}	High Level Output Voltage	I_{OH}= – 10µA I_{OH}= – 5mA, V_{DD}= 5.0V I_{OH}= – 1.5mA, V_{DD}= 3.0V	V_{DD}-0.1 3.5 2.0			V
I_{IL} I_{IH}	Input Leakage Current I/O Pins (pull-up resistor off)	Vin= V_{DD} or V_{SS} V_{DD}= 3.0V V_{DD}= 5.5V		0.1 0.1	1.0 1.0	µA
R_{PU}	Pull-up Resistor	Vin= 0V; All I/O Pins	50	100	200	kΩ

TIMER CHARACTERISTICS

(T_A = -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
t_{RES}	Resolution		$\frac{12}{f_{INT}}$			s
f_{IN}	Input Frequency on TIMER Pin	Stop Mode Run and Wait Modes			2 $\frac{f_{INT}}{8}$	MHz MHz
t_W	Pulse Width at TIMER Pin	V_{DD} = 3.0V V_{DD} = 4.5V V_{DD} = 5.5V	1 125 125			µs ns ns

A/D CONVERTER CHARACTERISTICS

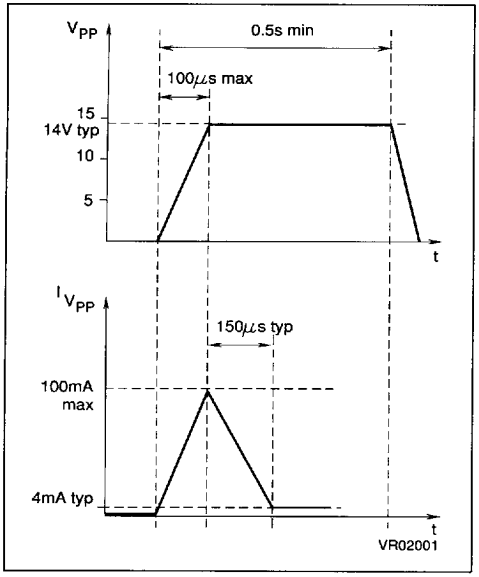
(T_A= -40 to +85°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Res	Resolution			8		Bit
A_{TOT}	Total Accuracy (1) (2)	f_{OSC} > 1.2MHz f_{OSC} > 32kHz		±1	±2 ±4	LSB
t_C	Conversion Time	f_{OSC} = 8MHz		70		µs
V_{AN}	Conversion Range		V_{SS}		V_{DD}	V
ZIR	Zero Input Reading	Conversion result when $V_{IN} = V_{SS}$	00			Hex
FSR	Full Scale Reading	Conversion result when $V_{IN} = V_{DD}$			FF	Hex
AD_I	Analog Input Current During Conversion	V_{DD}= 4.5V			1.0	µA
AC_{IN} (3)	Analog Input Capacitance			2	5	pF
ASI	Analog Source Impedance	Analog Channel switched just before conversion start (4)			30	kΩ

Notes:
1. Noise at V_{DD}, V_{SS} <10mV
2. With oscillator frequencies less than 1MHz, the A/D Converter accuracy is decreased.
3. Excluding Pad Capacitance.
4. ASI can be increased as long as the load of the A/D Converter input capacitor is ensured before conversion start.

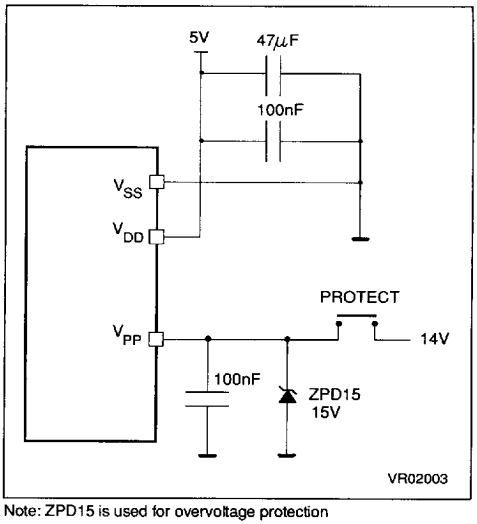
READ PROTECTION FUSE

If the ROM READOUT PROTECTION option is selected as enabled, the following waveform must be applied at the V_{PP} pin for the fuse to be blown:



The following circuit can be used for this purpose:

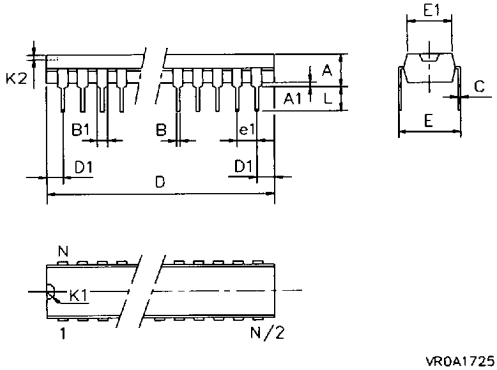
Figure 39. Example of READOUT PROTECTION fuse programming circuit



Note: ZPD15 is used for overvoltage protection

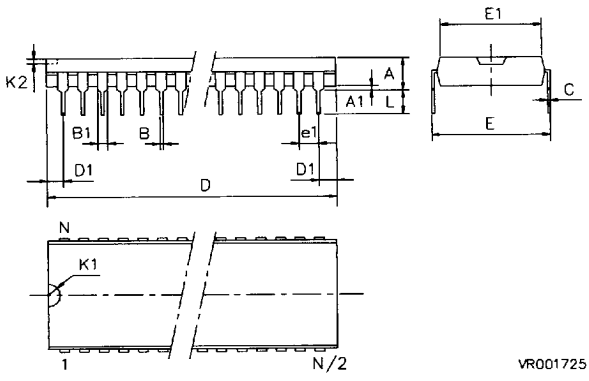
PACKAGE MECHANICAL DATA

Figure 40. 20-Pin Dual in Line Plastic (B), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.93			0.155
A1	0.254			0.010		
B			0.45			0.017
B1	1.39		1.65	0.055		0.065
C			0.25			0.009
D			25.4			1.000
D1			1.34			0.053
E		8.5			0.334	
E1			7.1			0.279
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L		3.30			0.129	
e1		2.54			0.10	
Number of Pins						
N	20					

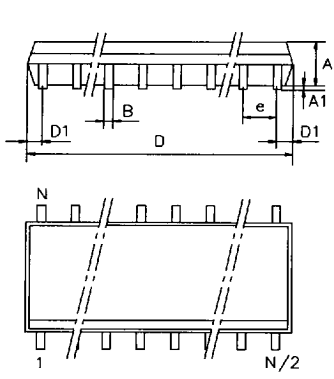
Figure 41. 28-Pin Dual in Line Plastic (B), 600-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		4.8	0.086		0.189
A1	0.51		1.77	0.010		0.069
B	0.38		0.58	0.015		0.023
B1	0.97		1.52	0.055		0.065
C	0.2		0.3	0.008		0.009
D	35.06		36.22	1.400		1.425
D1	–	–	–	–	–	–
E			16.3			0.641
E1		12.9			0.508	
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	3.18		4.44	1.25		0.174
e1		2.54			0.10	
Number of Pins						
N	28					

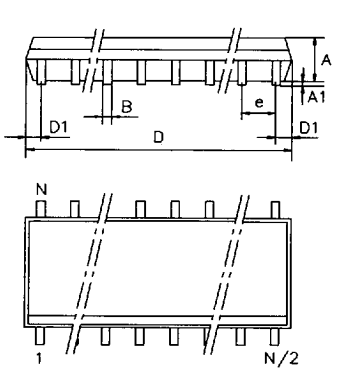
PACKAGES MECHANICAL DATA (Continued)

Figure 42. 20-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	12.6		13.0	.4961		.5118
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	20					

Figure 43. 28-Lead Small Outline Plastic (M), 300-Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.05		2.55	0.081		0.10
A1	0.1		0.3	0.004		.0118
B	0.35		0.49	.0138		.0192
C	0.23		0.32	.0091		.0125
D	17.7		18.1	.6969		.7125
D1	–	–	–	–	–	–
E	10.0		10.65	0.394		0.419
E1	7.40		7.60	.2914		.2992
E2	–	–	–	–	–	–
L	0.40		1.27	0.016		0.050
e		1.27			0.05	
α	–	–	–	–	–	–
Number of Pins						
N	28					

ORDERING INFORMATION

The following chapter deals with the procedure for transfer customer codes to SGS-THOMSON.

Communication of the customer code. Customer code is made up of the ROM contents and the list of the selected mask options. The ROM contents are to be sent on one diskette with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected mask options are communicated to SGS-THOMSON using the correctly filled OPTION LIST appended.

Listing Generation & Verification. When SGS-THOMSON receives the diskette, a computer listing is generated from it. This listing refers exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask.

SGS-THOMSON sales organization will provide detailed information on contractual points.

Table 18. ROM Memory Map

ST6210B,ST6215B (2K ROM Devices)

Device Address	Description
0000h-087Fh	Reserved (1)
0880h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved (1)
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved (1)
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

ST6220B,ST6225B (4K ROM Devices)

Device Address	Description
0000h-007Fh	Reserved (1)
0080h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved (1)
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved (1)
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Note 1. Reserved Areas should be filled with FFh

ORDERING INFORMATION TABLE

Sales Type	ROM x8	I/O	Additonal Features	Temperature Range	Package
ST6210BB1/XXX ST6210BB6/XXX	2K Bytes	12	A/D CONVERTER	0 to +70°C -40 to +85°C	PDIP20
ST6210BM1/XXX ST6210BM6/XXX				0 to +70°C -40 to +85°C	PSO20
ST6215BB1/XXX ST6215BB6/XXX		20	A/D CONVERTER	0 to +70°C -40 to +85°C	PDIP28
ST6215BM1/XXX ST6215BM6/XXX				0 to +70°C -40 to +85°C	PSO28
ST6220BB1/XXX ST6220BB6/XXX	4K Bytes	12	A/D CONVERTER	0 to +70°C -40 to +85°C	PDIP20
ST6220BM1/XXX ST6220BM6/XXX				0 to +70°C -40 to +85°C	PSO20
ST6225BB1/XXX ST6225BB6/XXX		20	A/D CONVERTER	0 to +70°C -40 to +85°C	PDIP28
ST6225BM1/XXX ST6225BM6/XXX				0 to +70°C -40 to +85°C	PSO28

Note: /XXX is a 2-3 alphanumeric character code added to the generic sales type on receipt of a ROM code and valid options.

ST6210B, ST6215B , ST6220B, ST6225B MICROCONTROLLER OPTION LIST

Customer . . . . . .
Address . . . . . .
. . . . . .
Contact . . . . . .
Phone No . . . . . .
Reference . . . . . .

SGS-THOMSON Microelectronics references

Device: [ ] ST6210B [ ] ST6215B [ ] ST6220B [ ] ST6225B

Package: [ ] Dual in Line Plastic [ ] Small Outline Plastic
In this case, select conditioning
[ ] Standard (Stick)
[ ] Tape & Reel

Temperature Range: [ ] 0°C to + 70°C [ ] – 40°C to + 85°C

Special Marking: [ ] No
[ ] Yes "_ _ _ _ _ _ _ _ _ _"
Authorized characters are letters, digits, '.', '–', '/' and spaces only.
Maximum character count DIP20 - DIP28: 10
SO20 - SO28:8

Oscillator Source Selection: [ ] Crystal/Resonator
[ ] RC Network

Watchdog Selection: [ ] Software Activation (STOP mode available)
[ ] Hardware Activation (no STOP mode)

OSG: [ ] Enabled
[ ] Disabled

Input pull-up selection on NMI pin : [ ] Yes [ ] No

Input pull-up selection on TIMER pin : [ ] Yes [ ] No

ROM Readout Protection: Please contact your local SGS-THOMSON Sales Office

Comment :
Supply Operating Range in the application: [ ] 3.0V to 6.0V
[ ] 4.5V to 6.0V

Notes . . . . . .
. . . . . .

Signature . . . . . .

Date . . . . . .