2048 x 8 EPROM
UV Erasable

Synertek®
INCORPORATED

SY2716

MEMORY PRODUCTS

Preliminary

- Single +5 Volt Power Supply
- Low Power Dissipation
  -525 mW Maximum
  132 mW Standby
- Access Time - 350nsec to 450nsec
- Totally Static Operation
- Pin Compatible With SY2316B, and SY2333 Mask Programmable ROMs
- Single Address Programming with 50msec Pulse
- TTL Compatible - Read and Program On All Inputs and Outputs

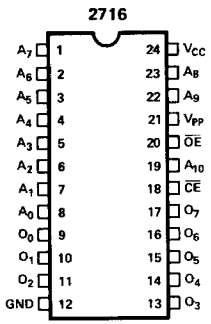
The SY2716 is a 16384-Bit electrically programmable, ultra-violet erasable, read-only memory. Organized 2048 words by 8 bits, the SY2716 operates from a single 5 volt power supply and is completely static in operation, requiring no clocks. In addition, a Chip Enabled controlled standby mode reduces the active power dissipation of 525 milliwatts to 132 milliwatts in standby, a 75% power savings.

The SY2716 is pin compatible with the existing 16K and 32K ROMs (SY2316B, SY2332), permitting simple conversion from EPROM prototype systems to mask programmable ROM production systems.

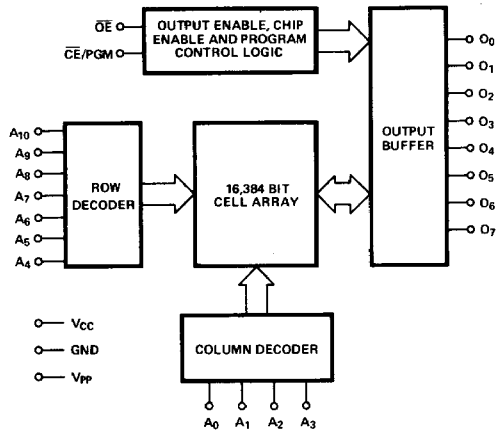
Programming the SY2716 is completely TTL compatible and requires no high voltage pulses. The SY2716 therefore can easily be programmed on PC boards in the system. In addition, each word can be individually programmed with the SY2716's single address programming. Total programming time for all 16384 bits is less than two minutes.

The high speed operation of the SY2716 (350nsec to 450nsec) makes this device ideal for use with high performance microprocessor systems now in production.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time	Temperature Range
SYC2716	450nsec	0°C to +70°C
SYC2716-1	350nsec	0°C to +70°C
SYC2716-2	390nsec	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7V
Power Dissipation	1.0W
V_{PP} (Program Voltage)	-0.3V to +26.5V

NOTE: During application of power, care must be taken to assure that V_{CC} is applied before or simultaneously with V_{PP}. V_{PP} must be removed before or simultaneously with V_{CC}.

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

READ D.C. CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5% (2716, 2716-2); V_{CC} = 5.0V ±10% (2716-1); V_{PP} = V_{CC} ±0.6V (Unless otherwise specified)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Conditions
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V Note 1
I_{PP1}	V_{PP} Current			5	mA	V_{PP} = 5.85V Note 1
I_{CC1}	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} Note 1
I_{CC2}	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400μA

NOTE 1. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.

READ A.C. CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5% (2716, 2716-2); V_{CC} = 5.0V ±10% (2716-1); V_{PP} = V_{CC} ±0.6V (unless otherwise specified)

Symbol	Parameter	2716 Limits Min	Typ	Max	2716-1 Limits Min	Typ	Max	2716-2 Limits Min	Typ	Max	Unit	Test Conditions
t_{ACC}	Address to Output Delay			450			350			390	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay			450			350			390	ns	$\overline{OE}$ = V_{IL}
t_{OE}	Output Enable to Output Delay			120			120			120	ns	$\overline{CE}$ = V_{IL}
t_{DF}	Output Enable High to Output Float	0		100	0		100	0		100	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Address to Output Hold	0			0			0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

A.C. Test Conditions

Input Pulse Levels ..... 0.8V to 2.0V
Input Rise and Fall Time 20nsec
Timing Measurement Levels: Input 1.5V
Output ..... 0.8 and 2.0V
Output Load ..... 1 TTL Gate and 100pF

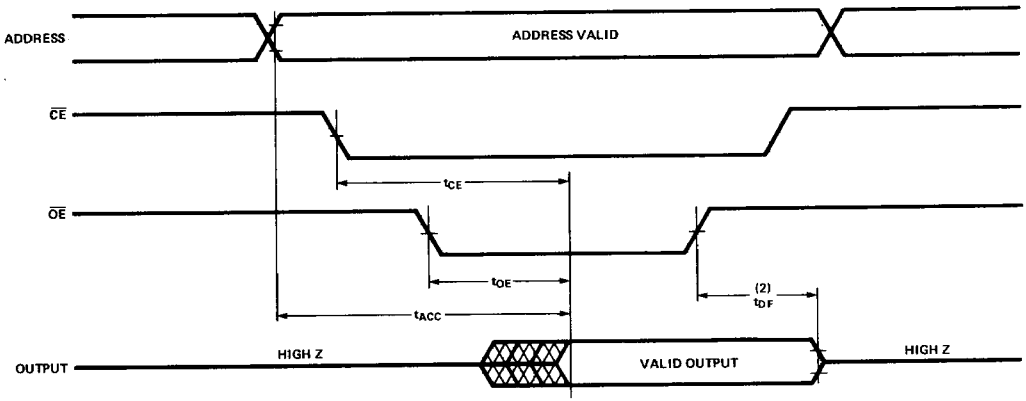
CAPACITANCE

T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

NOTE: This parameter is sampled and not 100% tested.

READ TIMING DIAGRAM



NOTE 2: t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

PROGRAMMING D.C. CHARACTERISTICS

T_A = 25°C ± 5°C; V_{CC} = 5V ± 5%; V_{PP} = 25V ± 1V

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Current (for any input)			10	μA	V_{IN} = 5.25V/0.45
I_{PP1}	V_{PP} Supply Current			5	mA	$\overline{CE}$/PGM = V_{IL}
I_{PP2}	V_{PP} Supply Current During Programming Pulse			30	mA	$\overline{CE}$/PGM = V_{IH}
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	-0.1		0.8	V	
V_{IH}	Input High Level	2.0		V_{CC}+1	V	

NOTE: During programming care must be taken to avoid Vpp transients exceeding the +26 volt maximum.

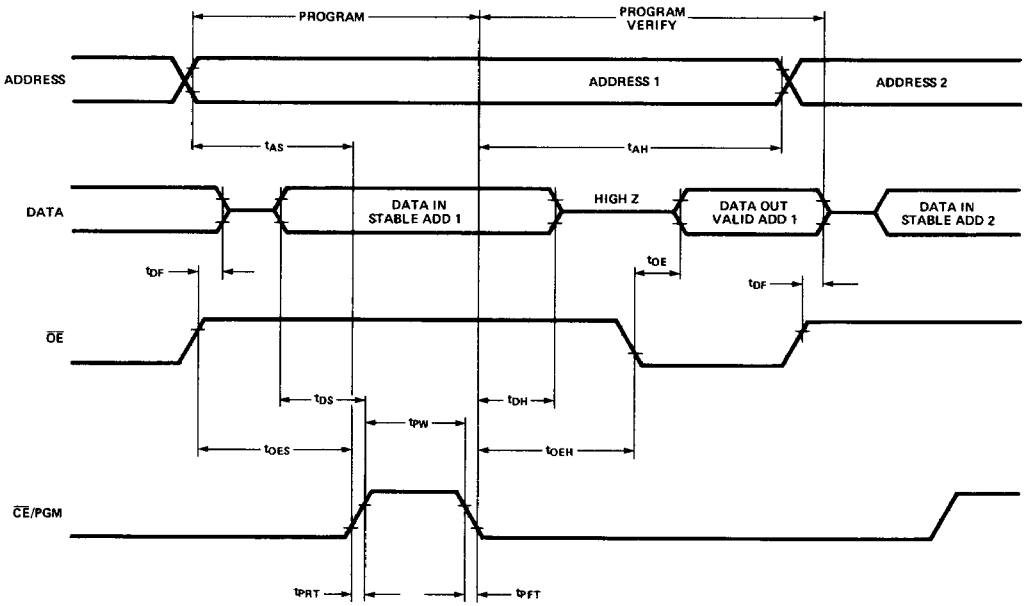
PROGRAMMING A.C. CHARACTERISTICS

T_A = 25°C ± 5°C; V_{CC} = 5V ±5%; V_{PP} = 25V ± 1V

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Output Enable to Output Float Delay	0		120	ns	$\overline{CE}$/PGM = V_{IL}
t_{OE}	Output Enable to Output Delay			120	ns	$\overline{CE}$/PGM = V_{IL}
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTE: During application of power, care must be taken to assure that V_{CC} is applied before or simultaneously with Vpp. Vpp must be removed before or simultaneously with V_{CC}. The maximum allowable voltage during programming which may be applied to the Vpp with respect to ground is +26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding the 26V maximum specification. For convenience in programming, the 2716 may be verified with the Vpp supply at 25V ± 1V. During normal read operation, however, Vpp must be at V_{CC}.

PROGRAMMING TIMING DIAGRAM



ERASURE

Erasure of the SY2716 begins to occur when exposed to light with wavelengths shorter than 4000 angstroms. Certain types of ambient light contain wavelengths in this range. Although exposure to sunlight or fluorescent light for a relatively long time is required to cause erasure, care should be taken to avoid exposure to this type of light for extended periods.

Erasing the SY2716 is accomplished by exposing the device to ultra violet light with a wavelength of 2537 angstroms. The minimum dose (integrated) required for erasure is 15 W-sec/cm^2 (intensity at the device x exposure time). A 12 mW/cm^2 lamp (without filter) placed one inch from the device will require about 20 minutes for complete erasure. After erasure, all bits are in the logic "1" state.

A.C. CONDITIONS OF TEST:

V_{CC}	5V ±5%
V_{PP}	25V ±1V
Input Rise and Fall Times (10% to 90%)	20 ns
Input Pulse Levels	0.8V to 2.2V
Input Timing Reference Level	1V and 2V
Output Timing Reference Level	0.8V and 2V

OPERATIONAL DESCRIPTION

MODE \ PINS	$\overline{CE}$/PGM	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

1. Programming
Initially, at delivery, all bits of the SY2716 have been erased, and, therefore, are in the logic "1" state. Data is programmed into each memory word by introducing logic "0"s at each desired bit. The 2716 programming mode is selected by applying +25 volts to the V_{PP} power pin and holding the $\overline{OE}$ Input in a logic "1" state. The data to be programmed is applied in an 8 bit parallel format to the Data Output pins. Addresses, as well as the data applied to the output pins, are completely TTL compatible. A 50 millisecond TTL level programming pulse is then applied to the $\overline{CE}$/PGM input to complete programming.

A TTL level Program pulse must be applied for each address location to be programmed. However, address locations may be selected at random, either individually or sequentially.

Because of this simple programming procedure, multiple 2716s can easily be programmed in parallel. Inputs of each of the devices are simply connected together and then common Data, Address and Program signals are applied to all devices simultaneously.

2. Program Inhibit
Because programming of the SY2716 is totally controlled by the $\overline{CE}$/PGM input, multiple 2716s can be simply programmed in parallel with different data. Addresses and Data Output pins of each device are connected in common to the desired data source. The specific 2716 to be programmed is then selected by applying a TTL logic "1" voltage level to the $\overline{CE}$/PGM pin of the desired device. Programming of all other devices connected in parallel is inhibited with a TTL logic "0" input on the $\overline{CE}$/PGM input.

3. Program Verify
Immediately following the programming of an SY2716 EPROM, each of the data words should be read to assure accurate programming. This verify may be performed with V_{PP} held at +25 volts by applying a low level TTL logic signal ("0") to the $\overline{OE}$ Input. Except during the verify and programming operations, V_{PP} should be held at +5 volts (V_{CC}).

4. Read Mode
The read mode is selected by holding both $\overline{CE}$/PGM and $\overline{OE}$ Inputs at a TTL logic "0" level while applying 5.0V power to both V_{CC} and V_{PP} inputs. Appropriate data previously programmed into the selected address then appears in the Data Output pins. Chip Enable ($\overline{CE}$) is the power control, and must be used to select the device. Output Enable ($\overline{OE}$) controls only the output stages and must be used to gate data to the Output pins independently of device selection.

5. Standby Mode
Power dissipation of the SY2716 is controlled by the $\overline{CE}$ input and can be reduced to standby power level (132 milliwatts max) simply by applying a TTL logic "1" signal to the $\overline{CE}$ Input. Whenever $\overline{CE}$ is in the logic "1" state, Outputs are in a high impedance state, independent of the $\overline{OE}$ input status.

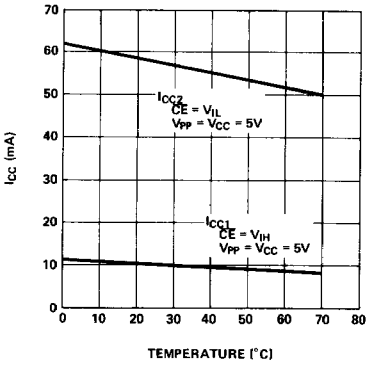
6. Output Control
The outputs of multiple SY2716s may be or-tied to provide memory expansion. Since these outputs will be tied in common to the same data bus, only one SY2716 should be selected ($\overline{OE}$ Logic "0" level) to prevent data bus contention between SY2716s or other memory circuits connected to the bus. The output of the desired SY2716 is enabled simply by providing a TTL logic "0" signal to the $\overline{OE}$ Input. Conversely, outputs of other 2716s are deselected by applying a logic "1" signal to their $\overline{OE}$ Inputs.

PROGRAMMING

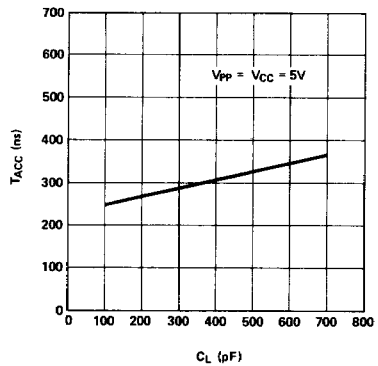
The SY2716 is programmed by selectively programming logic "0"s in the memory matrix set initially in the all logic "1" state by erasure. Only logic "0"s can be programmed electrically; logic "1"s can only be obtained by UV erasure. Programming is accomplished by applying a 50msec TTL pulse to the $\overline{CE}$/PGM pulse with 25V ±1V applied to V_{PP} and a TTL logic "1" applied to the $\overline{OE}$ input. The specific word to be programmed is selected with the address inputs, and the data to be programmed is applied to the data output pins.

TYPICAL CHARACTERISTICS

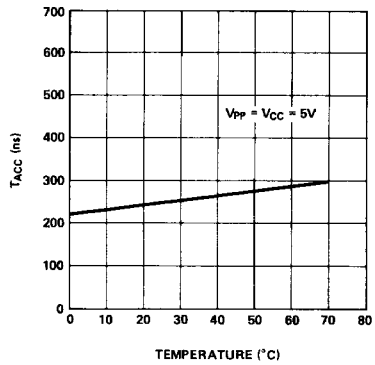
I_{CC} CURRENT VS. TEMPERATURE



ACCESS TIME VS. CAPACITANCE



ACCESS TIME VS. TEMPERATURE



PACKAGE DIAGRAM