27C256–IND
256K (32K × 8) EPROMs
Industrial Temperature Range

Product Specification

Application Specific Products

DESCRIPTION

Signetics 27C256 CMOS EPROM is a 256K-bit 5V only memory organized as 131,072 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27256.

The 27C256 is specified to operate over the industrial temperature range of −40°C to +85°C with no degradation in performance.

The 27C256 is available in both the windowed Ceramic DIP, the plastic DIP and the PLCC Packages. This device can be programmed with standard EPROM programmers.

FEATURES

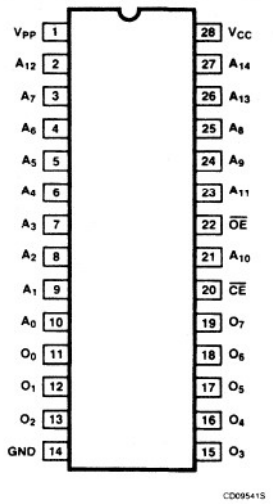
- **Low power consumption**
  - **100μA maximum CMOS standby current**
- **Quick pulse programming algorithm for high-speed production programming (4 second typical programming times)**
- **High-performance speeds**
  - **27C256I15: 150ns maximum access time**
  - **27C256I20: 200ns maximum access time**
- **Noise immunity features**
  - **± 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**

PIN DESCRIPTION

$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply
N.C.	No Connection
D.U.	Don't Use

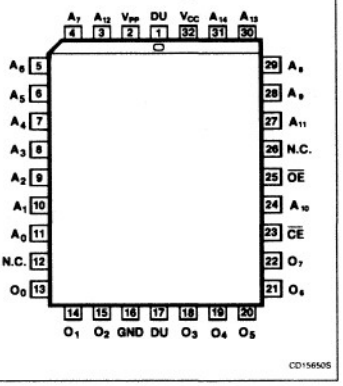
PIN CONFIGURATIONS

FA and N Packages



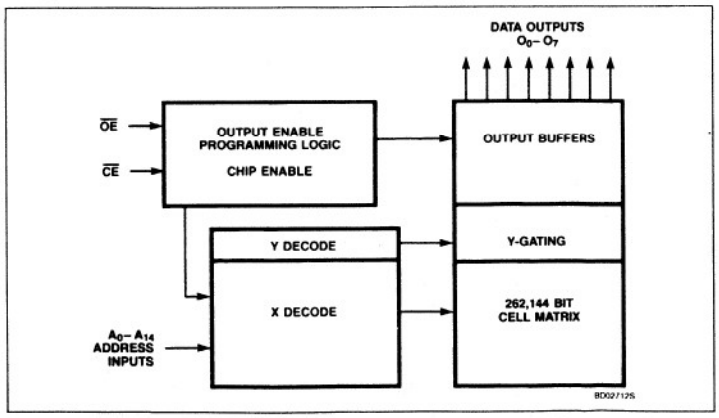
CD09541S

A Package



CD15650S

BLOCK DIAGRAM



BD02712S

READ MODE: 27C256

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C256 has a standby mode which reduces the maximum V_{CC} current to 100μA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin CERDIP with quartz window (600mil-wide)	27C256I15 FA 27C256I20 FA
28-pin Plastic Dual in-line (600mil-wide)	27C256I15 N 27C256I20 N
32-pin Plastic Leaded Chip Carrier (450 × 550mil)	27C256I15 A 27C256I20 A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Temperature under bias	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_I, V_O	Voltage inputs and outputs	−2.0 to (V_{CC} + 1)	V
V_H	Voltage on A_9[2] (During intelligent identifier interrogation)	−2.0 to +13.5	V
V_{PP}	Voltage on V_{PP}[2] (During programming)	−2.0 to +14.0	V
V_{CC}	Supply voltage[2]	−2.0 to +7.0	V

NOTE:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages are with respect to network ground.

DEVICE OPERATION[2]

MODE	$\overline{CE}$	$\overline{OE}$[10]	V_{PP}[8]	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

Notes on following page.

DC ELECTRICAL CHARACTERISTICS $-40°C \leq T_A \leq +85°C$, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Input current						
I_{IH}	Leakage	$V_{IN} = 5.5V = V_{CC}$		0.01	1.0	µA
I_{IL}	Low	$V_{IL} = 0.45V$		0.01	1.0	µA
I_{PP}	V_{PP} read	$V_{PP} = V_{CC}$			100	µA
Output current						
I_{LO}	Leakage	$\overline{OE}$ or $\overline{CE} = V_{IH}$ $V_{OUT} = 5.5V = V_{CC}$			1.0	µA
		$V_{OUT} = 0V = GND$			1.0	µA
I_{OS}	Short circuit[7, 9]	$V_{OUT} = 0V$			100	mA
Supply current						
I_{CC} TTL	Operating (TTL inputs)[4]	$\overline{CE} = \overline{OE} = V_{IL}$, f = 6.7MHz $V_{PP} = V_{CC}$ $O_{0-7} = 0mA$			20	mA
I_{SB} TTL	Standby (TTL inputs)[4]	$\overline{CE} = V_{IH}$			1.0	µA
I_{SB} CMOS	Standby (CMOS inputs)[5, 6]	$\overline{CE} = V_{IH}$			100	µA
Input voltage[2]						
V_{IL}	Low (TTL)	$V_{PP} = V_{CC}$	−0.5		0.8	V
V_{IL}	Low (CMOS)	$V_{PP} = V_{CC}$	−0.2		0.2	V
V_{IH}	High (TTL)	$V_{PP} = V_{CC}$	2.0		$V_{CC} + 0.5$	V
V_{IH}	High (CMOS)	$V_{PP} = V_{CC}$	$V_{CC} - 0.2$		$V_{CC} + 0.2$	V
V_{PP}	Read[8]	(Operating)	$V_{CC} - 0.7$		V_{CC}	V
Output voltage[2]						
V_{OL}	Low	$I_{OL} = 2.1mA$			0.45	V
V_{OH}	High	$I_{OH} = -2.5mA$	3.5			V
Capacitance[9] $T_A = 25°C$						
C_{IN}	Address and control	$V_{CC} = 5.0V$ f = 1.0MHz			6	pF
C_{OUT}	Outputs	$V_{IN} = 0V$ $V_{OUT} = 0V$			12	pF

NOTES:

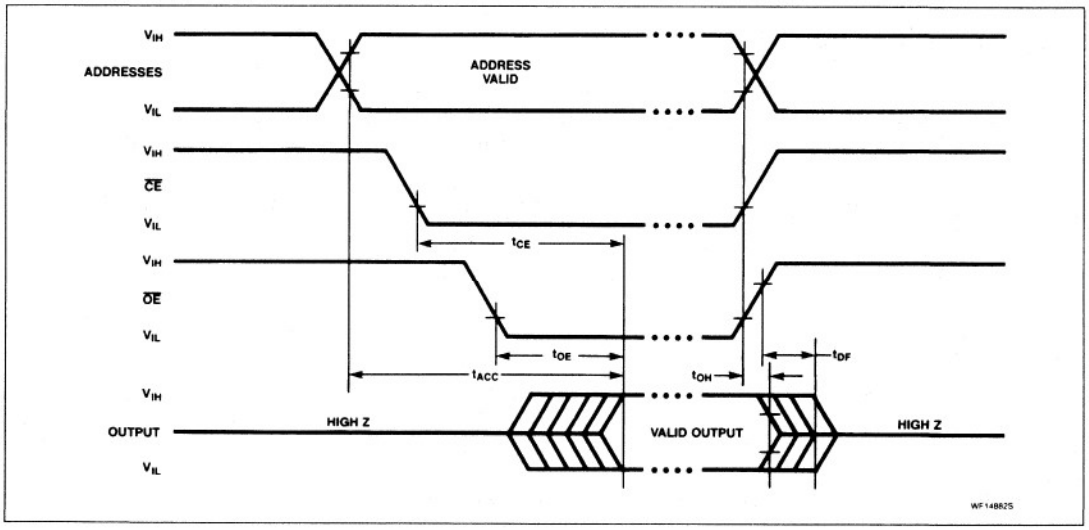
1. Minimum DC input voltage is −0.5V. During transitions the inputs may undershoot to −2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_A = 25°C$.
4. TTL inputs: Specification V_{IL}, V_{IH} levels.
   CMOS inputs: GND ±0.2V to V_{CC} ±0.2V.
5. $\overline{CE}$ is V_{CC} ±0.2V. All other inputs can have any value within specification.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 5MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC}, and can be connected directly to V_{CC}.
9. Guaranteed by design, not 100% tested.
10. X can be V_{IH} or V_{IL}.

AC ELECTRICAL CHARACTERISTICS $-40°C \leq T_A \leq +85°C$, $+4.5V \leq V_{CC} \leq +5.5V$, $R_L = 660\Omega$, $C_L = 100pF$

SYMBOL	TO	FROM	27C256I15		27C256I20		UNIT
			Min	Max	Min	Max	
Access time[1]							
t_{ACC}	Output	Address		150		200	ns
t_{CE}	Output	$\overline{CE}$		150		200	ns
t_{OE}[3]	Output	$\overline{OE}$		65		75	ns
Disable time[2]							
t_{DF}[4]	Output Hi-Z	$\overline{OE}$ or $\overline{CE}$		45		55	ns
t_{OH}	Output hold	Address, $\overline{CE}$ or $\overline{OE}$	0		0		ns

NOTES:
1. AC characteristics are tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$. Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed by design, not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

AC VOLTAGE WAVEFORMS



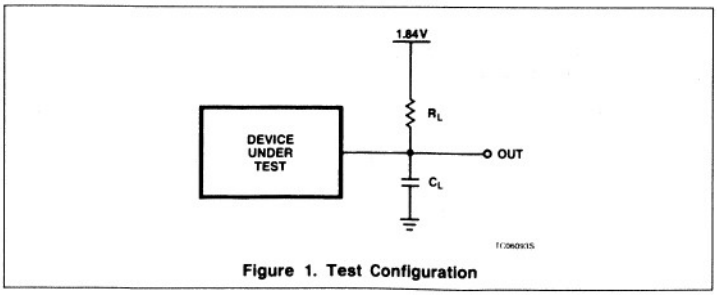


Figure 1. Test Configuration